IBM®

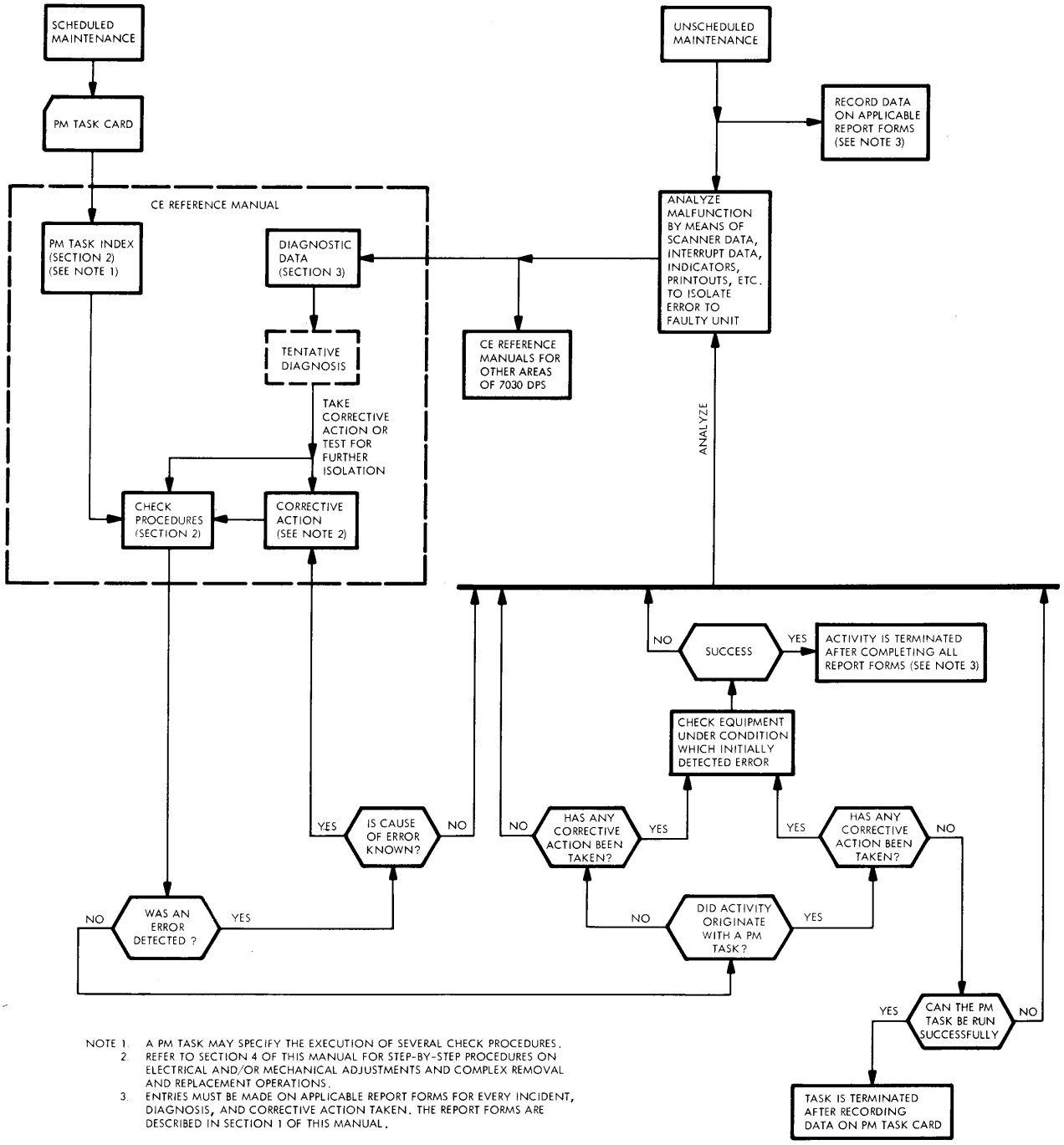
Customer Engineering

Reference Manual

7030 Data Processing System

Manual 04

7101 Central Processor Unit



NOTE 1. A PM TASK MAY SPECIFY THE EXECUTION OF SEVERAL CHECK PROCEDURES.
2. REFER TO SECTION 4 OF THIS MANUAL FOR STEP-BY-STEP PROCEDURES ON ELECTRICAL AND/OR MECHANICAL ADJUSTMENTS AND COMPLEX REMOVAL AND REPLACEMENT OPERATIONS.
3. ENTRIES MUST BE MADE ON APPLICABLE REPORT FORMS FOR EVERY INCIDENT, DIAGNOSIS, AND CORRECTIVE ACTION TAKEN. THE REPORT FORMS ARE DESCRIBED IN SECTION 1 OF THIS MANUAL.

MAINTENANCE PLAN (Frontispiece)

SECTION 1
INTRODUCTION AND SAFETY

PURPOSE AND SCOPE OF MANUAL

This manual provides IBM Customer Engineers with information necessary to perform preventive and corrective maintenance on the 7101 Central Processor Unit. In addition, the manual contains reference material which will help the Customer Engineer to analyze malfunctions within this unit.

MANUAL CONTENT

The material in this manual is grouped into six sections. The content of each section is briefly described below:

Section 1 Introduction and Safety - This section defines the purpose, scope, content, and format of the manual. In addition, the section contains a brief analysis of the maintenance plan as illustrated by the frontispiece, a brief listing of general safety practices, procedures for performing artificial respiration, and a summary of the personnel safety practices that must be observed when working on the subject unit.

Section 2 Check Procedures - This section contains the step-by step procedures that are required to accomplish preventive maintenance tasks. These procedures (referenced in Index 2-1) are used to execute physical maintenance and/or to test the performance of the subject unit to determine and ensure its satisfactory operation. This section also contains additional procedures which are referenced in the Diagnostic Data section to help and isolate equipment malfunctions. The material in this section is preceded by four indexes which cross-reference preventive maintenance tasks with their associated check procedures and which list the procedures, illustrations, and tables contained in this section.

Section 3 Diagnostic Data - This section contains reference material which is intended to assist the Customer Engineer in isolating equipment malfunctions. The reference material is grouped into categories such as: physical description; flow, block, and simplified logic diagrams; timing and sequence charts; lists of indications, switches, and applicable maintenance programs; and error analysis. The material in this section is preceded by three indexes which list the information categories, illustrations, and tables contained in this section.

Section 4 Corrective Procedures - This section contains the step-by-step procedures that should be used to accomplish electrical and/or mechanical adjustments and to perform complex removal and replacement operations. The material in this section is preceded by three indexes which list the information categories, illustrations, and tables contained in this section.

Section 5 Customer Engineering Memo's (CEM's) - This section is reserved for filing Customer Engineering Memo's that relate to the subject unit.

Section 6 Miscellaneous - This section is reserved for miscellaneous notes, etc., that the Customer Engineer considers pertinent for maintenance of the subject unit.

MANUAL FORMAT

The page, figure, table, and index coding scheme used in this manual was devised so that new and revised material can be inserted at any point without destroying the existing structure of the manual. Since Customer Engineering memo's and notes are filed in sequential order in Sections 5 and 6, the coding scheme described below will pertain only to Sections 1 through 4.

Page Coding

The upper-inner corner of each page in Sections 1 through 4 contains an alphanumeric code (M3-XX-X) which denotes the following:

Code M3 - specifies the 7030 series of CE reference manuals.

Code XX - specifies the manual number within the series.

Code X - specifies the section within the manual.

The lower-outer corner of each page (except the indexes) in Sections 1 through 4 is reserved for the page number. In Section 1, this corner contains a 1-digit number to specify the consecutive page numbers within this section. In Sections 2, 3, and 4, this corner contains a hyphenated 2-digit code which denotes the following:

1st digit - specifies the procedure or category number as per Index 2-2, 3-1, or 4-1.

2nd digit - specifies page number within the procedure or category.

The upper-outer corner of each page (except the indexes) in Sections 1 through 4 is reserved for subject identification. In Section 1, this corner contains the section title. In the body of Sections 2, 3, and 4, this corner contains the procedure or category title as per Index 2-2, 3-1, or 4-1. In the index pages of Sections 2, 3, and 4, this corner contains the section number and section title.

The lower-inner corner of each page in Sections 1 through 4 contains the page release date which is used for revision control purposes.

Figure and Table Coding

The figures and tables contained in Sections 2, 3, and 4 are identified by a 3-digit code (Figure/Table X. X. X) which denotes the following:

1st digit - specifies the section in which the figure or table is contained.

2nd digit - specifies the associated procedure or category within the section.

3rd digit - specifies the figure or table number within the procedure or category.

Index Coding

Each index in Sections 2, 3, and 4 is identified by a hyphenated 2-digit code (Index X-X) which denotes the following:

1st digit - specifies the section within the manual.

2nd digit - specifies the index number within the section.

MAINTENANCE PLAN ANALYSIS

The approach to preventive and unscheduled maintenance of the 7030 Data Processing System is shown and explained graphically in the frontispiece, entitled MAINTENANCE PLAN. The procedures to be followed in performing each type of maintenance are briefly described below:

Preventive Maintenance - All scheduled preventive maintenance operations to be performed on the 7030 Data Processing System are controlled, scheduled, and assigned by preventive maintenance (PM) Task Assignment Cards. When a preventive maintenance task is scheduled for execution, the CE manager will give the associated PM Task Assignment Card to one of his men. This card identifies the PM task by a 2-digit number and specifies which manual of the 7030 series of Customer Engineering Reference manuals is related to this task. Index 2-1 of the referenced manual identifies which check procedures are to be executed to accomplish this PM task.

If all of the check procedures associated with a PM task can be performed satisfactorily, the task is completed when the CE enters all pertinent information on the Task Assignment Card and returns it to his manager. However, if a malfunction is detected during the execution of a check procedure the CE must perform the following:

1. Make a tentative diagnosis of the malfunction. This diagnosis can be based on past experience or on an analysis of scanner information, interrupt data, indicators, printouts, etc., and on the diagnostic data in Section 3 of the associated 7030 CE reference manual.

2. Either take corrective action and check the results by executing an applicable check procedure or execute an appropriate check procedure to further isolate the malfunction.

3. Repeat steps 1 and 2, above, until the cause of the malfunction has been analyzed, corrected, and checked.

4. Check the equipment under conditions which initally detected the malfunction. If the equipment still does not operate properly, repeat steps 1 through 4, above.

5. Record all pertinent information, such as failure indications, programs, and check procedures used for error isolation, defective component type and location, start-stop time, total man-hours, etc., on a Maintenance Activity Form. If additional space is required for the report, supplement the above with a Comments Form. In addition, if components have been replaced, complete a Failed Parts Return Form which will be sent with the defective part to the manufacturing plant.

6. Continue execution of the PM task. If another malfunction is detected, repeat steps 1 through 5, above.

7. After the PM task has been satisfactorily completed, enter all pertinent information on the PM Task Assignment Card and return the card to the CE manager.

Unscheduled Maintenance

Unscheduled maintenance is generally performed on-line to correct malfunctions that render the system inoperative for customer use. Whenever an operational malfunction is detected, the CE should perform the following:

1. Enter pertinent information concerning the incident in the Operations Log and record the error information on a Maintenance Activity Form. Detailed instructions for completing these forms are contained in the 7030 Data Reporting Procedures manual.

2. Make a tentative diagnosis of the malfunction. This diagnosis can be based on past experience, on an analysis of scanner information, interrupt data, indicators, printouts, etc., and/or on an analysis of the diagnostic data contained in Section 3 of the associated 7030 CE reference manual.

3. Determine whether temporary repairs will make the system operational for customer use. That is, if the system can be made operational by bypassing the malfunctioning section of the equipment (e.g., Lookahead level) or by replacing a faulty unit or section of the equipment (e.g., tape drive, exchange channel, etc.), then only temporary repairs should be made and the malfunction should be corrected either on an off-line basis or during the subsequent scheduled maintenance period. If temporary repairs are feasible, perform them and proceed to step 6. If temporary repairs are not possible, proceed to step 4.

4. Take corrective action and check the results by executing an applicable check procedure or execute an appropriate check procedure to further isolate the malfunction.

5. Repeat steps 2 through 4, above, until the cause of the malfunction has been analyzed, corrected, and checked.

6. To ensure that the temporary or permanent repairs are satisfactory, check the equipment under conditions which initially detected the malfunction. If the equipment still does not operate properly, repeat steps 2 through 5, above.

7. Return the system to customer use, and record all pertinent information in the Operations Log. If temporary repairs were performed, the incident should not be "closed out" on the Maintenance Activity Form until the malfunction has been corrected.

8. After the maintenance activity is terminated (on-line, off-line, or during scheduled maintenance time), record all pertinent information, such as: failure indications, programs and check procedures used for error isolation, corrective action taken, defective component type and location, start-stop time, total man-hours, etc., on the Maintenance Activity Form. If additional space is required for the report, supplement the above with a Comments Form. If any components have been replaced, complete a Failed Parts Return Form which will be sent with the defective part to the manufacturing plant.

SAFETY

Safety cannot be overemphasized. To ensure personal safety and the safety of co-workers, each CE should make it an everyday practice to observe safety precautions at all times. All CE's should become familiar with the general safety practices and procedures for performing artificial respiration that are outlined in IBM Form 124-0002. For convenience, this form is duplicated below.

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM Equipment:

1. Do not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your Manager if you MUST work alone.
2. Remove all power AC & DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked in off position.
4. When it is absolutely necessary to work on equipment having exposed live electrical circuitry anywhere in the machine, the following precautions must be followed:
   a. Another person familiar with power off controls must be in the immediate vicinity.
   b. Rings, wrist watches, chains and bracelets shall not be worn.
   c. Safety glasses shall be worn.
   d. Only insulated pliers or screwdrivers shall be used.
   e. Keep one hand in pocket.
   f. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   g. Avoid contacting ground potential (metal floor strips, machine frames, etc.)
5. Safety glasses must be worn when working on live equipment, soldering, drilling, driving pins and all other conditions that may be hazardous to the eyes.
6. Special safety instructions for handling Cathode Ray Tubes and extreme high voltages must be followed as outlined in CEM's.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Do not lift machines or devices weighing in excess of 60 lbs.
11. All safety changes must be ordered and installed in the prescribed manner.
12. All safety devices such as guards, shields, signs, etc. shall be restored after maintenance.
13. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
14. All machine covers must be in place before machine is returned to customer.
15. Maintain good housekeeping in area of machines while performing and after completing maintenance.
16. Avoid wearing loose clothing that may be caught in moving machinery.

KNOWING SAFETY RULES IS NOT ENOUGH
OBSERVE THEM — FOLLOW THEM
USE GOOD JUDGMENT

THINK SAFETY WORK SAFELY

FORM # 24-0002-1

Standard Technique
LAY VICTIM IN PRONE POSITION

Elbows bent, one hand on the other. Head on hands, face to one side. Kneel at victim's head on either or both knees.

1 PLACE HANDS

Fingers spread, thumbs touching, heels of hands just below a line between armpits.

2 APPLY PRESSURE

Rock forward slowly until arms are vertical. Keep elbows straight.

3 RELEASE PRESSURE

Rock back slowly. Grasp victim's arms just above elbows. Continue backward.

4 LIFT ARMS

Raise arms until tension is felt for maximum chest expansion. Lower arms to complete cycle.

REPEAT CYCLE 12 TIMES PER MINUTE

Photos Courtesy American National Red Cross

Artificial Respiration
GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count** Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions** Remove foreign objects—Pull tongue forward.
3. **Loosen Clothing — Keep Warm** Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position** After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor** Have someone summon medical aid.
6. **Don't Give Up** Continue without interruption until victim is breathing without help or is certainly dead.

Reprint Courtesy Mine Safety Appliances Co.

Rescue Breathing for Adults
Victim on His Back Immediately

1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. **Blow** until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.

Thumb and finger positions

Final mouth to mouth position

POWER DOWN ON SIGMA ONLY

1. Turn off AC and DC switches on front of SIGMA maintenance console (frame 31).

2. Turn off AC and DC switches on front of PDF labeled SIGMA.

3. Turn off CB5 and CB10 on front of PDF.

4. Turn off CB26 and CB30 located (right side facing unit) on PDF. CB26 de-energizes cube blowers, and CB30 de-energizes all service outlets. If CB30 is left on, bus 14 will be energized in frame 31.

CAUTION

-48vdc will be present on emergency-off (EMO) switches in frames 31 and 28.

5. Tag AC and DC switches turned off on PDF with appropriate Warning Tags.

INDEX 2-1. PREVENTIVE MAINTENANCE (PM) TASKS

PM TASK NUMBER	PM TASK TITLE	CHECK PROCEDURES TO BE EXECUTED
01	SEVA Reliability	(Refer to program writeup)
02	I-Box	(Refer to program writeup)
03	SAU Test Program	(Refer to program writeup)
04	PAU Test Program	(Refer to program writeup)
05	I Chkr Program	(Refer to program writeup)
06	KC BA1 Memory 1	(Refer to program writeup)
07	Memory 2	(Refer to program writeup)
08	I Box Program with Bias	(Refer to program writeup)
09	K Prime	(Refer to program writeup)
10	Lookahead	(Refer to program writeup)
11	A-Checker	(Refer to program writeup)
12	Interrupt	(Refer to program writeup)
13	SAU Program with Bias	(Refer to program writeup)
14	PAU Program with Bias	(Refer to program writeup)
15	I Chkr Program with Bias	(Refer to program writeup)
16	Memory 1 with Bias	(Refer to program writeup)
17	Memory 2 with Bias	(Refer to program writeup)
18	Deleted	

INDEX 2-1. PREVENTIVE MAINTENANCE (PM) TASKS (cont'd)

PM TASK NUMBER	PM TASK TITLE	CHECK PROCEDURES TO BE EXECUTED
19	Filter Check FR 11-16	2
20	Filter Check FR 17-22	2
21	Filter Check FR 23-28	2
22	Gate Fan Check	3
23	Check Hardware	4
24	Power Supply Check	No. 2 of Manual 02
25	Sample Pulse Alignment Check	1
26	Check Clamp Supply Voltage	9
27	Word Driver Tuning, Turn-on Time	7
28	Index Tunnel Diode Storage Tuning Program	6
29	Chk Turn Latitude 15 SA-BD	6
30	Chk Word Driver Outputs Top and Bottom	7
31	Check Strobe and Latch Drivers	8
32	Check Data In	9
33	Chk +12VDC Power Supply	Corrective Procedure 2
34	Error Trigger Check	11

INDEX 2-2. CHECK PROCEDURES

PROCEDURE NUMBER	PROCEDURE TITLE	ISSUE DATE
1	Sample Pulse Alignment Check	2/1/62
2	Filter Check	7/1/61
3	Gate Fan Check	12/1/61
4	Gate Latch and Slide Check	12/1/61
5	Index Core Storage Check (for CPU 7101, Serial Nos. 30,000-30,005 and 30,007 only)	1/1/63
6	Index Tunnel Diode Storage Tuning Program (for CPU 7101, Serial Nos. 30,006 and 30,008)	1/1/63
7	Word Driver Tuning Turn-On Time	1/1/63
8	Latch and Strobe Drivers	1/1/63
9	Clamp Supply Voltage	1/1/63
10	Data-In Pulse	1/1/63
11	Error Trigger Check	1/1/63

INDEX 2-3. LIST OF ILLUSTRATIONS

FIGURE NUMBER	FIGURE TITLE	ISSUE DATE
2.5.1	Dropped Bits, Flow Chart	12/1/61
2.5.2	Picked Bits, Flow Chart	12/1/61
2.5.3	Index Core Storage, Simplified Logic	12/1/61
2.5.4	Index Core Storage, Waveforms (1)	12/1/61
2.5.5	Index Core Storage, Waveforms (2)	12/1/61
2.7.1	Word Driver Output Waveshape	1/1/63
2.8.1	Example of Fetch Timing for Index Tunnel Diode Storage	1/1/63
2.10.1	Example of Store Timing for Index Tunnel Diode Storage	1/1/63
2.10.2	Tunnel Diode Array Card Inputs	1/1/63

INDEX 2-4. LIST OF TABLES

TABLE NUMBER	TABLE TITLE	ISSUE DATE
2.1.1	CPU Sample Test Points	2/1/62
2.5.1	SA Groups	12/1/61
2.5.2	Index Core Storage Array Test Points	12/1/61
2.7.1	Word Driver, Test Points	1/1/63
2.8.1	Latch Drivers, Test Points	1/1/63
2.8.2	Strobe Drivers, Test Points	1/1/63
2.10.1	Bit Driver, Test Points	1/1/63
2.11.1	Sigma Errors	1/1/63

DESCRIPTION

This procedure is used to check the alignment of the clock sample pulses in the 7101 Central Processor Unit (CPU) of the 7030 Data Processing System (DPS), Serial No. 30, 004 and higher. Basically, the test compares various CPU sample pulses for coincidence with a delayed clock reference pulse. The output of the master oscillator is sent through a fixed-value delay line into a 40-foot cable which terminates in a portable terminator box. The output of this box is displayed on the lower beam of a dual-beam oscilloscope, and the sample pulse to be tested (table 2.1.1) is displayed on the upper beam of this oscilloscope. All sample pulses throughout the CPU should be coincident with the delayed clock reference pulse (+ or - 10 nanoseconds) except as noted in table 2.1.1.

EQUIPMENT

Oscilloscope - Tektronix type 551 dual-beam, with type 53/54L, fast-rise, calibrated preamplifiers

Sample Pulse Alignment Tool (P/N 5230780)

PROCEDURAL STEPS

1. Allow warmup period of 30 minutes for CPU and oscilloscope.

2. Set up CPU timing test on 7101 CE console:

   a. Set Load Index (LX) instruction into both half-words of PANEL KEYS.

   b. Set MAINT MOD level switch to DOWN position.

   c. Set RPT INST level switch to DOWN position.

   d. Set TIME CLOCK level switch to DOWN position.

   e. Set IRPT level switch to DOWN position.

   f. Set INH SCAN level switch to DOWN position.

   g. Depress MASTER (Reset) pushbutton.

   h. Depress START (Clock) pushbutton.

   i. Depress START (Program) pushbutton.

3. During latter part of warmup period, check sample pulses at their measurement points for rise time, shape, and voltage level. Open cables and bad card or card socket contacts may affect timing on lines other than those directly involved.

4. After warmup period, compensate oscilloscope probes, using internal oscilloscope calibrator.

5. Remove jumper between pins A and J of card socket 12A1C03, and insert alignment tool drape cable paddle into card socket 12A1C23.

6. Connect lower-beam oscilloscope probe to output of alignment tool. This signal, obtained from a raw clock pulse delayed by a fixed-value delay line (contained in location 12A1C03) and 40 feet of cable, represents the clock reference pulse.

7. Connect upper-beam oscilloscope probe to sample test point to be checked (table 2.1.1). All sample pulses throughout the CPU should be coincident with clock reference pulse (+ or - 10 nanoseconds) except as noted in table 2.1.1.

8. If sample pulse being checked does not coincide with clock reference pulse, change tap point of delay line on load point delay card to correct this condition (table 2.1.1). If sample pulse is not delayed at load point, change tap point of delay line on clock delay card (table 2.1.1).

9. After all points indicated in table 2.1.1 have been checked and corrected, remove reference pulse drape cable paddle from test socket, and replace jumper wire between pins A and J of card socket 12A1C03A.

Date: October 16, 1962

From (Dept/Loc): DP Customer Engineering 900-4
Poughkeepsie, Extension 4242-M

IBM

Subject and/or Reference: Sample Pulse Alignment Tool (P/N 5230780)

To: Mr. S. J. Murray
Customer Engineering
Oakland, California

There is no "standard fixed value" delay because each Stretch machine varies slightly in timing.

You can find this exact delay by measuring the difference between the raw clock output and the driven sample pulses. A standard VB (P/N 371782) capped to this value can then be used with the sample pulse alignment tool for checking pulses.

If we can be of further assistance, please advise.

M. K. Muller
Technical Operations Manager

MKM:jjm

TABLE 2.1.1. CPU SAMPLE TEST POINTS

Sample Test Point		Type Line	Type Pulse	Load Point Delay Card		Clock Delay Card	
Location	Logic			Location	Logic	Location	Logic
11A2F26C	11.12.02.1	-P	ABAB -180	11A2E28	11.12.01.1		
11A2K24F	11.12.02.1	+N	ABAB			12A1C05	11.07.02.1
11A2H21F	11.12.02.1	-P	ABAB	11A2F24 11A2F23	11.12.02.1 11.12.02.1	12A1C05	11.07.02.1
11A2J21B	11.12.02.1	+N	ABAB			12A1C05	11.07.02.1
11A2F27F	11.12.02.1	+N	ABAB -180	11A2E28	11.12.01.1		
11A2G22F	11.12.02.1	+N	ABAB	11A2G26	11.12.02.1		
12A4D24B	11.12.03.1	+N	SABR			12A1C06	11.07.02.1
13A4A09B	27.09.07.1	-P	SAR	16A4H03	28.46.13.1	12A1B11	11.07.02.1
13B3A27B	21.50.01.1	-P	SAC	16A4G11	28.46.12.1	12A1B20	11.07.04.1
13A4E05G	27.09.07.1	+P	DLY'D SAC	17B4G28	28.68.91.1		
14A1J25B	22.09.01.1	-P	SAC	16A3D27	28.46.12.1	12A1B20	11.07.04.1
14A1J27G	22.09.01.1	-P	SABR	16A4G03	28.46.11.1	12A1B07	11.07.02.1
14B1G27B	24.00.07.1	+P	SBC	16A4H08	28.46.14.1	12A1B25	11.07.04.1
14B1H05B	22.09.01.1	-P	SAC	16A3E27	28.46.12.1	12A1B20	11.07.04.1
14B1H03G	22.09.01.1	-P	SABR	16A4G04	28.46.11.1	12A1B07	11.07.02.1
15A3B18C	28.20.25.1	+N	SABR	15B3D22	28.27.71.1	12A1B08	11.07.02.1
15A3A20C	28.20.26.1	+N	SABR	15B3B08	28.27.71.1	12A1B08	11.07.02.1
15A3A21B	28.20.25.1	+N	SAR	15B3B12	28.27.70.1	12A1B12	11.07.02.1
15A3B22B	28.20.26.1	+N	SABR	15B3B11	28.27.70.1	12A1B08	11.07.02.1
15A3A25B	28.20.25.1	+N	SAC	15B3B21	28.27.70.1	12A1B19	11.07.04.1
15A3A16B	28.20.27.1	+N	SBC	15B3B06	28.27.71.1	12A1B24	11.07.04.1
15B3A27B	28.27.70.1	+N	SAC	15B3B24	28.27.70.1	12A1B19	11.07.04.1
15B3A25B	28.27.70.1	+N	SAC	15B3A23	28.27.70.1	12A1B19	11.07.04.1

TABLE 2.1.1. CPU SAMPLE TEST POINTS (cont'd)

Sample Test Point		Type Line	Type Pulse	Load Point Delay Card		Clock Delay Card	
Location	Logic			Location	Logic	Location	Logic
15B3C21B	28.27.71.1	+N	SBC	15B3B18	28.27.71.1	12A1B24	11.07.04.1
15B3C24B	28.27.71.1	+N	SBC	15B3C18	28.27.71.1	12A1B24	11.07.04.1
15B3D27B	28.27.71.1	+N	SABR	15B3C26	28.27.71.1	12A1B08	11.07.02.1
15B3D25C	28.27.70.1	+N	SABR	15B3B25	28.27.70.1	12A1B08	11.07.02.1
15B3A21H	28.27.70.1	+N	SAC +30	15B3D21	28.27.70.1	12A1B19	11.07.04.1
16A3C21B	28.46.12.1	+N	SAC	16A3B27	28.46.12.1	12A1B20	11.07.04.1
16A4D02B	28.46.11.1	+N	SABR	16A4G06	28.46.11.1	12A1B07	11.07.02.1
16A4D04B	28.46.13.1	+N	SAR	16A4G10	28.46.13.1	12A1B11	11.07.02.1
16A4D09B	28.46.15.1	+N	SBR	16A4H10	28.46.15.1	12A1C11	11.07.02.1
16A4D06B	28.46.14.1	+N	SBC	16A4H06	28.46.14.1	12A1B25	11.07.04.1
16A4E03B	28.46.13.1	+N	SAR	16A4H02	28.46.13.1	12A1B11	11.07.02.1
16A4E06B	28.46.14.1	+N	SBC	16A4H07	28.46.14.1	12A1B25	11.07.04.1
16A4E09B	28.46.14.1	+N	SBC	16A4H05	28.46.14.1	12A1B25	11.07.04.1
16A4F11B	28.46.11.1	+N	SAR	16A4G07	28.46.11.1	12A1B07	11.07.02.1
16B4C11F	28.51.21.1	+N	SAR	16A4G08	28.46.13.1	12A1B11	11.07.02.1
16B4C18B	28.51.22.1	+N	SAC	16A3B26	28.46.12.1	12A1B20	11.07.04.1
16B4C17B	28.51.22.1	+N	SBC	16A4H04	28.46.14.1	12A1B25	11.07.04.1
16B4F18F	28.51.24.1	+N	SAR	16A4G09	28.46.13.1	12A1B11	11.07.02.1
17A3B21B	28.68.12.1	+N	SAR	17B4A17	28.68.12.1	12A1C07	11.07.02.1
17A3B19B	28.68.13.1	+N	SBC	17B4A18	28.68.13.1	12A1B27	11.07.04.1
17A3C18B	28.68.15.1	+N	SABR	17B4A25	28.68.15.1	12A1B09	11.07.02.1
17A3C16C	28.68.14.1	+N	SBC	17B4A24	28.68.14.1	12A1B27	11.07.04.1
17A3C21B	28.68.11.1	+N	SAC	17B4A14	28.68.91.1	12A1C21	11.07.04.1
17A3C25B	28.68.11.1	+N	SAC	17B4A13	28.68.91.1	12A1C21	11.07.04.1
17A3D27B	28.68.19.1	+N	SABR	17B4A27	28.68.19.1	12A1B09	11.07.02.1
17B2K08B	28.68.15.1	+N	SABR	17B2K27	28.68.15.1	12A1B09	11.07.02.1
17B2K07B	28.68.12.1	+N	SAR	17B2K19	28.68.12.1	12A1C07	11.07.02.1

TABLE 2.1.1. CPU SAMPLE TEST POINTS (cont'd)

Sample Test Point		Type Line	Type Pulse	Load Point Delay Card		Clock Delay Card	
Location	Logic			Location	Logic	Location	Logic
17B2K03B	28.68.91.1	+N	SAC	17B2K15	28.68.91.1	12A1C21	11.07.04.1
17B2K05B	28.68.91.1	+N	SAC	17B2K16	28.68.91.1	12A1C21	11.07.04.1
17B4A08B	28.68.19.1	+N	SABR	17B4A28	28.68.19.1	12A1B09	11.07.02.1
17B4A07B	28.68.14.1	+N	SBC	17B4A22	28.68.14.1	12A1B27	11.07.04.1
17B4A05B	28.68.13.1	+N	SBC	17B4A21	28.68.13.1	12A1B27	11.07.04.1
18A3H05B	38.71.05.1	+N	SABC	19B3B10	38.71.01.1	12A1B16	11.07.03.1
18A3G26B	38.71.06.1	+N	SABR	19B3D08	38.71.04.1	12A1B10	11.07.02.1
18A3H03B	38.71.05.1	-P	SABC	19B3A06	38.71.01.1	12A1B16	11.07.03.1
18B1K26B	38.71.08.1	+N	SABC	19B3E05	38.71.01.1	12A1B16	11.07.03.1
18A4E22B	38.71.06.1	-P	SABR	19B3D07	38.71.04.1	12A1B10	11.07.02.1
18B4A02B	38.71.07.1	+N	SABC	19B3E04	38.71.01.1	12A1B16	11.07.03.1
18B4A08B	38.71.13.1	+N	SBC	18B4B07	38.71.13.1	12A1C14	11.07.04.1
18B4A12B	38.71.11.1	+N	SABR	19B3A08	38.71.04.1	12A1B10	11.07.02.1
18B4A15B	38.71.11.1	+N	SAC	19B4B09	38.71.11.1	12A1C22	11.07.04.1
18B4A18B	38.71.09.1	+N	SABC	19B3A07	38.71.03.1	12A1B16	11.07.03.1
18B2G08B	38.71.10.1	+N	SABC	19B3B09	38.71.01.1	12A1B16	11.07.03.1
18B4C04C	38.71.10.1	+N	SABC	19B3F04	38.71.02.1	12A1B16	11.07.03.1
19A2D03B	31.30.03.1	-P	SABR	19B3A12	38.71.04.1	12A1B10	11.07.02.1
19A2F08B	31.30.02.1	-P	SABC	19B3B07	38.71.01.1	12A1B16	11.07.03.1
19B1J22B	38.71.02.1	+N	SABC	19B3B15	38.71.02.1	12A1B16	11.07.03.1
19B1K03B	38.71.02.1	+N	SABC	19B3D03	38.71.02.1	12A1B16	11.07.03.1
19B1D13C	38.71.13.1	+N	SABR	19B1D14	38.71.13.1	12A1B10	11.07.02.1
19B2F17B	38.71.02.1	+N	SABC	19B3B14	38.71.02.1	12A1B16	11.07.03.1
19B2J22H	38.71.13.1	+N	SAC	18B4A07	38.71.11.1	12A1C22	11.07.04.1
19B2K04B	38.71.04.1	+N	SABR	19B3A15	38.71.04.1	12A1B10	11.07.02.1
19B4A08C	38.71.03.1	+N	SABR	19B3B12	38.71.03.1	12A1B16	11.07.03.1
19B4A26C	38.71.03.1	+N	SABC	19B3B11	38.71.03.1	12A1B16	11.07.03.1
19B4C23H	38.71.13.1	+N	SBR			12A1B26	11.07.04.1

TABLE 2.1.1. CPU SAMPLE TEST POINTS (cont'd)

Sample Test Point		Type Line	Type Pulse	Load Point Delay Card		Clock Delay Card	
Location	Logic			Location	Logic	Location	Logic
20A2E17C	34.08.02.1	+N	SABC	19B3B06	38.71.01.1	12A1B16	11.07.03.1
20B2G25B	31.30.01.1	-P	SABC	19B3B08	38.71.01.1	12A1B16	11.07.03.1
20B2G25G	31.30.01.1	-P	SABR	19B3A13	38.71.04.1	12A1B10	11.07.02.1
21B2J12G	53.06.40.1	-P	A-A-A	21B2H12	53.06.40.1	12A1C10	11.07.04.1
21B2E13H	53.06.40.1	-P	A-A-A	21B2J07	53.06.40.1	12A1C10	11.07.04.1
21B2F05G	53.06.40.1	+N	A-A-A	21B2J08	53.06.40.1	12A1C10	11.07.04.1
21B4J08B	53.06.40.1	-P	A-A-A	21B4J10	53.06.40.1	12A1C10	11.07.04.1
21B2J12A	54.48.02.1	-P	ABAB			12A1C19	11.07.03.1
22A4C07H	56.60.01.1	-N	EARLY A			12A1B22	11.07.04.1
22A2J16B	56.61.01.1	+N	B-A TIME			12A1C27	11.07.04.1
22A4A08B	56.62.01.1	+N	A-A-A			12A1C22	11.07.04.1
22B4F22B	54.26.01.1	-P	ABAB	25B1C27	61.04.90.1	12A1B18	11.07.03.1
23A2K04A	51.02.01.1	+P	ABAB			12A1C18	11.07.03.1
23B1J09B	51.52.03.1	+N	ABAB	23B1J06	51.55.10.1	12A1B17	11.07.03.1
23B2K13B	51.52.01.1	+N	ABAB	23B2J12	51.55.10.1	12A1B17	11.07.03.1
23B2J02B	51.55.01.1	+N	ABAB	23B2J03	51.55.10.1	12A1B17	11.07.03.1
23A4D05H	51.56.20.1	-P	A-A-A			12A1C15	11.07.04.1
23A2K09B	59.95.01.1	+N	ABAB	23A2K11	59.95.01.1	12A1C18	11.07.03.1
23A4E27F	59.95.01.1	+N	ABAB	23A4G16	59.95.01.1	12A1E10	11.07.02.1
24A2F04C	59.11.01.1	-P	ABAB	25B1B14	61.04.88.1	12A1B18	11.07.03.1
24A4B20F	48.10.03.1	+N	ABAB	24A1F22	48.10.03.1	12A1B18	11.07.03.1
24A1E25B	48.10.05.1	+N	ABAB	24A1E23	48.10.05.1	12A1B18	11.07.03.1
24A1F25B	48.10.05.1	+N	ABAB	24A1F23	48.10.05.1	12A1B18	11.07.03.1
24A1B13C	48.10.05.1	-N	ABAB	24A1B14	48.10.05.1	12A1B18	11.07.03.1

TABLE 2.1.1. CPU SAMPLE TEST POINTS (cont'd)

Sample Test Point		Type Line	Type Pulse	Load Point Delay Card		Clock Delay Card	
Location	Logic			Location	Logic	Location	Logic
25A4C15B	61.04.04.1	+N	ABAB	25B1C19	61.04.91.1	12A1B18	11.07.03.1
25A2G12B	61.04.02.1	+N	ABAB	25B1C21	61.04.91.1	12A1B18	11.07.03.1
25A3G15B	61.04.03.1	+N	ABAB	25B1C20	61.04.91.1	12A1B18	11.07.03.1
25A3J04C	61.02.73.1	+N	ABAB	25B1D21	61.04.88.1	12A1B18	11.07.03.1
25B1J13B	61.04.05.1	+N	ABAB	25B1D20	61.04.88.1	12A1B18	11.07.03.1
25B1K13B	61.04.05.1	+N	ABAB	25B1D27	61.04.91.1	12A1B18	11.07.03.1
25B3B21F	37.81.02.1	-P	ABAB	25B3B18	37.81.02.1	12A1F08	11.07.02.1
25A1J13B	61.04.01.1	+N	ABAB	25B1C22	61.04.91.1	12A1B18	11.07.03.1
25A3J15G	61.01.78.1	+N	EARLY SAMPLE (60)	25B1D26	61.04.91.1	12A1B18	11.07.03.1
25A3J25H	61.02.50.1	+P	NOT CLOCK	25B1B24	61.04.91.1	12A1B18	11.07.03.1
26A1J26D	61.90.11.1	+N	ABAB	25B1B25	61.04.90.1	12A1B18	11.07.03.1
26A3J27D	61.90.11.1	+N	ABAB	25B1C25	61.04.90.1	12A1B18	11.07.03.1
26B1J26D	61.90.12.1	+N	ABAB	25B1C24	61.04.90.1	12A1B18	11.07.03.1
26B4F22D	61.90.12.1	+N	ABAB	25B1C23	61.04.90.1	12A1B18	11.07.03.1
27A4B17B	61.91.21.1	+N	ABAB	25B1C26	61.04.90.1	12A1B18	11.07.03.1
27B1D20C	61.81.66.1	+N	ABAB	25B1B26	61.04.90.1	12A1B18	11.07.03.1
28B1G23D	66.21.01.1	+N	MPY AB	25B1D25	61.04.91.1	12A1B18	11.07.03.1
28B3D23D	66.21.01.1	+N	MPY AB	25B1D24	61.04.91.1	12A1B18	11.07.03.1
28A4J17B	68.11.01.1	+N	MPY AB	25B1B27	61.04.90.1	12A1B18	11.07.03.1
28B2D07B	28.64.05.1	+N	SAC	17B2K21	28.68.91.1	12A1C21	11.07.04.1
28B2D06F	28.64.04.1	+N	SBC	17B2K24	28.68.13.1	12A1B27	11.07.04.1
28B2F04F	28.64.05.1	+N	SAR	17B2K18	28.68.12.1	12A1C07	11.07.02.1

Note: This table is for CPU 7101, Serial No. 30,004 and higher.

DESCRIPTION

This procedure is performed to check the air filters in the specified CPU frames for dust, dirt, and damage.

PROCEDURAL STEPS

1. Visually check air filters in the CPU frames specified by the PM Task Card.

2. Remove dirty or damaged filters by unscrewing five filter retaining plate screws on the blower assembly. Vacuum-clean salvageable filters, and replace damaged filters (P/N 5203249).

3. Install filters, with the arrow on filter pointing toward blower assembly. Replace filter retaining plate and screws.

DESCRIPTION

This procedure is performed to check the fans in gates B2 through B8 and A7 of the 7101 CE console.

PROCEDURAL STEPS

1. Open gates and visually check that fans are operating.
2. Check that the screen covering the fan is not pushed in toward the fan blades. If it is, straighten it so that fan blades have maximum clearance.
3. If a fan does not operate properly, turn off power to fan.
   a. If assembly is old type (fan mounted inside plenum) proceed to step 4.
   b. If assembly is new type (fan mounted outside of plenum) proceed to step 7.
4. Disconnect power plug to fan.
5. Remove two bolts holding assembly to frame.
6. Install new assembly (P/N 597152). Secure with two bolts to frame. Proceed to step 12.
7. Disconnect power plug to fan.
8. Remove four screws holding fan to assembly.
9. Remove fan guard assembly from old fan by removing four bolts holding guard to fan.
10. Install fan guard assembly on new fan (P/N 597300) with four bolts.
11. Secure fan to assembly with four screws.
12. Connect power plug and turn on power to fan.

DESCRIPTION

This procedure is performed to check the adjustment and condition of the gate latches and slides and to lubricate the gate slides.

PROCEDURAL STEPS

1. Check that the gates slide without binding or sticking. Check that the gate casters do not touch the floor when the gates are travelling on the tower caster.
2. Lubricate the slides with IBM # 6 oil. Use the oil sparingly.
3. Check that the latches operate properly.
4. Check the unit for overall cleanliness.
5. For mechanical adjustments refer to General Reference Manual (01), page 7-21, mechanical adjustments of a 20-inch frame.

DESCRIPTION

This procedure checks the ability of the index core storage section to write and read 1's and 0's in all bit positions from the Sigma console.

PROCEDURAL STEPS

1. Initial Setup

   a. Maintenance mode active.

   b. Time clock disabled.

   c. All other switches off or neutral.

2. Write 1's in all indexes in all bits.

   a. Address keys = 20_8.

   b. Panel key set 01 and 10 to UP.

   c. Master Reset.

   d. Start Clock.

   e. Store. NOTE: W register should now equal 20_8.

   f. Consecutive Store 15 times. NOTE: W register should step from 20_8 to 37_8.

3. Read 1's from all indexes.

   a. Address keys = 20_8.

   b. Master Reset.

   c. Start Clock.

   d. Display.

Note

The W register should now = 20_8. Index Register 0 is now displayed in both the X register and 1Y register. All bits should be 1's. Record failures.

   e. Consecutive Display 15 times.

Note

The W register should step from 20_8 to 37_8. The index registers are displayed in both the X register and 1Y register. The 2Y register contains the previous display. All bits should be 1's. Record the failures.

f. If any errors occur refer to the flow chart, Figure 2.5.1, and Step 8 for isolation of the error.

4. Write 0's (data) in all indexes, the same as write 1's (Step 2) except that:

   Step 2b = Panel key set 01 and 10 DOWN.

5. Read 0's (data) in all indexes, the same as read 1's (Step 3) except that:

   a. All data bits should be 0's.

   b. For Step 3f refer instead to the flow chart, Figure 2.5.2, and Step 8 for isolation of the error.

6. Write 0 parities in all indexes, the same as write 1's (Step 2) except that:

   a. Step 2b for Panel key set 01 and 10 = NEUTRAL.

   b. Step 2b for Panel keys 17, 23, 27, 31, 49, 55, 59, 63, = SET.

7. Read 0 parities from all indexes, the same as read 1's (Step 3) except that:

   a. All parity bits should be 0.

   b. For Step 3f refer instead to Figure 2.5.2 and Step 8 for errors.

IF no errors have occurred above in Steps 1 through 7, proceed to Step 9. The following Step 8 is used in conjunction with the flow charts for scoping the index core storage circuits.

8. Cycling on single index for scoping.

   a. Perform the initial setup as in Step 1.

   b. Set the panel key set 01 and 10 UP or DOWN when scoping for dropped or picked bits respectively.

Note

If a picked parity bit is being scoped, set the panel key set 01 and 10 to the neutral position and enter the pattern in the panel keys as in Step 6.

c. Set the address keys to 40_8.

d. Store (Master reset, start clock and store, W register = 20).

e. Set the panel key set 01 and 10 to the neutral position and set the panel keys to:

0-31	LX $X?		Bits 12 and 27 SET, 19-22 = IX
32-63	SX $X?	41	Bits 44, 49, 55, and 59 SET Bits 51-54 = IX

f. Set repeat instruction active.

g. Master reset.

h. Start clock.

i. Enter the instruction.

j. Program start.

Note

The "run" indicator should now be on and the "inactive" indicator off. Scope the circuits indicated as failing in the flow charts. Scope points are listed in Table 2.5.2. The oscilloscope set-up, waveforms, and timing are shown in Figures 2.5.3 and 2.5.4.

9. Time clock check

a. Set the maintenance mode active.

b. Set the time clock disable inactive.

c. Set the time clock test active.

d. Master reset.

e. Start clock.

Note

The interval timer and time clock should now be visible in the X register. If errors occur, look for erratic stepping of the X register. Read, write, and clear oscilloscope points are on Table 2.5.2.

TABLE 2.5.1. SA GROUPS

Bit	14B4A07 & A08		Bit	14B4A07 & A09		Bit	14B4A06 & C10	
	Group 3	Group 4		Group 5	Group 6		Group 1	Group 2
0	X		24	X		46	X	
1	X		25	X		47	X	
2	X		26		X	48		X
3	X		27		X	49		X
4		X	P24-27	X		P32-49	X	
5		X	28	X		P46-49		X
6	X		29		X	50	X	
7	X		30		X	51		X
8		X	31	X		52		X
9		X	P28-31	X		53	X	
10	X		32		X	54	X	
11	X		33		X	55		X
12		X	34	X		P50-55		X
13		X	35	X		56	X	
14	X		36		X	57	X	
15	X		37		X	58		X
16		X	38	X		59		X
17		X	39	X		P56-59	X	
P0-17	X		40		X	60	X	
18	X		41		X	61		X
19		X	42	X		62		X
20		X	43	X		63	X	
21	X		44		X	P60-63	X	
22	X		45		X			
23		X						
P18-23		X						

TABLE 2.5.2. INDEX CORE STORAGE ARRAY TEST POINTS

Bit	Inhibit Output at H	Sense	Bit	Inhibit Output at H	Sense
0	14B2 D03	14B4A10Y	33	14B2 E15	14B4C19V
1	" E03	" A10V	34	" F15	" A20Y
2	" F03	" A11Y	35	" D16	" A20V
3	" D04	" A11V	36	" E16	" C20Y
4	" E04	" C11Y	37	" F16	" C20V
5	" F04	" C11V	38	" D17	" A21Y
6	" D05	" A12Y	39	" E17	" A21V
7	" E05	" A12V	40	" F17	" C21Y
8	" F05	" C12Y	41	" D18	" C21V
9	" D06	" C12V	42	" E18	" A22Y
10	" E06	" A13Y	43	" F18	" A22V
11	" F06	" A13V	44	" D19	" C22Y
12	" D07	" C13Y	45	" E19	" C22V
13	" E07	" C13V	46	" F19	" A23Y
14	" F07	" A14Y	47	" D20	" A23V
15	" D08	" A14V	48	" E20	" C23Y
16	" E08	" C14Y	49	" F20	" C23V
17	" F08	" C14V	32-49	" D21	" A24Y
0-17	" D09	" A15Y	50	" E21	" A24V
18	" E09	" A15V	51	" F21	" C24Y
19	" F09	" C15Y	52	" D22	" C24V
20	" D10	" C15V	53	" E22	" A25Y
21	" E10	" A16Y	54	" F22	" A25V
22	" F10	" A16V	55	" D23	" C25Y
23	" D11	" C16Y	50-55	" E23	" C25V
18-23	" E11	" C16V	56	" F23	" A26Y
24	" F11	" A17Y	57	" D24	" A26V
25	" D12	" A17V	58	" E24	" C26Y
26	" E12	" C17Y	59	" F24	" C26V
27	" F12	" C17V	56-59	" D25	" A27Y
24-27	" D13	" A18Y	60	" E25	" A27V
28	" E13	" A18V	61	" F25	" C27Y

	Inputs for Timing
CLEAR	14B1 G18E
WRITE	14B1 G19E
READ	14B1 G20E
INHIBIT	14B1 E27E
INHIBIT	14B1 F27E
STROBE	14B4 C09B

Drivers 14B1

Output at H

Address	Read	Write	Clear
TC	H 11	J 11	K 11
0	H 12	J 12	K 12
1	H 13	J 13	K 13
2	H 14	J 14	K 14
3	H 15	J 15	K 15
4	H 16	J 16	K 16
5	H 17	J 17	K 17
6	H 18	J 18	K 18
7	H 19	J 19	K 19
8	H 20	J 20	K 20
9	H 21	J 21	K 21
10	H 22	J 22	K 22
11	H 23	J 23	K 23
12	H 24	J 24	K 24
13	H 25	J 25	K 25
14	H 26	J 26	K 26
15	H 27	J 27	K 27

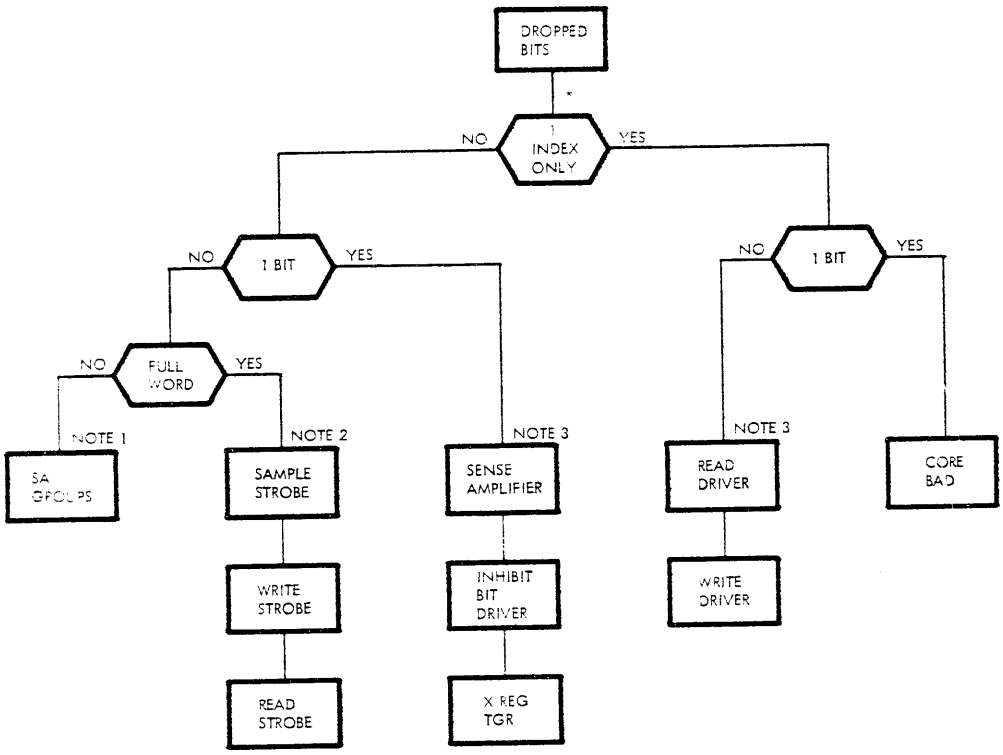
Sense

Output at Y = Input at A

Output at V = Input at G

TABLE 2.5.2. INDEX CORE STORAGE ARRAY TEST POINTS (cont'd)

Bit	Inhibit Output at H	Sense	Bit	Inhibit Output at H	Sense	Inputs for Timing
29	" F13	" C18Y	62	" D26	" C27V	
30	" D14	" C18V	63	" E26	" A28Y	
31	" E14	" A19Y	60-63	" F26	" A28V	
28-31	" F14	" A19V	46-49	" F27	" C28Y	
32	" D15	" C19Y				



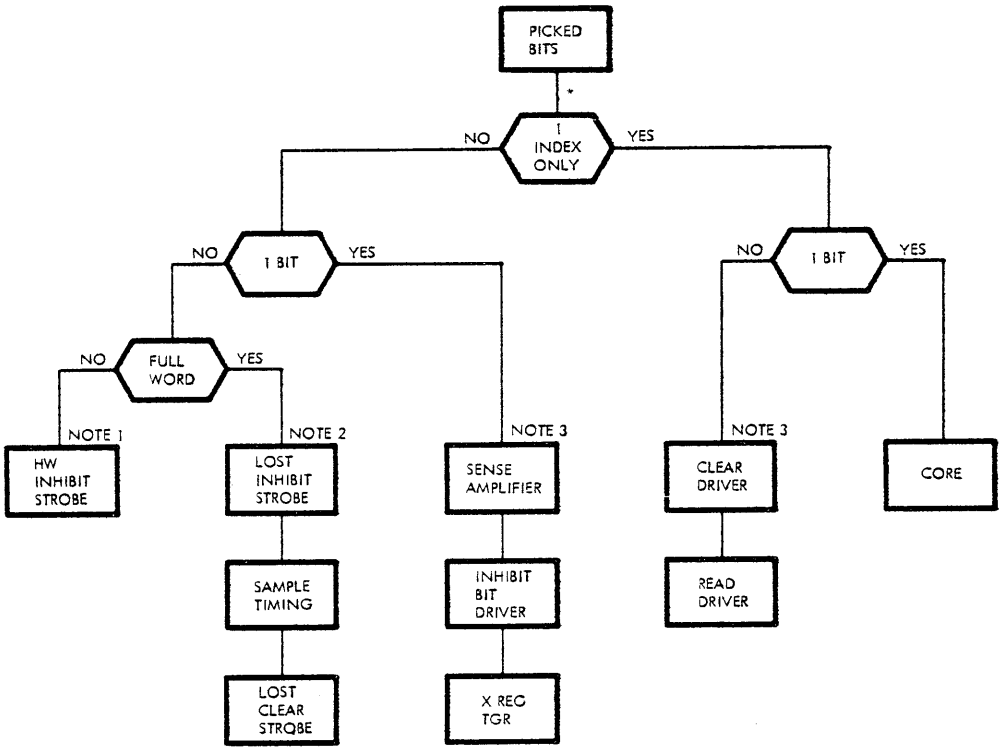
*SEE STEP 8 FOR OSCILLOSCOPE PROCEDURE WHEN EXITING.

NOTE 1 - TABLE 2.5.1 LISTS THE BITS IN EACH SA STROBE GROUP.

NOTE 2 - FIGURE 2.5.3 CONTAINS THE SIMPLIFIED LOGIC FOR THIS AREA.

NOTE 3 - TABLE 2.5.2 LISTS THE OSCILLOSCOPE POINTS FOR THESE BOXES.

FIGURE 2.5.1. DROPPED BITS, FLOW CHART



*SEE STEP 8 FOR OSCILLOSCOPE PROCEDURE WHEN EXITING.

NOTE 1 - LHW = 14B1E26, Z7 RHW = 14B1E26, F27

NOTE 2 - FIGURE 2.5.3 CONTAINS THE SIMPLIFIED LOGIC FOR THIS AREA.

NOTE 3 - TABLE 2.5.2 LISTS THE OSCILLOSCOPE POINTS FOR THESE BLOCKS.

FIGURE 2.5.2. PICKED BITS, FLOW CHART

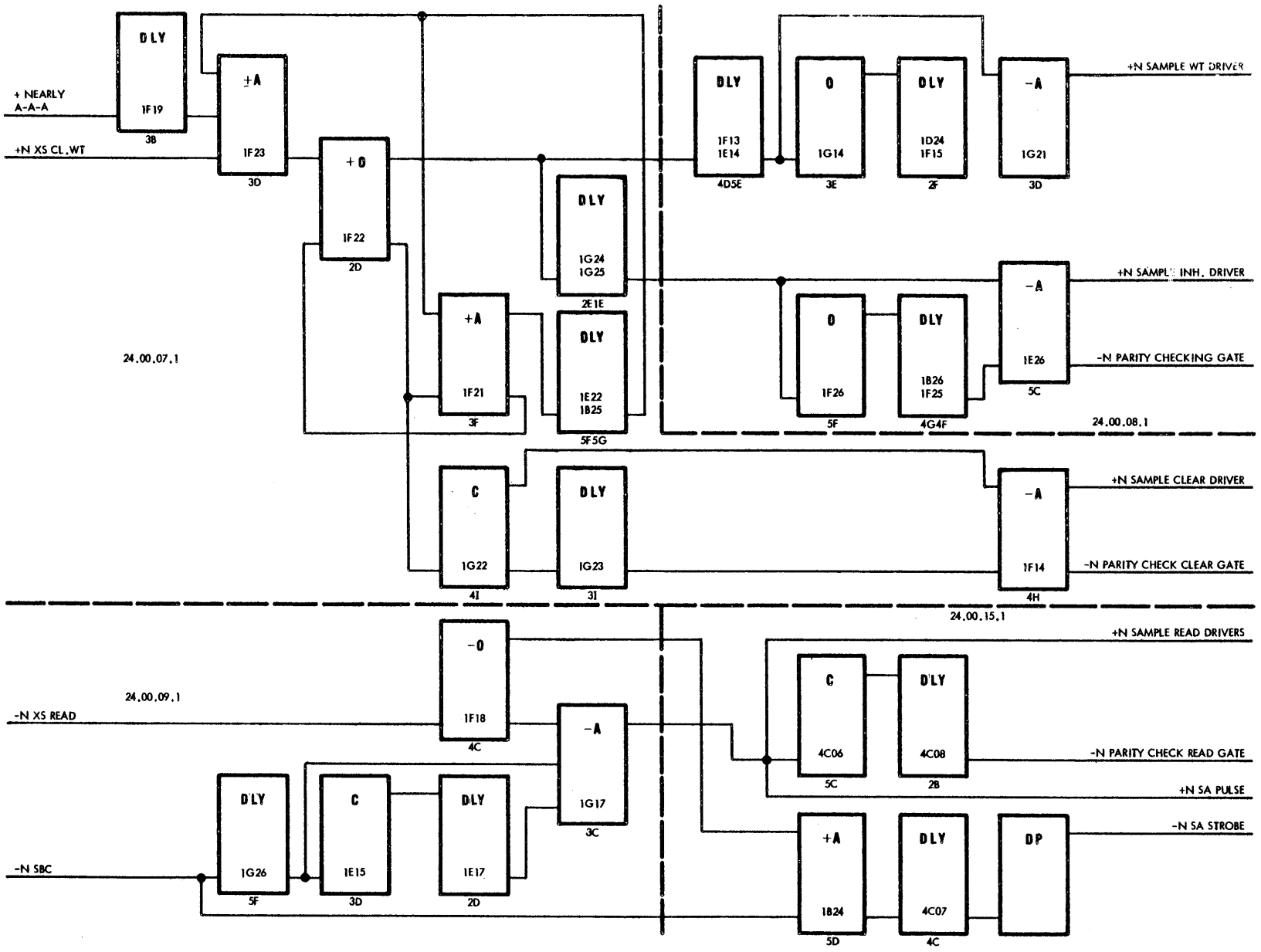


FIGURE 2.5.3 INDEX CORE STORAGE, SIMPLIFIED LOGIC

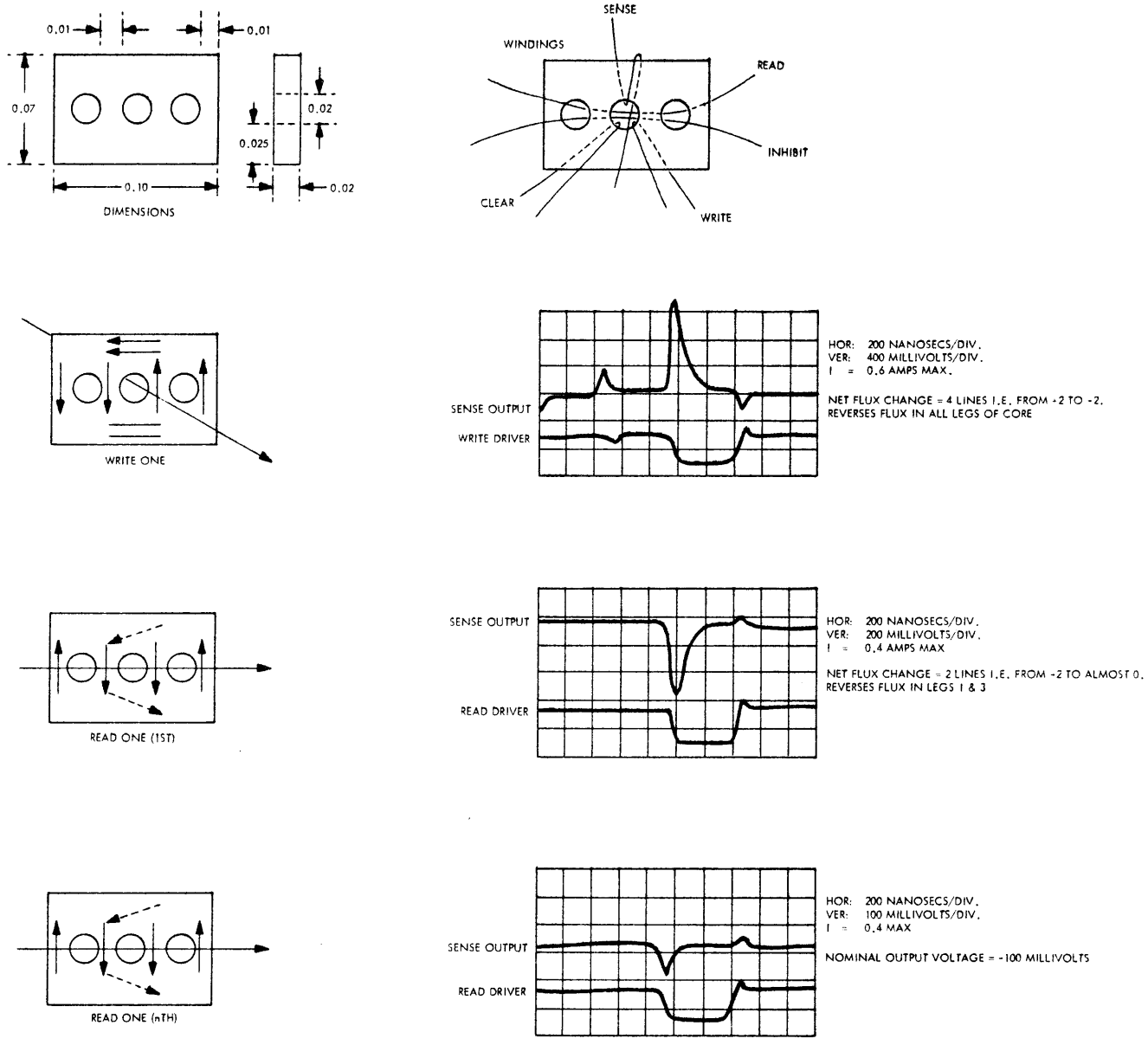
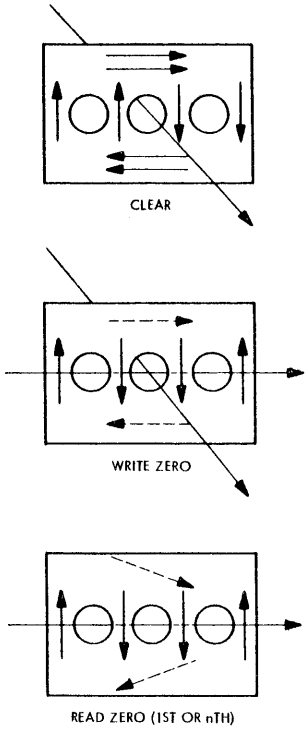
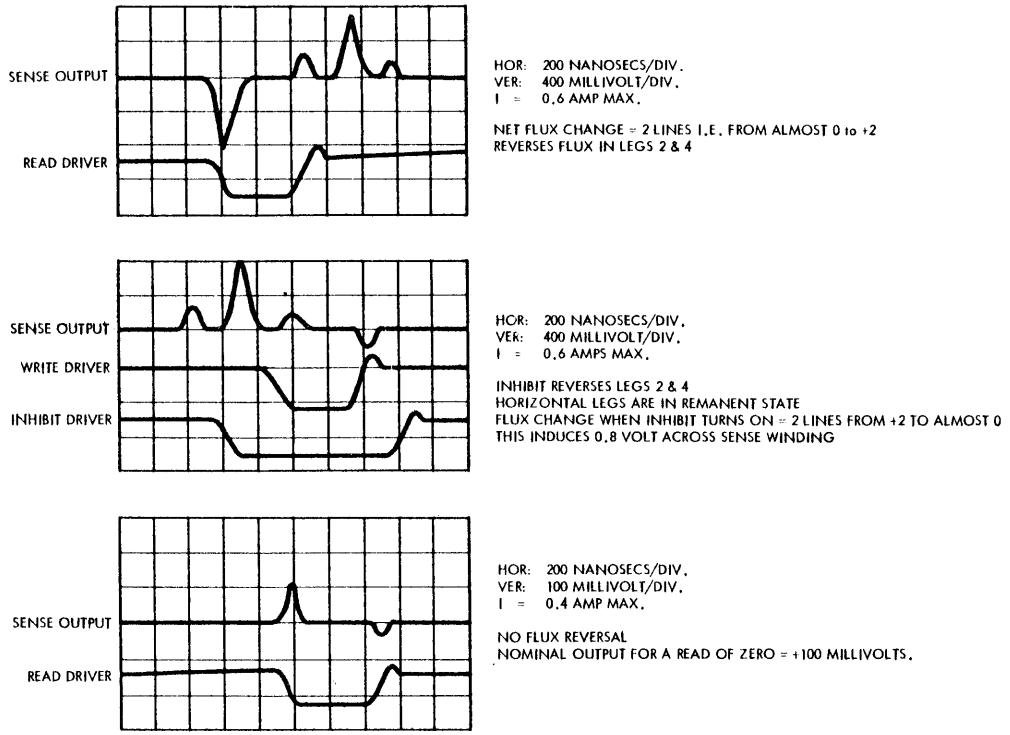


FIGURE 2.5.4. INDEX CORE STORAGE, WAVEFORMS





OPERATION	FLUX
CLEAR	
INHIBIT	NOT APPLICABLE
WRITE	
READ	
READ	

ONE

OPERATION	FLUX
CLEAR	
INHIBIT	
WRITE	
READ	
READ	

ZERO

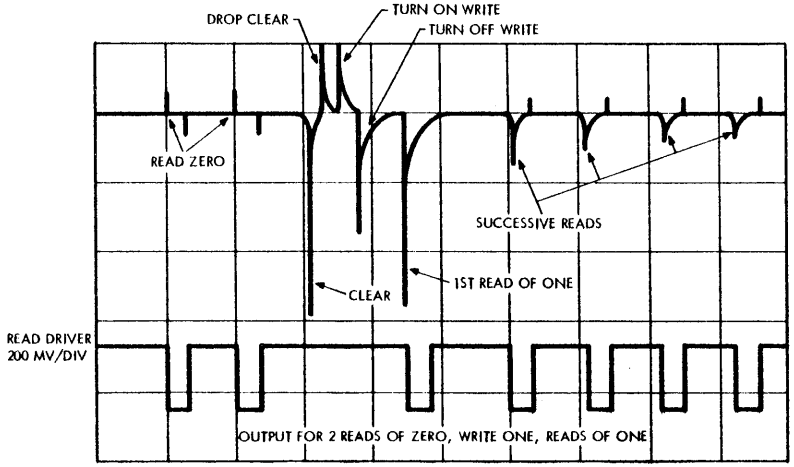


FIGURE 2.5.5 INDEX CORE STORAGE, WAVEFORMS

DESCRIPTION

The Index Tunnel Diode Storage Tuning program is executed to check the reliability of the index tunnel diode storage registers. This program applies to systems with serial numbers of 30,006 and 30,008.

REQUIREMENTS

Index Tunnel Diode Tuning Tape (Two Programs, XTDT1 and XTDT2)

Index Tunnel Diode Storage Unit, 7101 Instruction Unit IBM CEIM, Form R23-9916.

PROCEDURAL STEPS

1. Load XTDT1 tuning tape to obtain a typewriter printout:

   a. Make tape ready.

   b. Execute IPL (initial program load) and channel signal.

2. With XTDT1 loaded, proceed as follows to load XTDT2:

   a. Set maintenance key 31 for program operating procedure printout on the printer.

   b. Execute IPL and channel signal.

3. Follow instructions printed on printer, and execute program with all options and all tests.

4. If this program picks or drops a bit in the tested index register, refer to the Corrective Procedures section of this manual.

DESCRIPTION

This procedure describes the tuning of the turn-on time for the word drivers.

REQUIREMENTS

Vacuum Tube Voltmeter (P/N 5231703)

Oscilloscope, Tektronix 555 (P/N 523004)

Preamplifier Oscilloscope, Sampling Tektronix type N (P/N 5231736)

Probe, Oscilloscope, Tektronix P6025 (P/N 5231737)

Preamplifier Type B (P/N 460998)

Preamplifier Type CA (P/N 460999)

PROCEDURAL STEPS

1. Turn off d-c power before removing cards. Remove word driver cards from panel before adjusting their potentiometers.

2. Two potentiometers are on the card. The 100-ohm potentiometer, for the amplitude adjustment, should not be disturbed. The 1K potentiometer adjusts the turn-on time for the word driver and should be adjusted.

3. Maintain following timing relationships:

   a. Word-driver pulse sync on 14B1G17A.

   b. Use 2-nsec/cm time base and 10v/cm for scoping turn-on time. Establish ground reference by scoping a ground pin, and measure turn-on time as stated below.

   c. Load Store Index instruction for word to be checked.

   d. Scope at output pin of word driver to be checked (table 2.7.1).

   e. Word pulse 180-nsec duration +20 nsec measured at 50 percent point of the output voltage of the word driver. Top and bottom word-driver timing pulses should be skewed by 50 nsec. (See fig. 2.8.1, timings 3, 4, and 5.)

4. Word pulse as described in 3,e, should have an operational turn-on time of 10.5 nsec ± 10.0 nsec from +26v level to ground level with clamp voltage set at -3.2v. Tune word driver to a tolerance of ±0.25 nsec (i.e., 10.5 ± 0.25 nsec). (See fig. 2.7.1.)

TABLE 2.7.1. WORD DRIVER, TEST POINTS

Word Driver Input				Word Driver Output	
Word	Sample Word Driver	Address Sel.	Clamp Voltage	Array Card 1 Bits 0-32	Array Card 2 Bits 33-P46-49
XTC	14B2C11C	14B2C11E	14B2C11G	14B2C11H	14B2C11Z
0	C12D	C12E	C12G	C12H	C12Z
1	C13C	C13E	C13G	C13H	C13Z
2	C14D	C14E	C14G	C14H	C14Z
3	C15C	C15E	C15G	C15H	C15Z
4	C16D	C16E	C16G	C16H	C16Z
5	C17C	C17E	C17G	C17H	C17Z
6	C18D	C18E	C18G	C18H	C18Z
7	C19C	C19E	C19G	C19H	C19Z
8	C20D	C20E	C20G	C20H	C20Z
9	C21C	C21E	C21G	C21H	C21Z
10	C22D	C22E	C22G	C22H	C22Z
11	C23C	C23E	C23G	C23H	C23Z
12	C24D	C24E	C24G	C24H	C24Z
13	C25C	C25E	C25G	C25H	C25Z
14	14B2 C26D	14B2C26E	14B2C26G	14B2C26H	14B2C26Z
15	14B2C27C	14B2C27E	14B2C27G	14B2C27H	14B2C27Z

*The clamp circuit test point output voltage is found at test point output 14B2C28A.

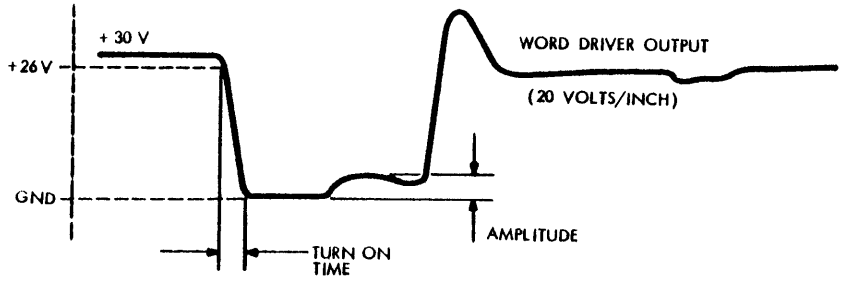


FIGURE 2.7.1. WORD DRIVER OUTPUT WAVESHAPE

DESCRIPTION

This procedure checks the latch and strobe driver timings.

REQUIREMENTS

Oscilloscope, Tektronix Type 555 (P/N 523004)

Preamplifier type B (P/N 460998)

Preamplifier type CA (P/N 460999)

PROCEDURAL STEPS

1. For latch or strobe pulse, sync on 14B1B14H.

2. Scope at pin E, F, or G of latch or strobe cards. See table 2.8.1 or 2.8.2 for pin locations.

3. Maintain following timing relationships:

   a. Word pulse 180-nsec duration ±20 nsec measured at 50 percent point of word-driver output voltage.

   b. Latch-driver pulse must be at the -1v level or more negative 80 nsec minimum prior to turn-off of latest word pulse as described in 3, a, and must extend 20 nsec or more beyond the +30v level of rise of latest word pulse turn-off (fig. 2.8.1, timing 7).

   c. Strobe pulse must be at -1v level or more negative at 50 percent point of turn-on of word pulse and must remain at this level or more negative for at least 5 nsec after latch timing pulse has reached -1v or more negative level (fig. 2.8.1 , timings 3 and 6).

TABLE 2.8.1. LATCH DRIVERS, TEST POINTS

Latch Sample No.	Input	Output	
	Location	Latch No.	Location
(1)	14B2F13A	1	14B2F13E
		2	F13F
		3	F13G
(2)	14B2H13A	4	14B2H13E
		5	H13F
		6	H13G
(3)	14B2K13A	7	14B2K13E
		8	K13F
		9	K13G
(4)	14B2K25A	10	14B2K25E
		11	K25F
		12	K25G
(5)	14B2H25A	13	14B2H25E
		14	H25F
		15	H25G
(6)	14B2F25A	16	14B2F25E
		17	F25F
		18	F25G

*The clamp circuit test point output voltage is found at test point output 14B2C28A.

TABLE 2.8.2. STROBE DRIVERS, TEST POINTS

Input		Output	
Strobe No.	Location	Strobe Group No.	Location
(1)	14B2E13A	1	14B2E13E
		2	E13F
		3	E13G
(2)	14B2G13A	4	14B2G13E
		5	G13F
		6	G13G

TABLE 2.8.2. STROBE DRIVERS TEST POINTS (cont'd)

Input		Output	
Strobe No.	Location	Strobe Group No.	Location
(3)	14B2J13A	7	14B2J13E
		8	J13F
		9	J13G
(4)	14B2J25A	10	14B2J25E
		11	J25F
		12	J25G
(5)	14B2G25A	13	14B2G25E
		14	G25F
		15	G25G
(6)	14B2E25A	16	14B2E25E
		17	E25F
		18	E25G

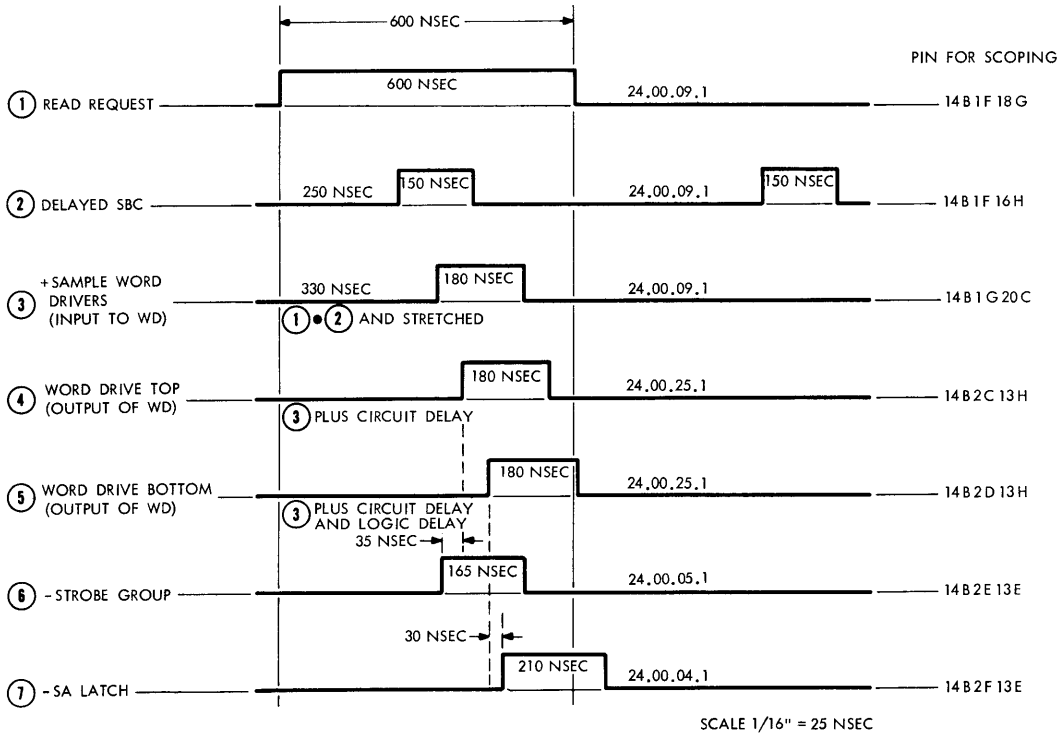


FIGURE 2.8.1. EXAMPLE OF FETCH TIMING FOR INDEX TUNNEL DIODE STORAGE

DESCRIPTION

This check is performed to determine whether the supply voltage clamp is functioning.

REQUIREMENTS

Vacuum tube voltmeter (P/N 5231703)

PROCEDURAL STEPS

Using a vacuum tube voltmeter (P/N 5231703), check output voltage at card location 14B2C28A. The clamp-difference voltage is determined with respect to -12vdc (i.e., if the output of the clamp card is -8.8vdc with respect to ground, then the clamp-difference voltage with respect to -12vdc is -3.2vdc).

DESCRIPTION

This procedure checks the timing of the data-in pulse of the index tunnel diode storage register.

REQUIREMENTS

Oscilloscope, Tektronix Type 555

PROCEDURAL STEPS

1. Using scope, check data-in bit driver output (table 2.10.1). The data-in bit driver should turn on within 30 nsec of the latch output pulse and remain on for the duration of the latch output pulse (fig. 2.10.1, timings 17 and 18).

2. Location of array card inputs.(fig. 2.10.2).

TABLE 2.10.1. BIT DRIVER, TEST POINTS

Bits	Bit Line Output or Input to SA-BD	Bits	Bit Line Output or Input to SA-BD
0	14B2E9A	15	14B2G10S
1	E9S	16	G11A
2	E10A	17	G11S
3	E10S	P0-17	G12A
4	E11A	18	G12S
5	E11S	19	G14A
6	E12A	20	G14S
7	E12S	21	G15A
8	E14A	22	G15S
9	E14S	23	G16A
10	E15A	P18-23	G16S
11	E15S	24	J10A
12	E16A	25	J10S
13	E16S	26	J11A
14	14B2G10A	27	14B2J11S

TABLE 2.10.1. BIT DRIVER, TEST POINTS (cont'd)

Bits	Bit Line Output or Input to SA-BD	Bits	Bit Line Output or Input to SA-BD
P24-27	14B2J12A	47	14B2G22S
28	J12S	48	G23A
29	J14A	49	G23S
30	J14S	P32-49	G24A
31	J15A	50	G24S
P28-31	J15S	51	G26A
32	J16A	52	G26S
33	J16S	53	G27A
34	J22A	54	G27S
35	J22S	55	G28A
36	J23A	P50-55	G28S
37	J23S	56	E22A
38	J24A	57	E22S
39	J24S	58	E23A
40	J26A	59	E23S
41	J26S	P56-59	E24A
42	J27A	60	E24S
43	J27S	61	E26A
44	J28A	62	E26S
45	J28S	63	E27A
46	14B2G22A	P60-63	E27S
		P46-49	14B2E28A

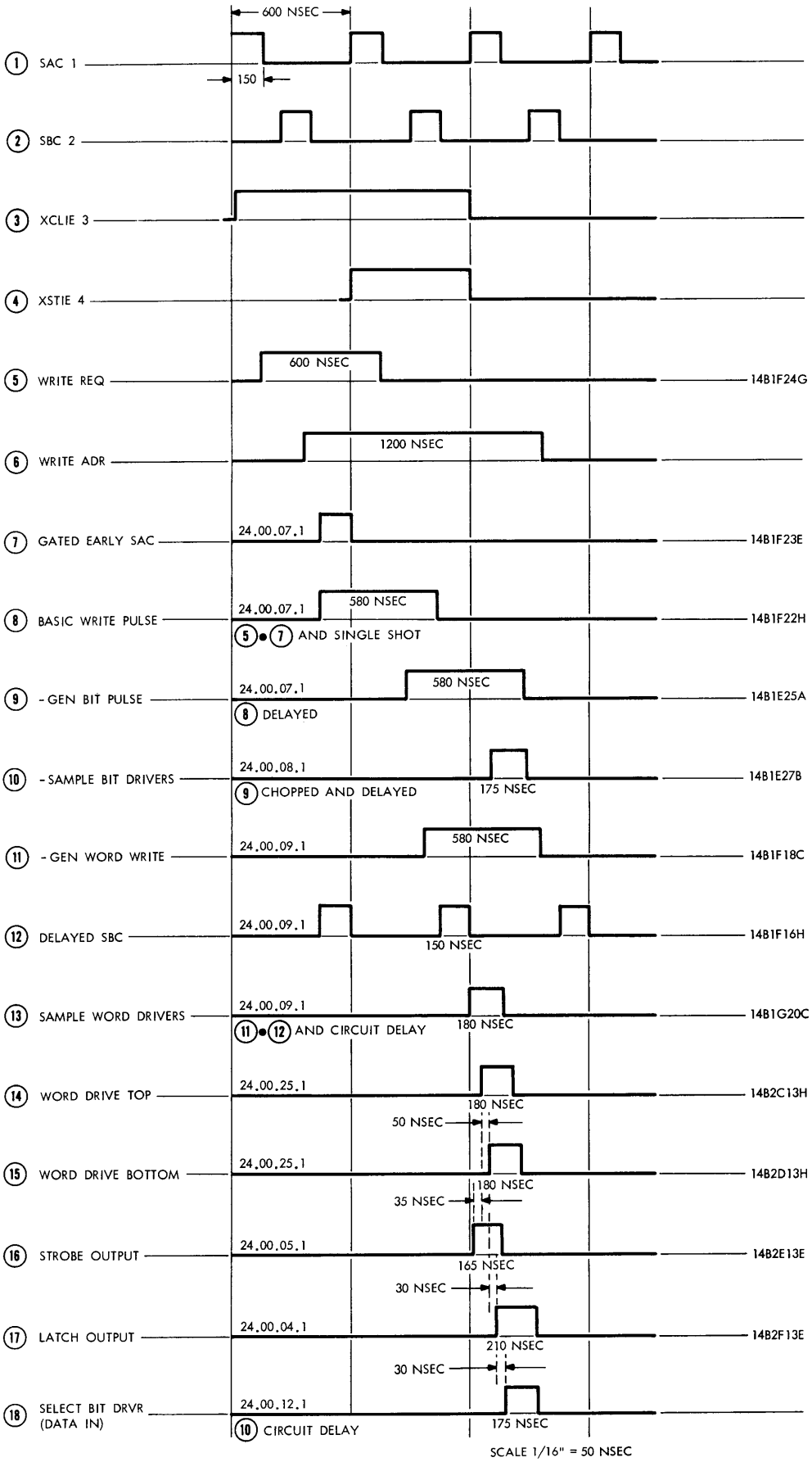
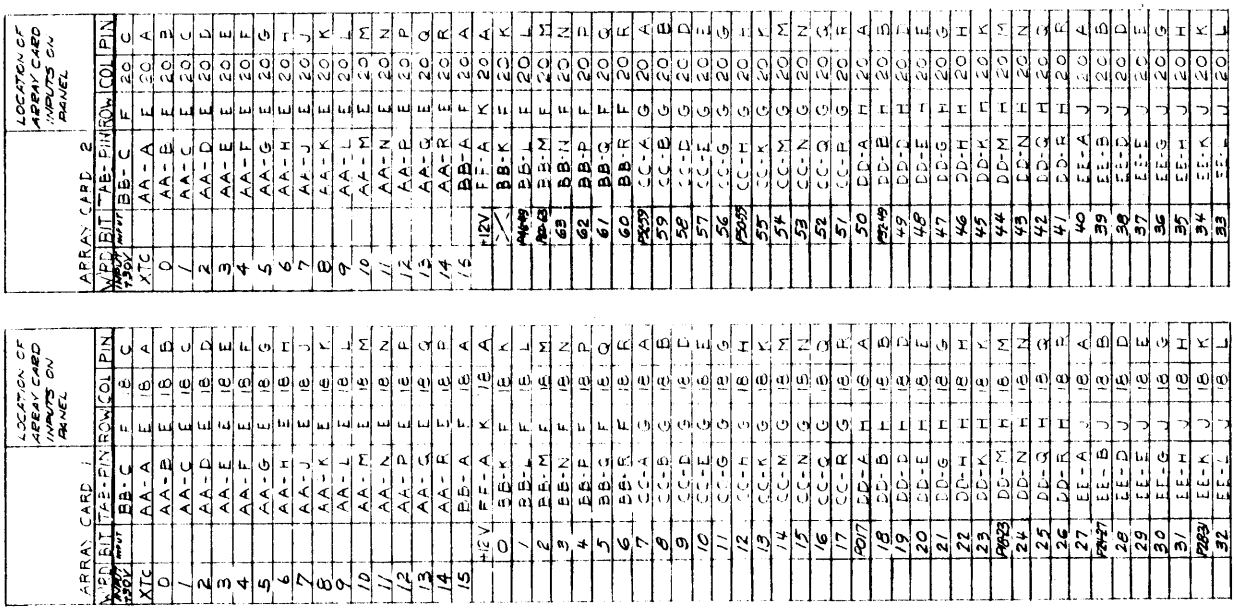


FIGURE 2.10.1. EXAMPLE OF STORE TIMING FOR INDEX TUNNEL DIODE STORAGE



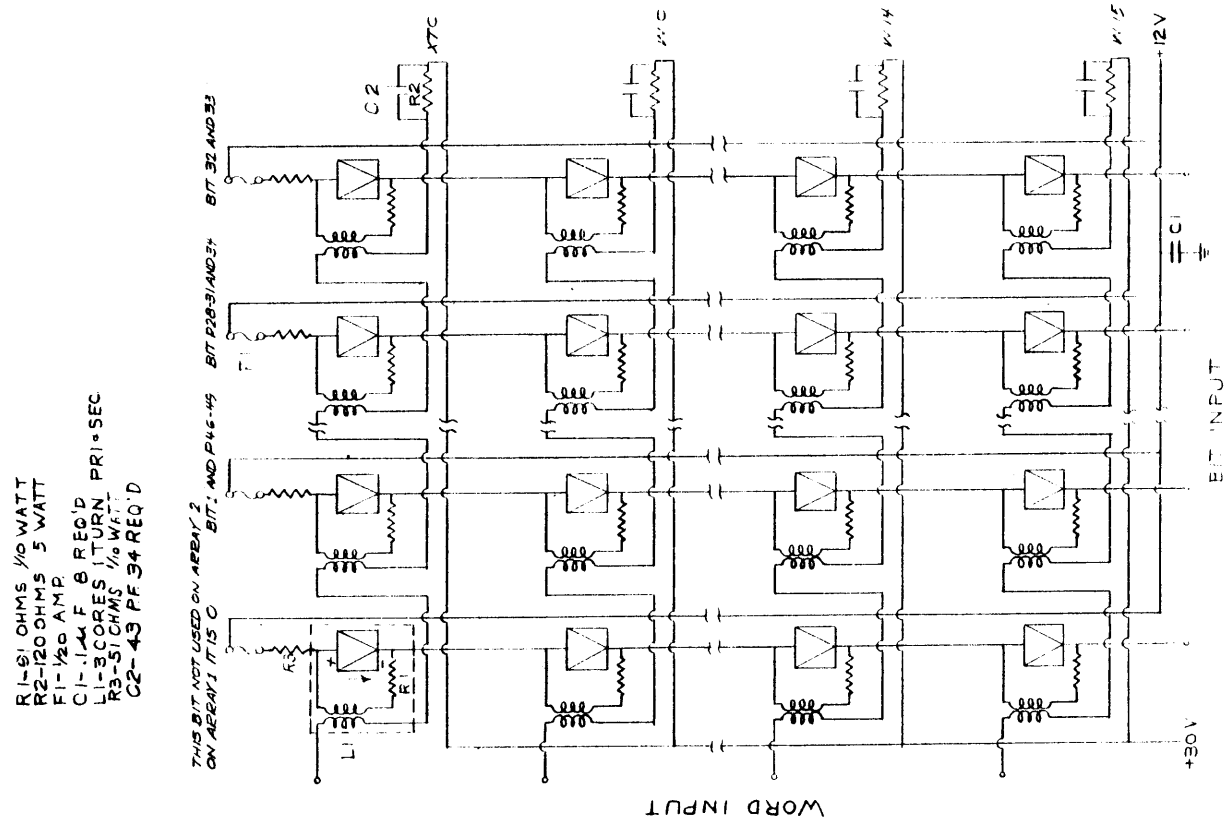


FIGURE 2.10.2. TUNNEL DIODE ARRAY CARD INPUTS

DESCRIPTION

Most of the errors which can occur on Sigma are not programmable and therefore cannot be checked in this manner. This procedure pinpoints appropriate SMS cards to remove which will generate these errors and also checks for a correct error scan.

PROCEDURAL STEPS

1. Set maintenance mode switch to ON.
2. Set scan inhibit switch to OFF.
3. Set stop-on-single-error switch to ON.
4. Cycle Sigma routines of SEVA program (or other program which exercises area being checked).
5. With program running, pull SMS card indicated in table 2.11.1.
6. Computer should stop with the appropriate error indicator on. If not, investigate cause, starting with logic shown.
7. A scan should have occurred.
8. Unload punch, and check scan card indicated (table 2.11.1) for correct error punch. No other error punches should be present.
9. Reload punch, and restart program for next error. (It is not necessary to clear the write check on the punch at this time.)
10. When all errors have been checked, restore console and punch to normal.

TABLE 2.11.1. SIGMA ERRORS

Error	SMS Card	Type	Logic	Loc	Scan Card	Col	Row	Remarks
ICLOC	13B4J26	DBZZ	21.04.06.1	1A & C	Σ1	46	6	
ICAIC	13B3A24	DDZX	21.04.03.1	3I	Σ1	46	5	
ICAC	13B3E14	UWRE	21.04.05.1	3A	Σ1	46	4	
IABC	13A4A28	DDZY	27.04.03.1	3F	Σ1	46	3	
IAIC	13A4J28	DK--	27.10.02.1	4E	Σ1	46	2	
IAC1	13A4C11	DBZW	27.11.01.1	5A & C	Σ1	46	1	
IAC2	13A4C10	DBZW	27.11.02.1	5A & C	Σ1	46	0	
IAC3	13A4C09	DBZW	27.11.03.1	5A & C	Σ1	46	11	
IAC4	13A3C20	DBZW	27.11.04.1	5A & C	Σ1	46	12	
IAC5	13A3C19	DBZW	27.11.05.1	5A & C	Σ1	45	9	
IAC6	13A3C18	DBZW	27.11.06.1	5A & C	Σ1	45	8	
XAC	14B3E21	DEZJ	24.00.01.1	3H	Σ1	46	8	
~~LA ADR ERR~~	~~11A1E18~~	~~ZADR~~	~~15.02.04.1~~	~~4C~~	~~Σ1*~~	~~54~~	~~0~~	~~*(X2 & up only)~~
~~RA PAR~~	~~11B1E24~~	~~DEYY~~	~~14.03.01.1~~	~~3J~~	~~Σ1*~~	~~64~~	~~3~~	~~*(X2 & up only)~~
RES COMP	21B4J23	DBZU	59.06.03.1	2D & E	Σ3	61	5	
LU COMP	21A1E27	DBZX	53.56.01.1 02.1	1D	Σ3	61	6	
~~AB PAR~~	~~24A2B06*~~	~~DBZS~~	~~59.01.01.1~~	~~1G~~	~~Σ3~~	~~61~~	~~7~~	~~*(X2 & up only)~~
CD PAR	24A2C02	DBZS	59.51.01.1	1G	Σ3	61	8	
WI PAR	21A2E13	DFYZ	52.80.05.1	3C	Σ3	61	9	
BNDREG PAR	12A4C10	DK--	16.04.01.1	5B & D	Σ4	55	4	
I PARITY	20A1E24	DFYY	34.08.41.1	4A	Σ4	35*	12*	*34-9 for X1, X2, & K1
LA PARITY	20A1E27	DEYY	34.08.41.1	4E	Σ4	34	9*	*Row 8 for X1, X2, & K1
UNCOR ECC	20A2D06	DBZZ	34.08.61.1	5D	Σ4	35	1L*	*Row 12 for X1, X2, & K1
DBL. ECC PERM	20A3E08	DBZZ	34.01.52.1	1B & H	Σ4	34	7*	*Row 6 for X1, X2, & K1
A CKR PAR	24A4A09	SV--	41.03.01.1	5I	Σ4	13	12	
A CKR RES	24A4J18	DBZZ	45.02.02.1	4E	Σ4	12	9	
LA ADR ERR	~~11A1E18~~ 11A2E19	~~ZADR~~ ZA1J	15.02.04.1	~~4C~~ 4C	Σ4*	55	12	*(X1, X2, & K1 only)
RA PAR	11B1E24	DEYY	14.03.01.1	3J	Σ4*	64	3	*(X1, X2, & K1 only)
AB PAR	24A2C02*	DBZS	59.01.01.1	1G	Σ3	61	7	*(X1, X2, & K1 only)

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2	LA Flow Diagrams
3	PAU Flow Diagrams and Tables
4	Indicators
5	Switches
6	Maintenance Programs
7	Error Analysis
8	PAU Timing Charts
9	Sigma Errors That Cause a Scan
10	Test Equipment, Tools, and Maintenance Supplies Required to Test Tunnel Diode Array
11	SAU Flow Diagrams

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3.1.6	Y-Z Start Trigger and YR-ZL Transfer Sequencer	1/1/63
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3.1.8	YL-ZL Transfer Sequencer	1/1/63
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3.3.4	Floating Point – Add (+), Add Magnitude (+MG), Add Double (D+), Add Magnitude Double (D+MG),	2/1/62
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3.3.12	Floating Point – Store Low Order (SLO)	2/1/62
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3.3.14	Floating Point – Add to Exponent (E+), Add Immediate to Exponent (E+I)	2/1/62
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3.7.16	Conditions for Setting ZDF Trigger in I Unit	2/1/62

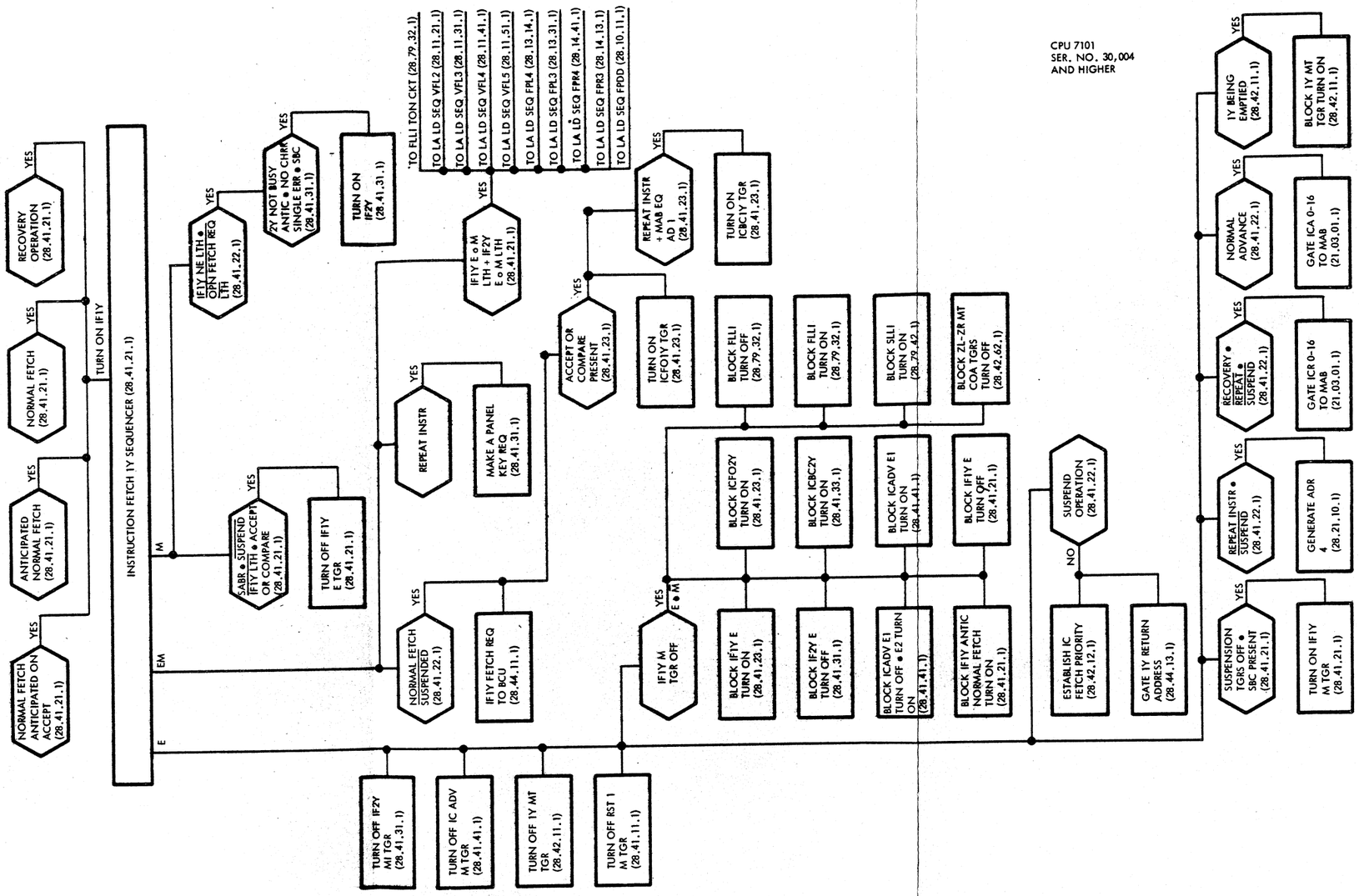


FIGURE 3.1.1. IF 1Y SEQUENCER

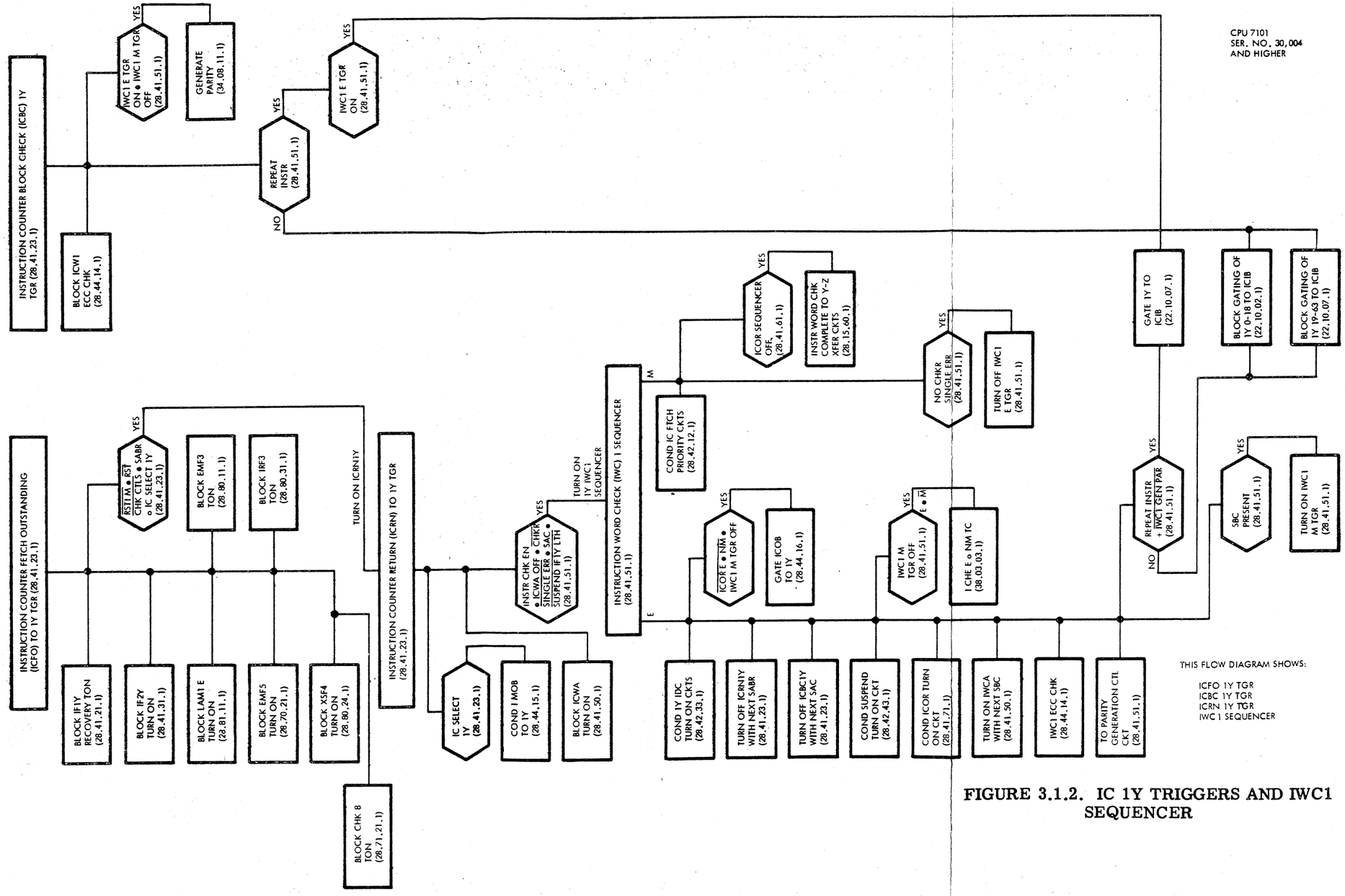


FIGURE 3.1.2. IC 1Y TRIGGERS AND IWC1 SEQUENCER

CPU 7101
SER. NO. 30,004
AND HIGHER

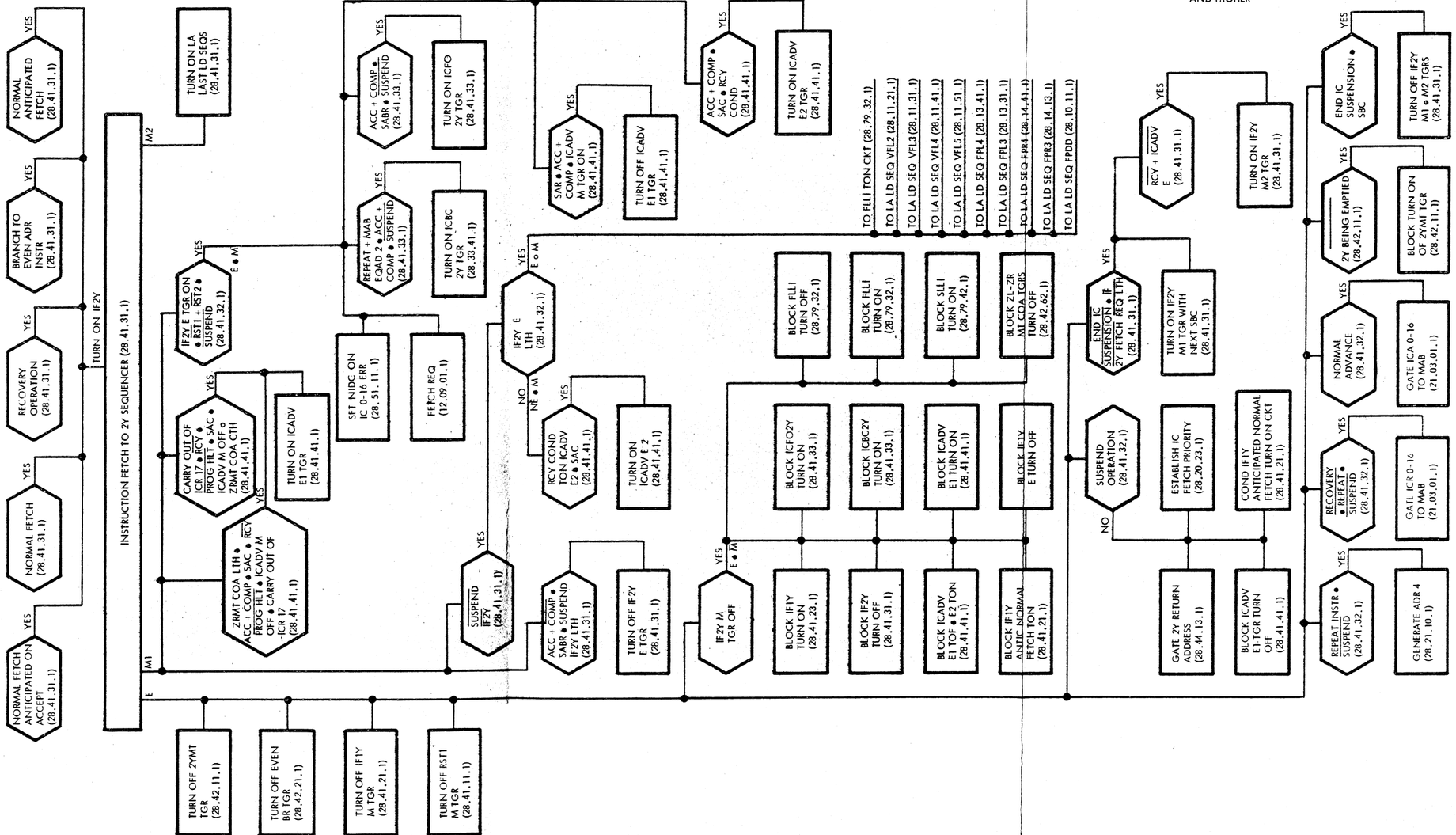


FIGURE 3.1.3. IF 2Y SEQUENCER

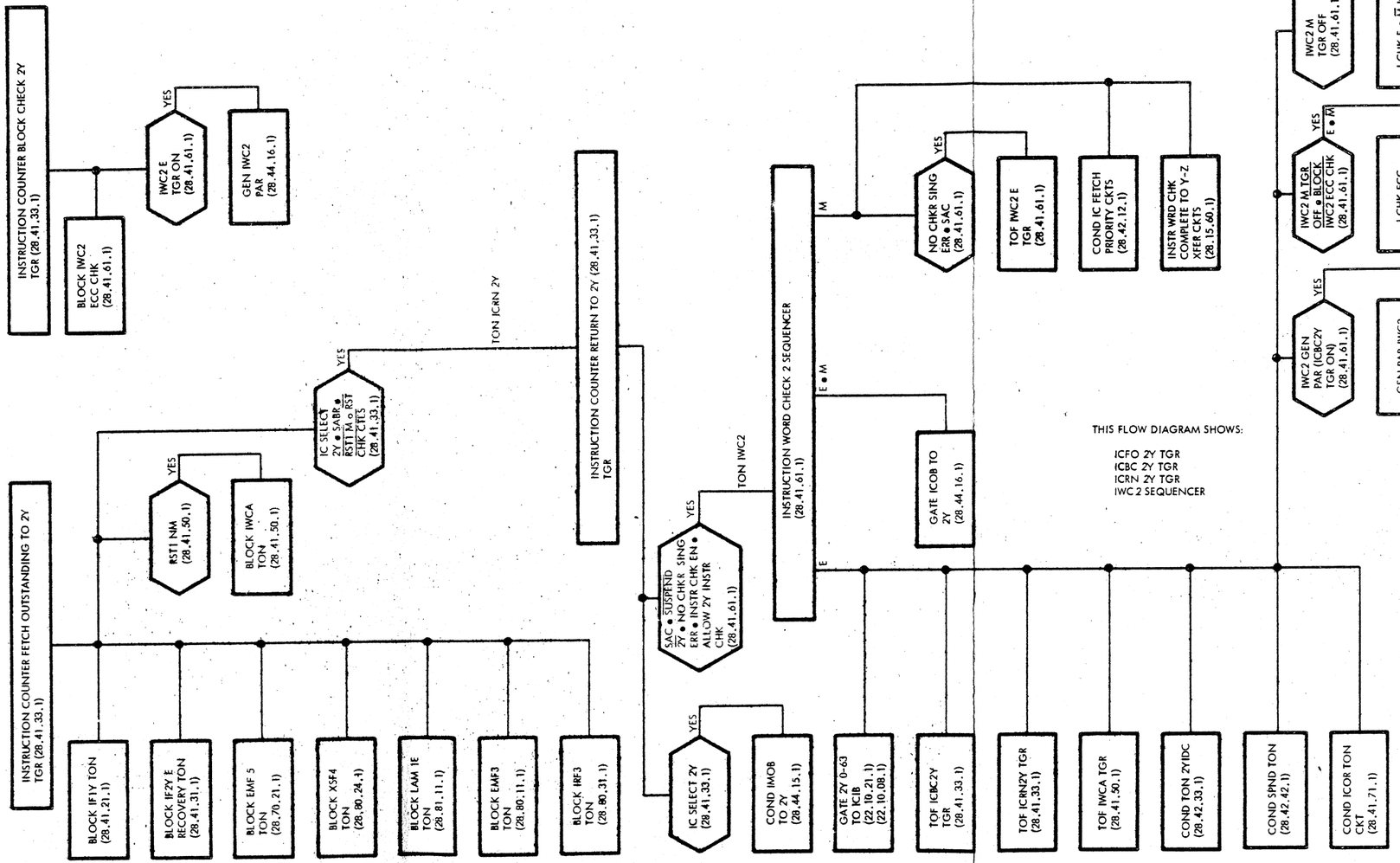


FIGURE 3.1.4. IC 2Y TRIGGERS AND IWC2 SEQUENCER

CPU 7101
SER. NO. 30,004
AND HIGHER

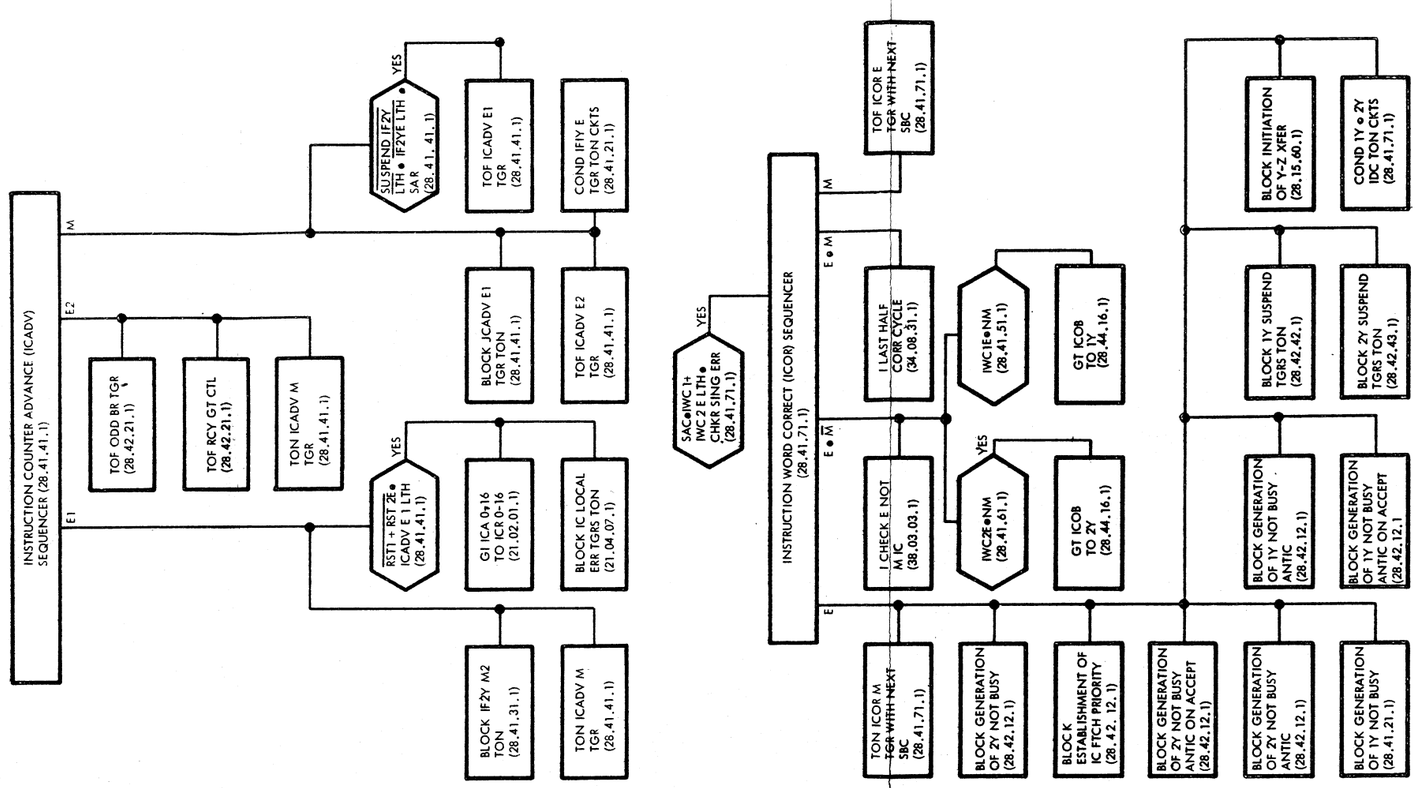


FIGURE 3.1.5. IC ADV SEQUENCER AND ICOR SEQUENCER

CPU 7101
SER. NO. 30,004
AND HIGHER

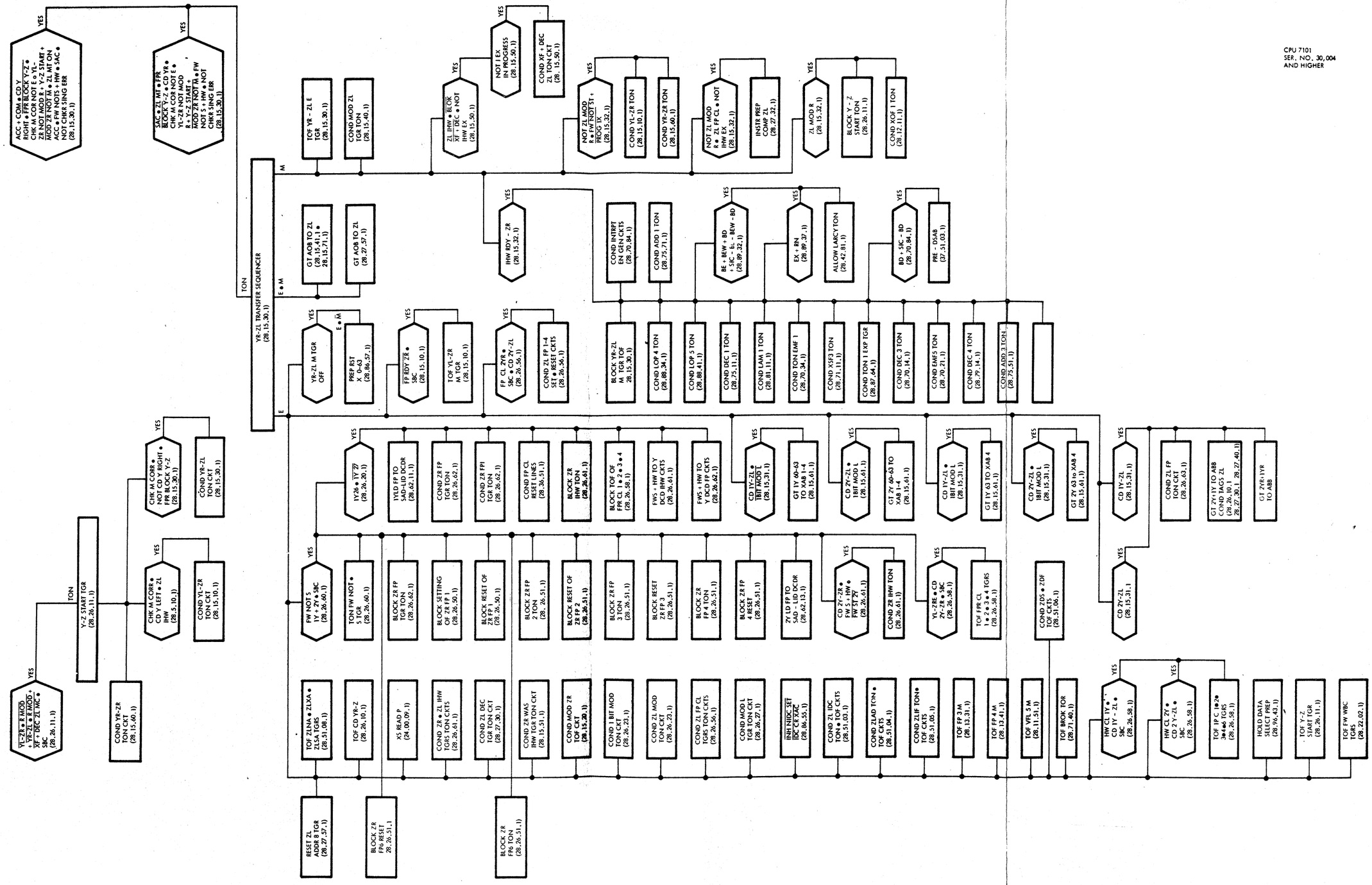


FIGURE 3.1.6. Y-Z START TRIGGER AND YR-ZL TRANSFER SEQUENCER

CPU 7101
SER. NO. 30,004
AND HIGHER

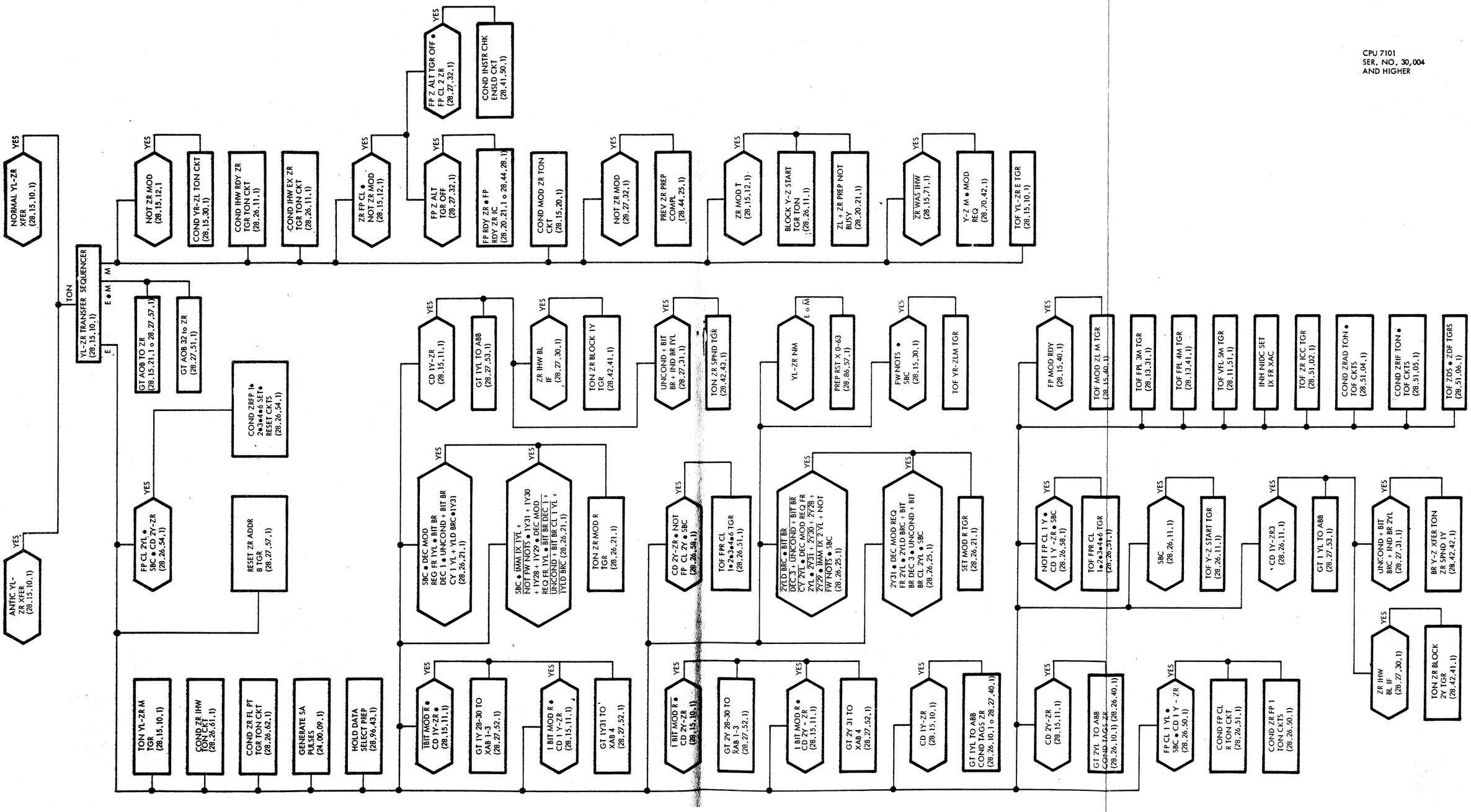


FIGURE 3.1.7. YL-ZR TRANSFER SEQUENCER

CPU 7101
SER. NO. 30,004
AND HIGHER

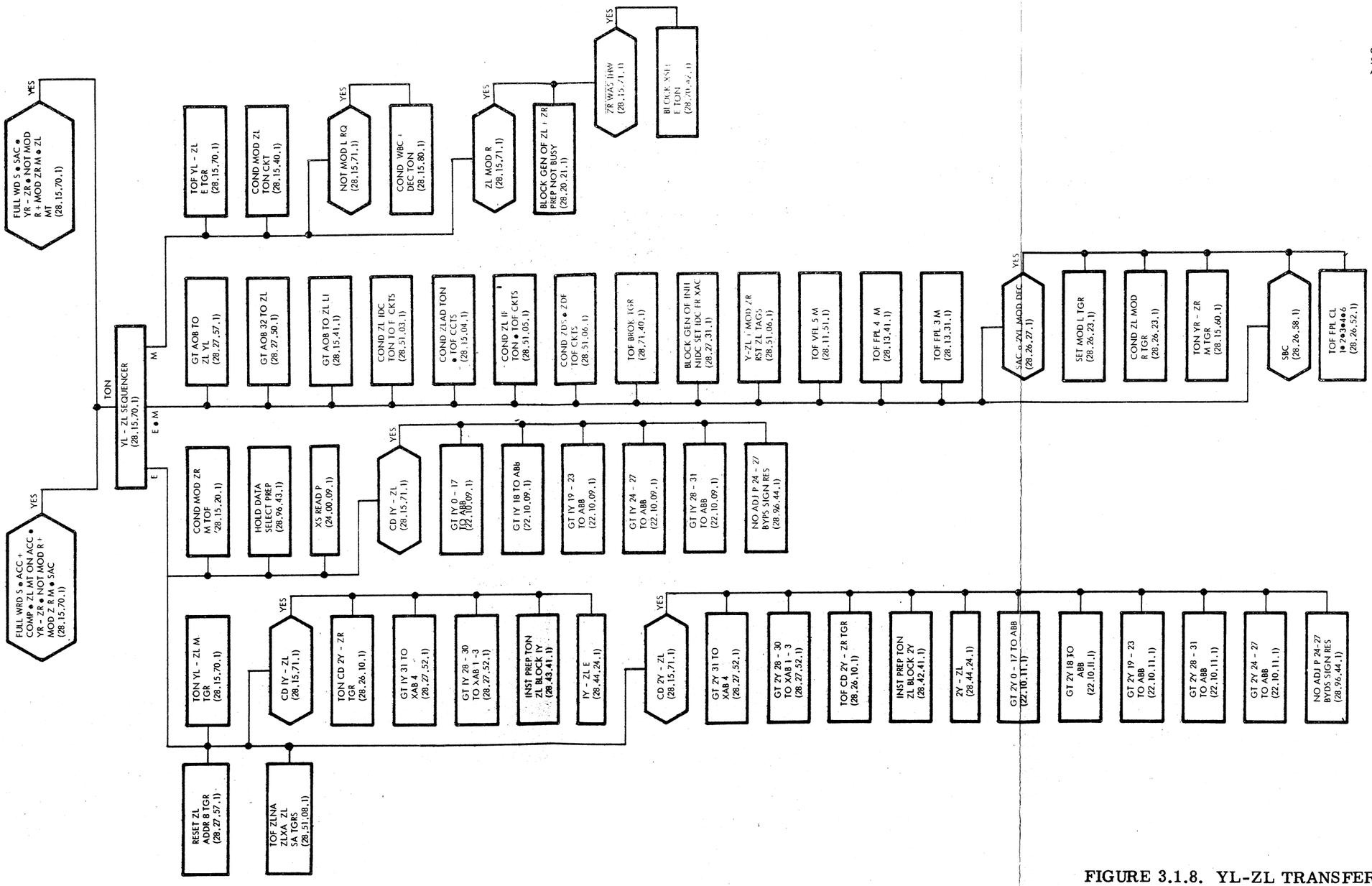


FIGURE 3.1.8. YL-ZL TRANSFER SEQUENCER

CPU 7101
SER. NO. 30,004
AND HIGHER

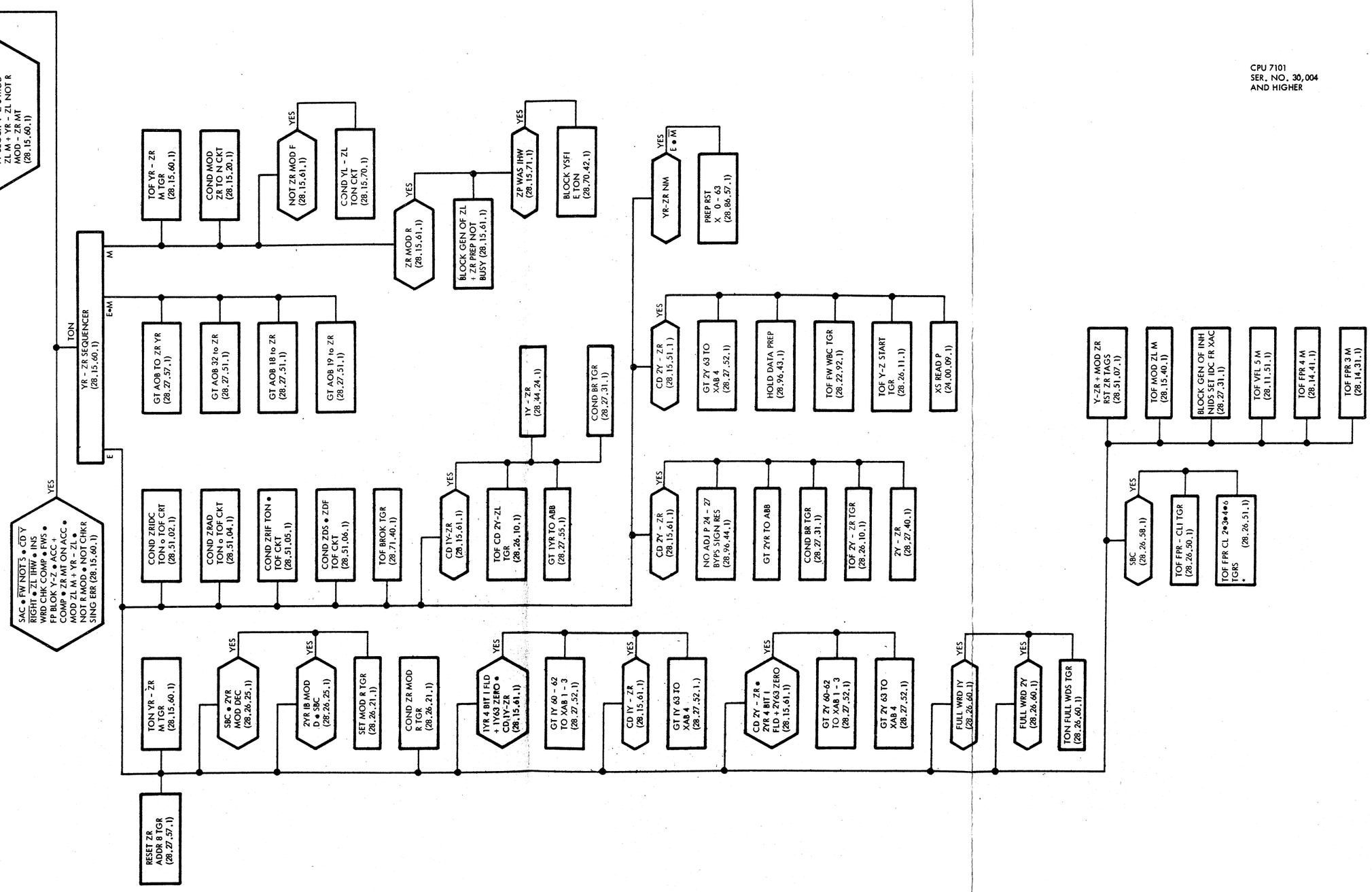


FIGURE 3.1.9. YR-ZR TRANSFER SEQUENCER

FIGURE 3.1.10. ZR MOD REQ TRIGGER AND MOD ZR SEQUENCER

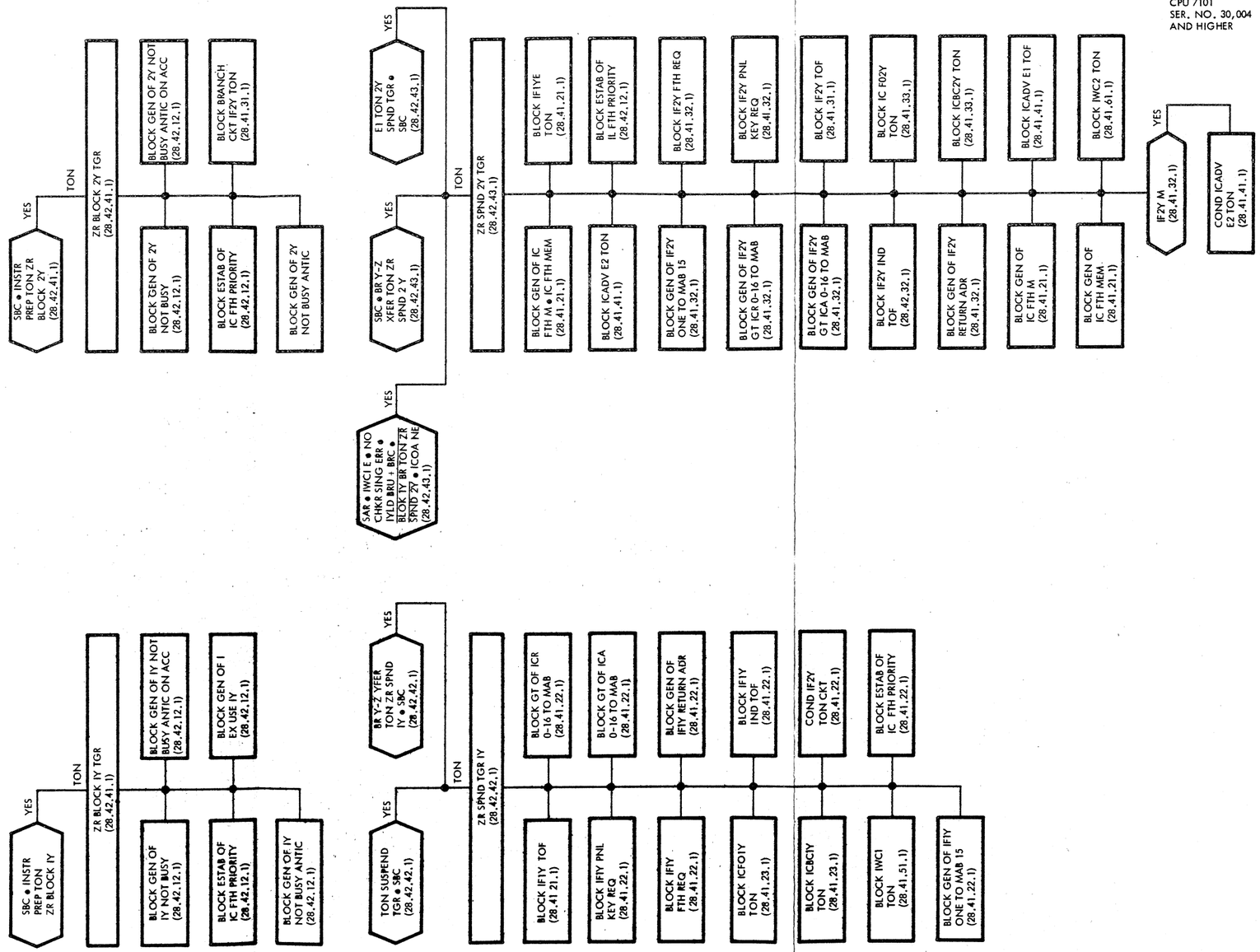


FIGURE 3.1.11. ZR BLOCK AND SUSPEND TRIGGERS

CPU 7101
SER. NO. 30,004
AND HIGHER

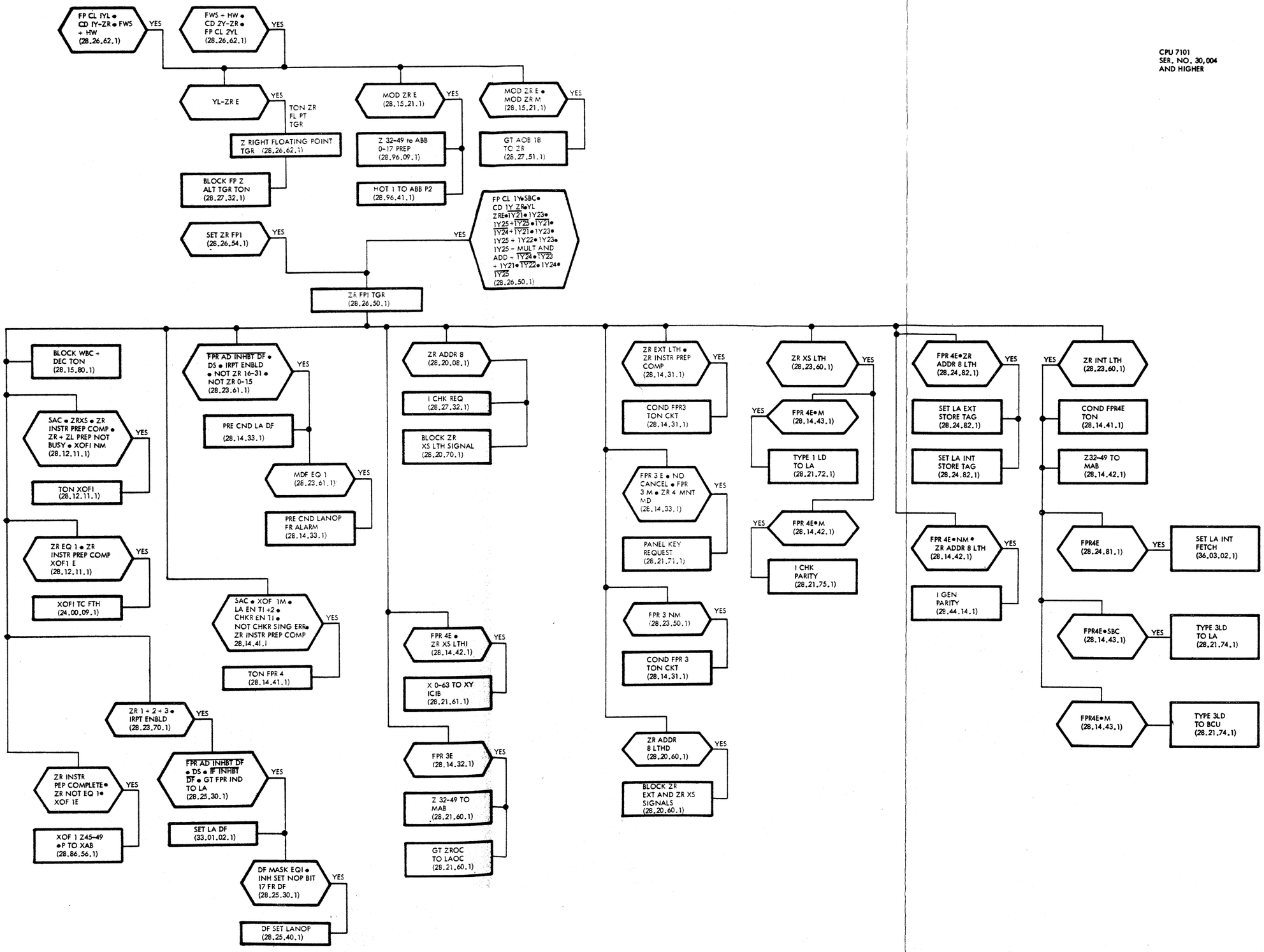


FIGURE 3.1.12. ZR FP 1 TRIGGER

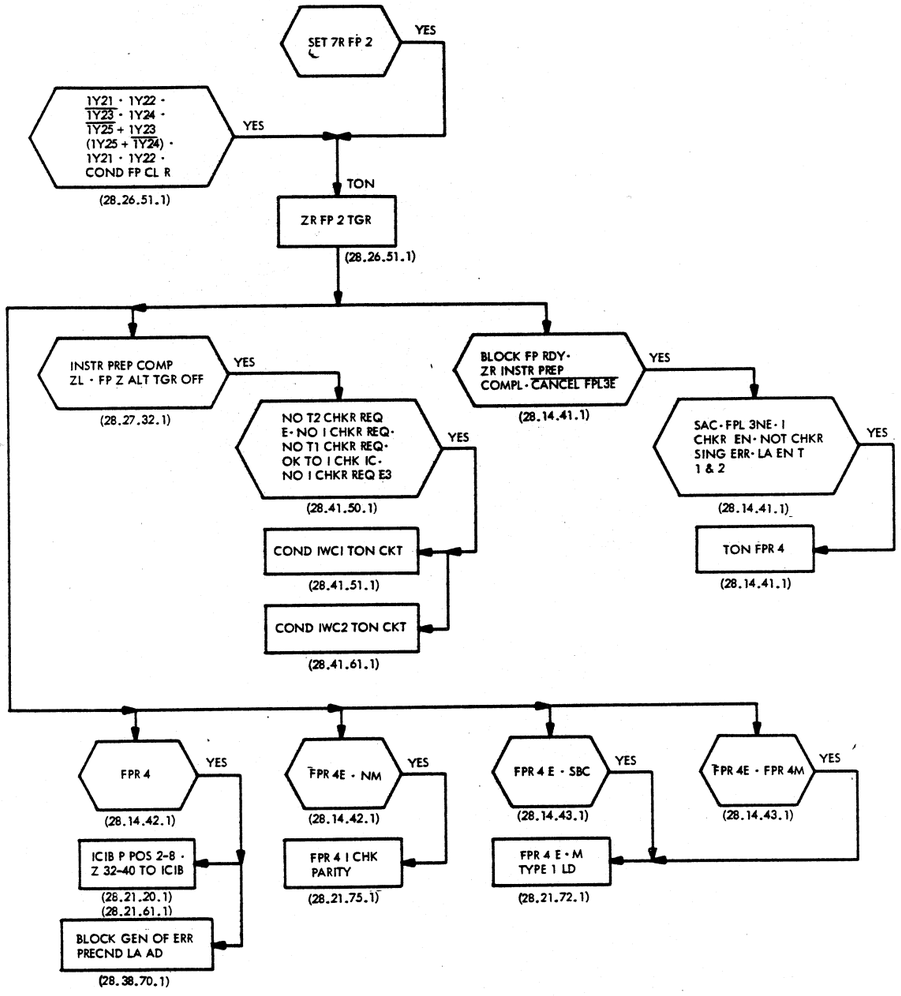


FIGURE 3.1.13. ZR FP TRIGGERS 2, 3, 4, AND 6 (SHEET 1 OF 3)

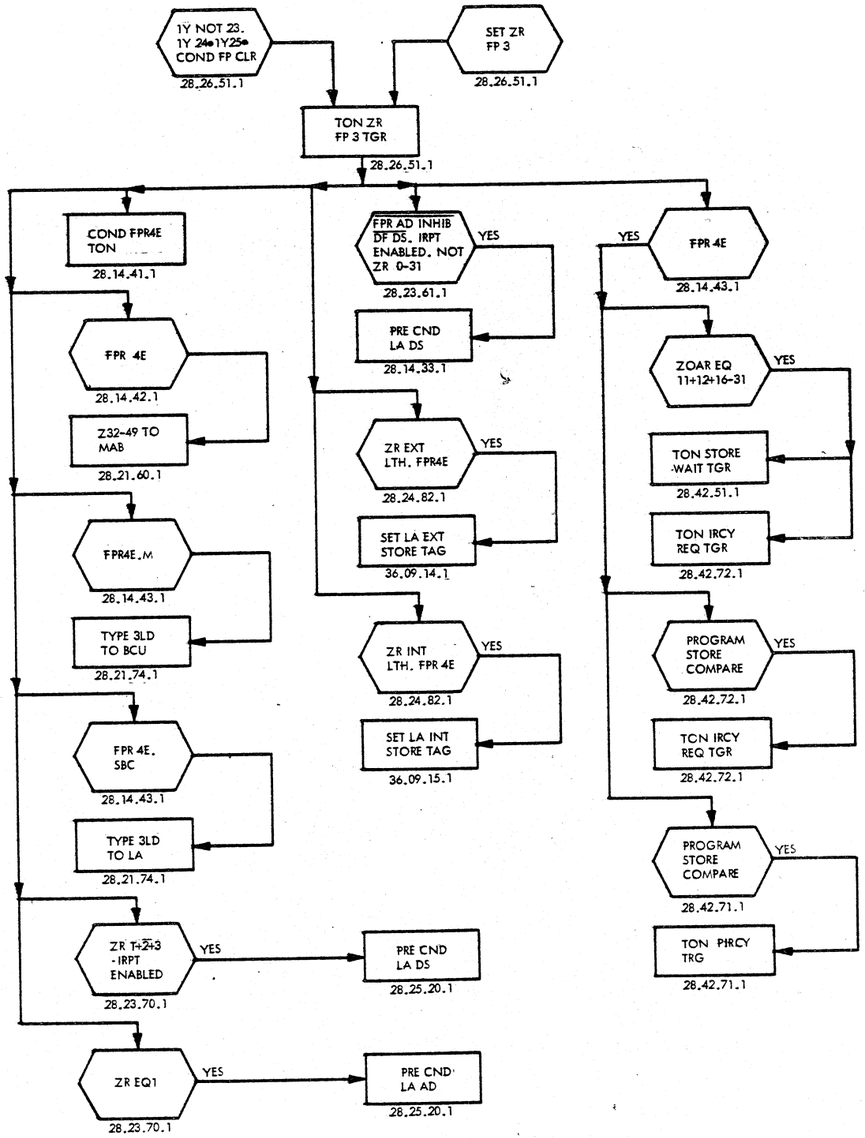


FIGURE 3.1.13. ZR FP TRIGGERS 2, 3, 4, AND 6 (SHEET 2 OF 3)

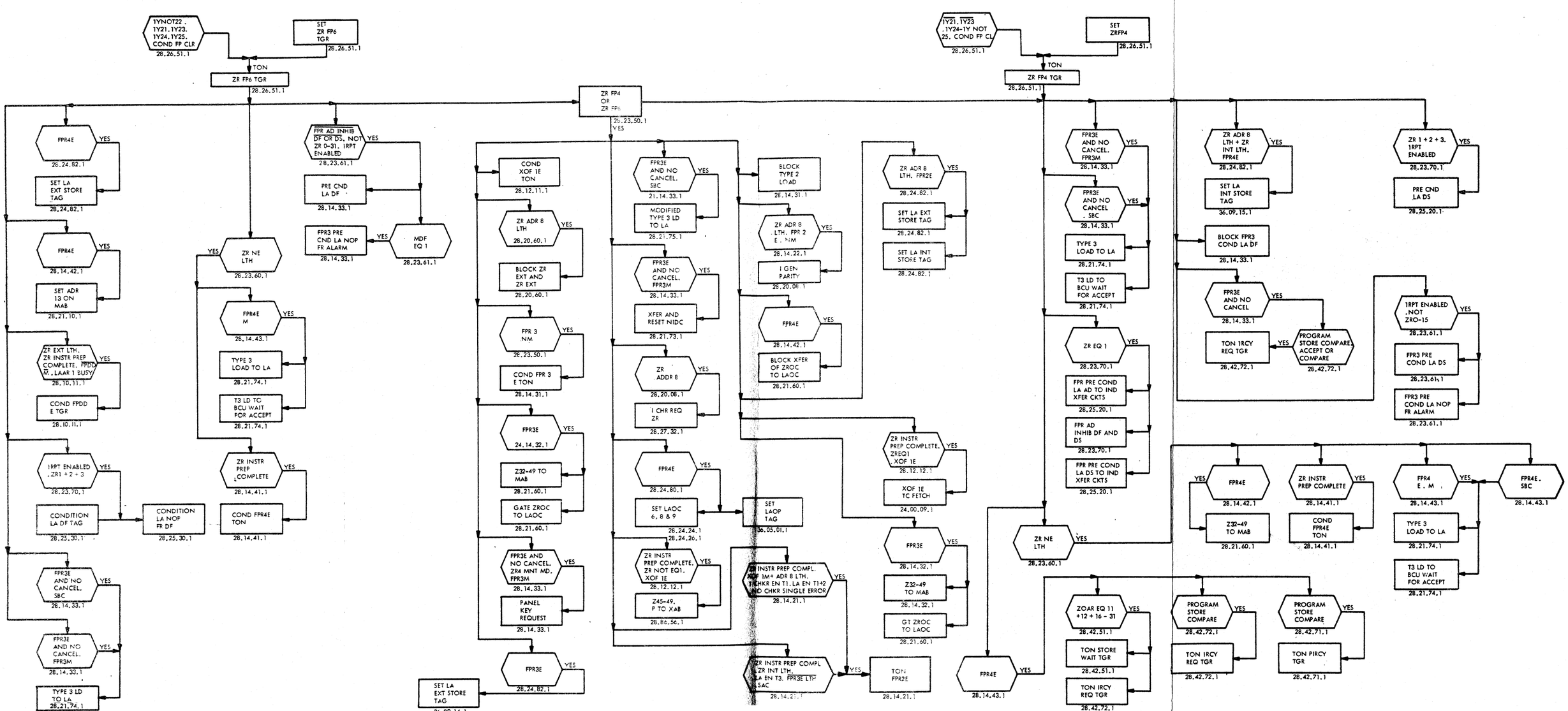
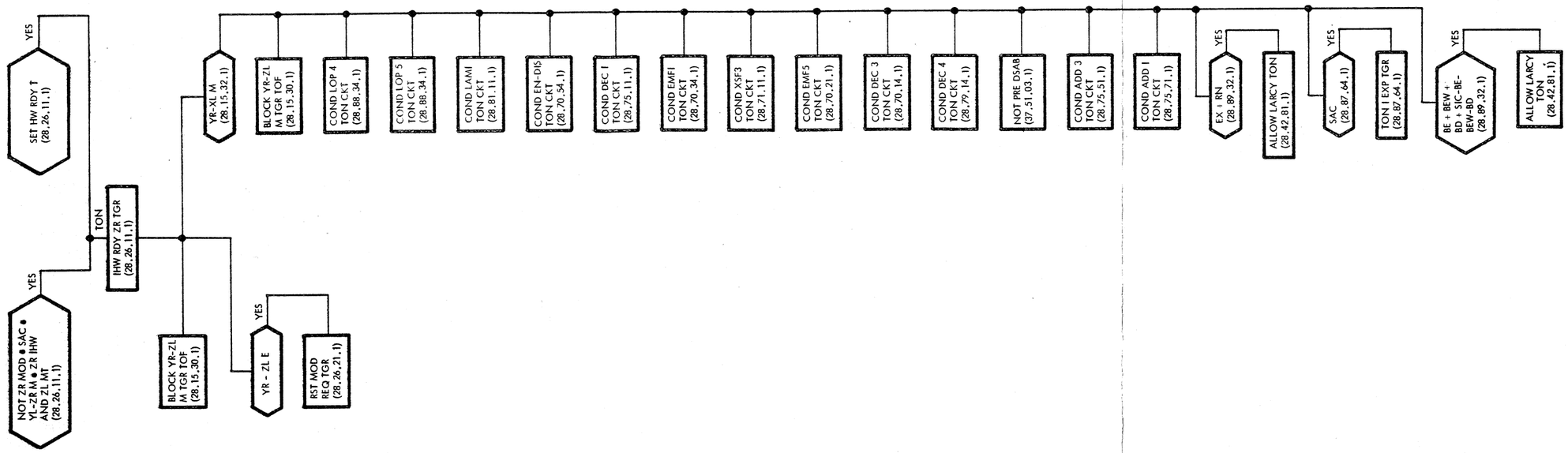


FIGURE 3.1.13. ZR FP TRIGGERS 2, 3, 4, AND 6 (SHEET 3 OF 3)



CPU 7101
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AND HIGHER

FIGURE 3.1.14. ZR IHW TRIGGER, IHW RDY TRIGGER, AND IHW EX ZR TRIGGER

CPU 7101
SER. NO. 30,004
AND HIGHER

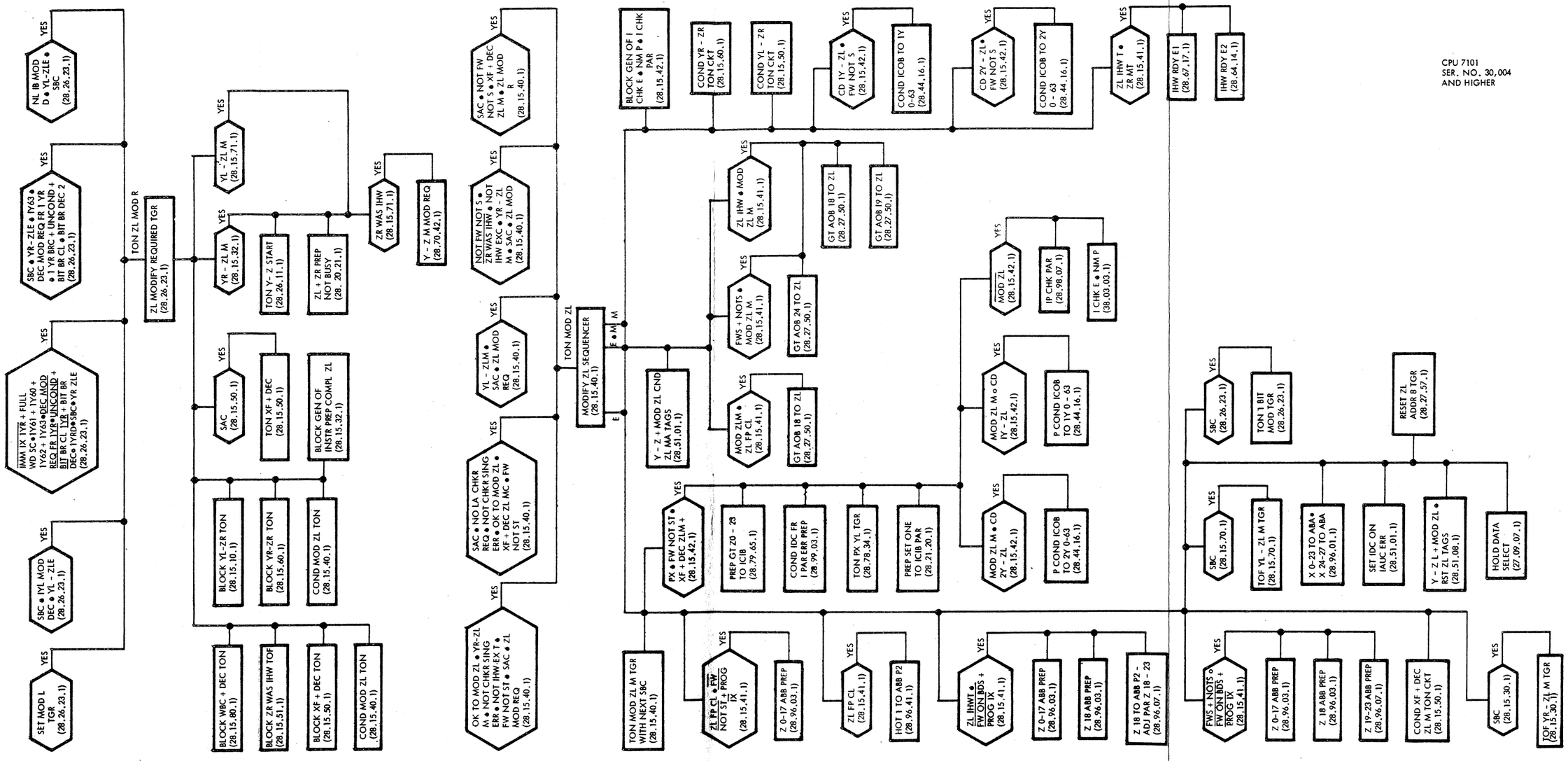

FIGURE 3.1.15. ZL MOD REQ TRIGGER AND MOD ZL SEQUENCER

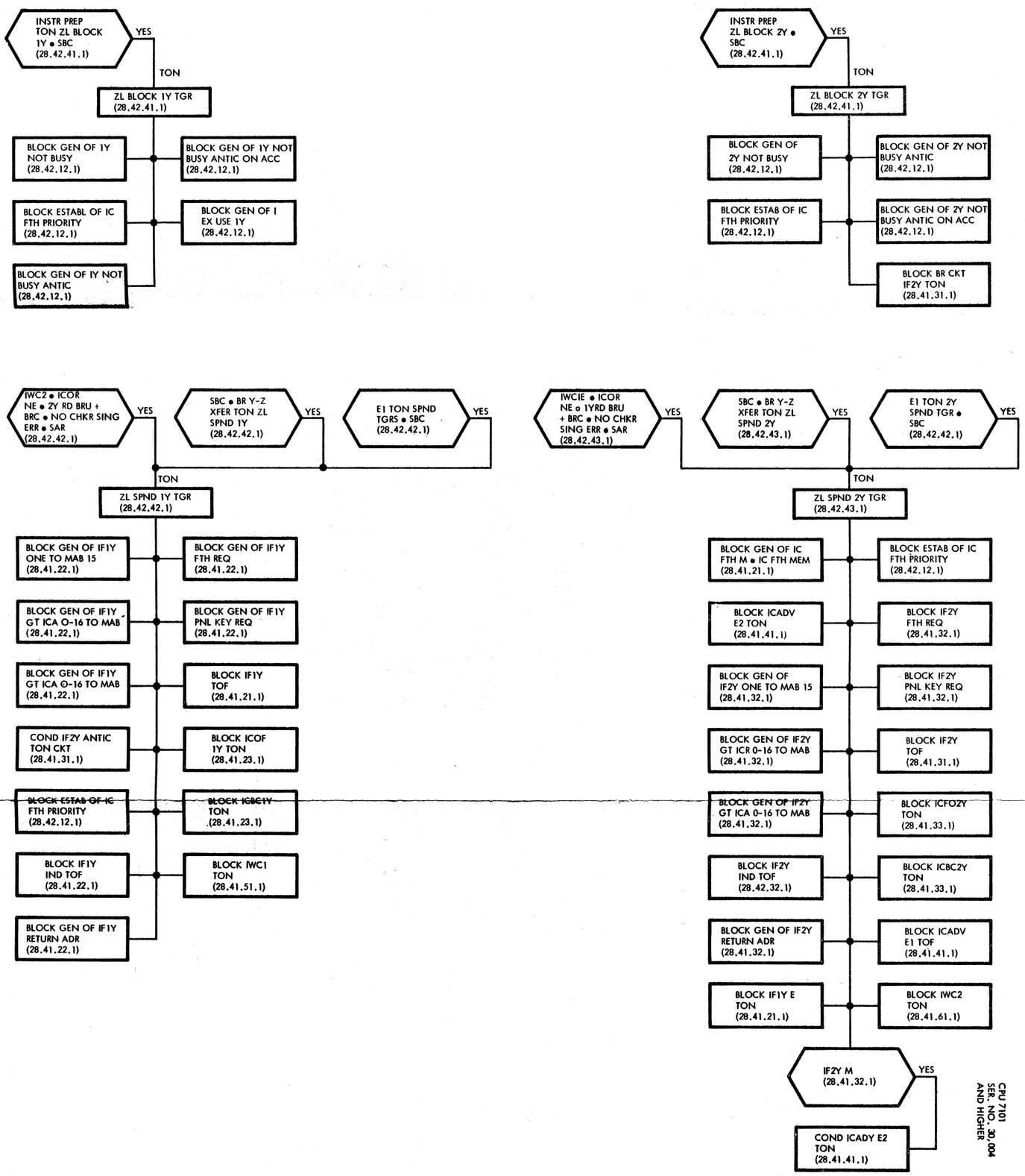

FIGURE 3.1.16. ZL BLOCK AND SUSPEND TRIGGERS

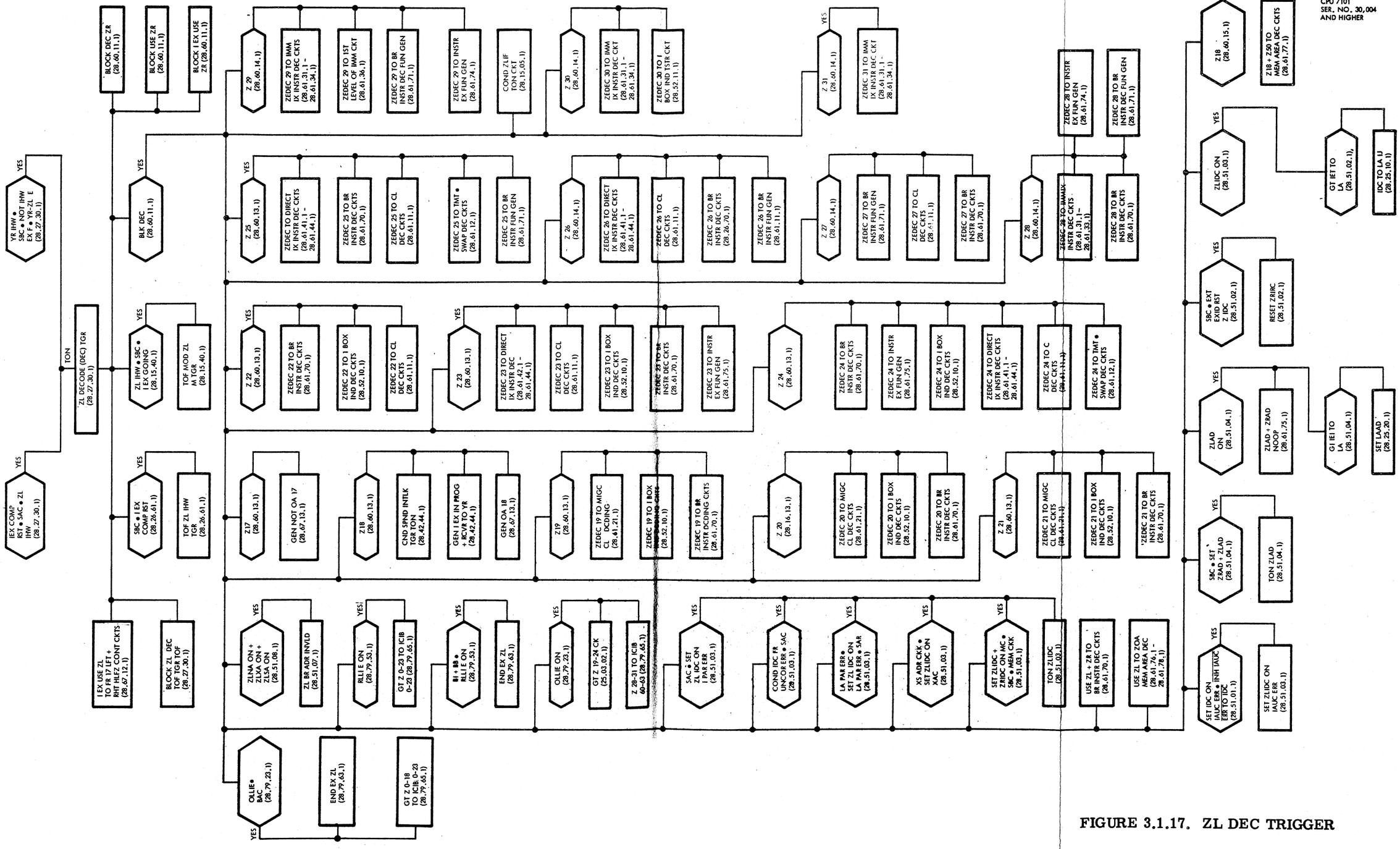

FIGURE 3.1.17. ZL DEC TRIGGER

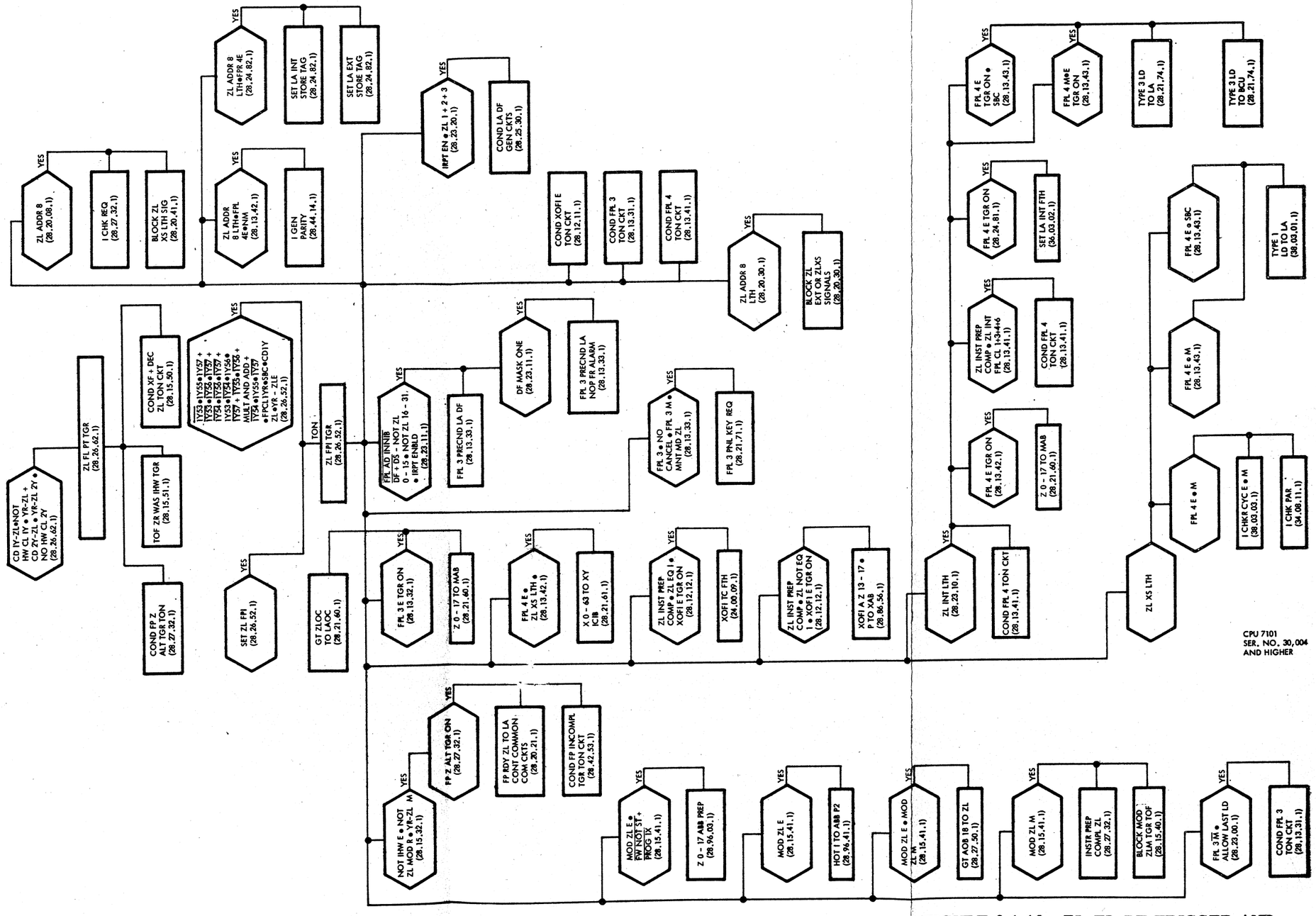

FIGURE 3.1.18. ZL FL PT TRIGGER AND ZL FP 1 TRIGGER

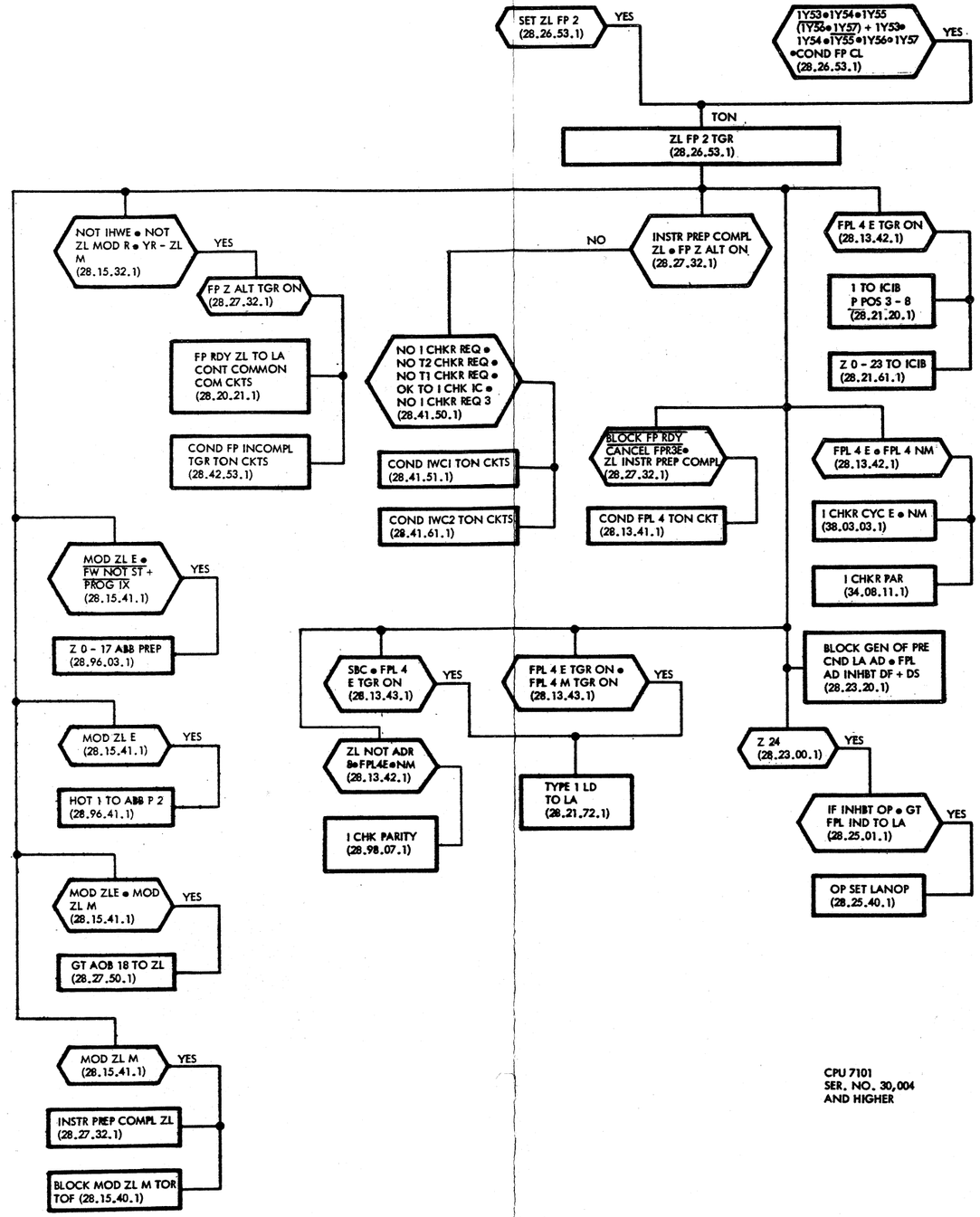

FIGURE 3.1.19. ZL FP2 TRIGGER

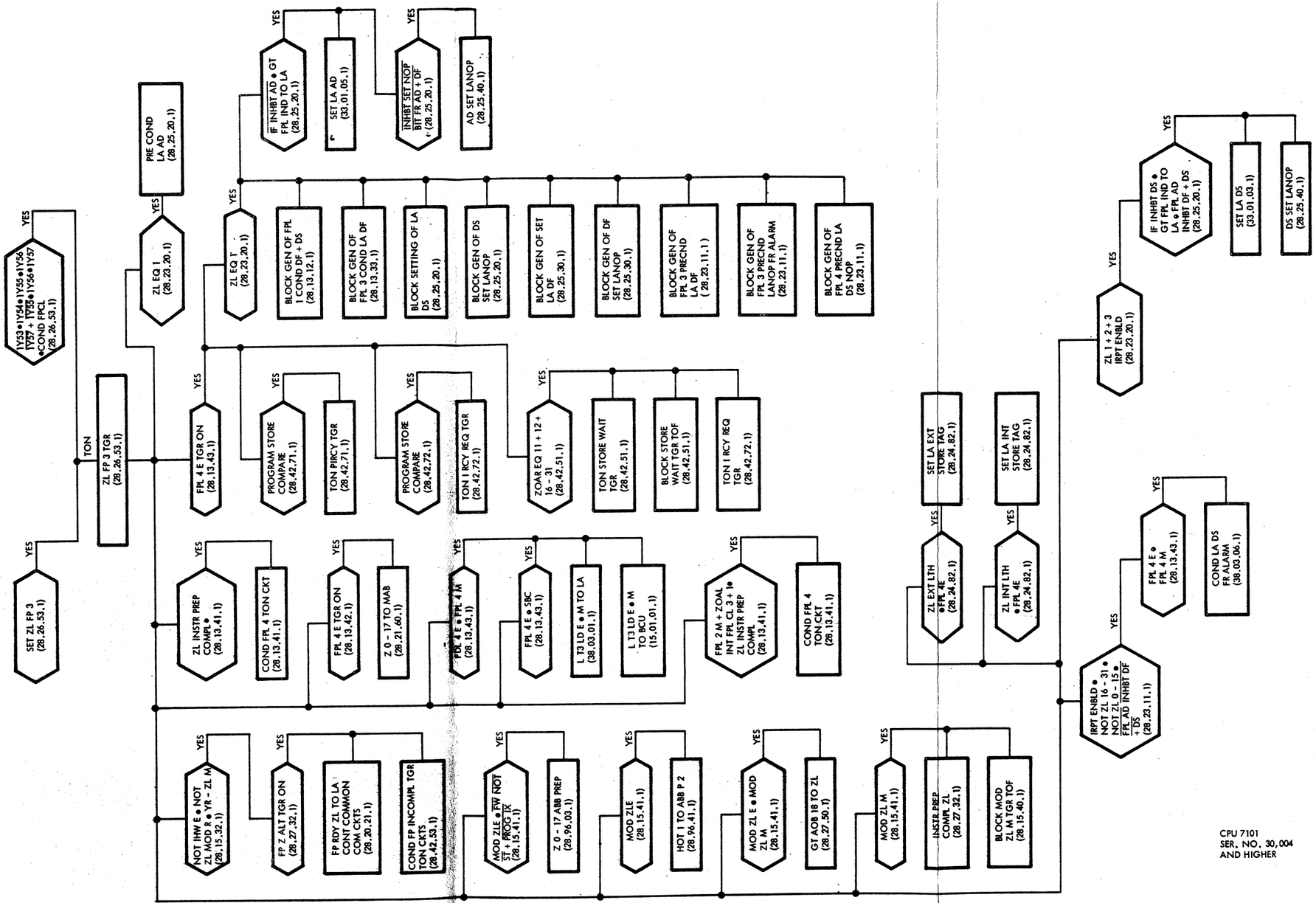

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FIGURE 3.1.20. ZL FP3 TRIGGER

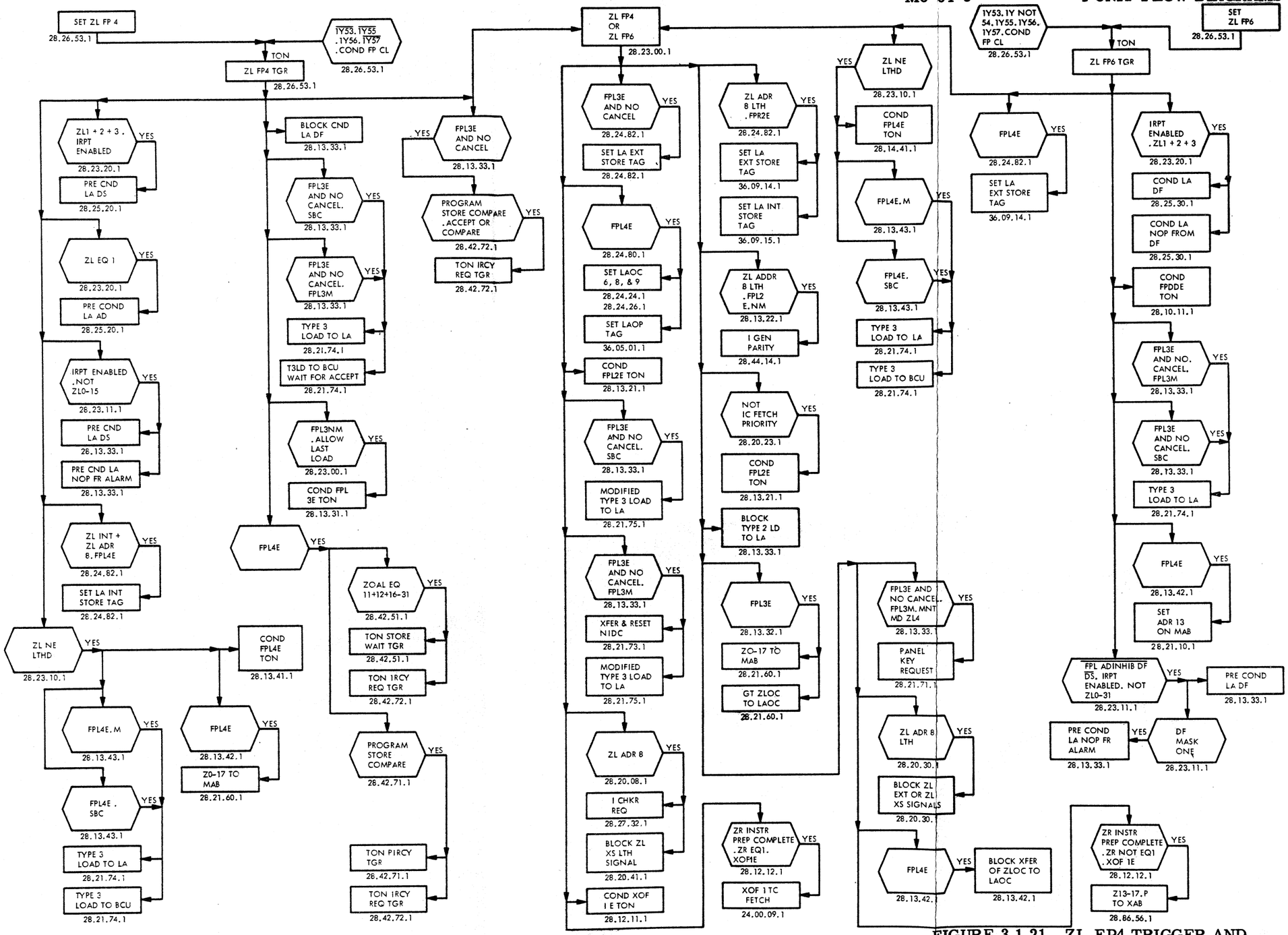


FIGURE 3.1.21. ZL FP4 TRIGGER AND ZL FP6 TRIGGER

CPU 7101
SER. NO. 30,004
AND HIGHER

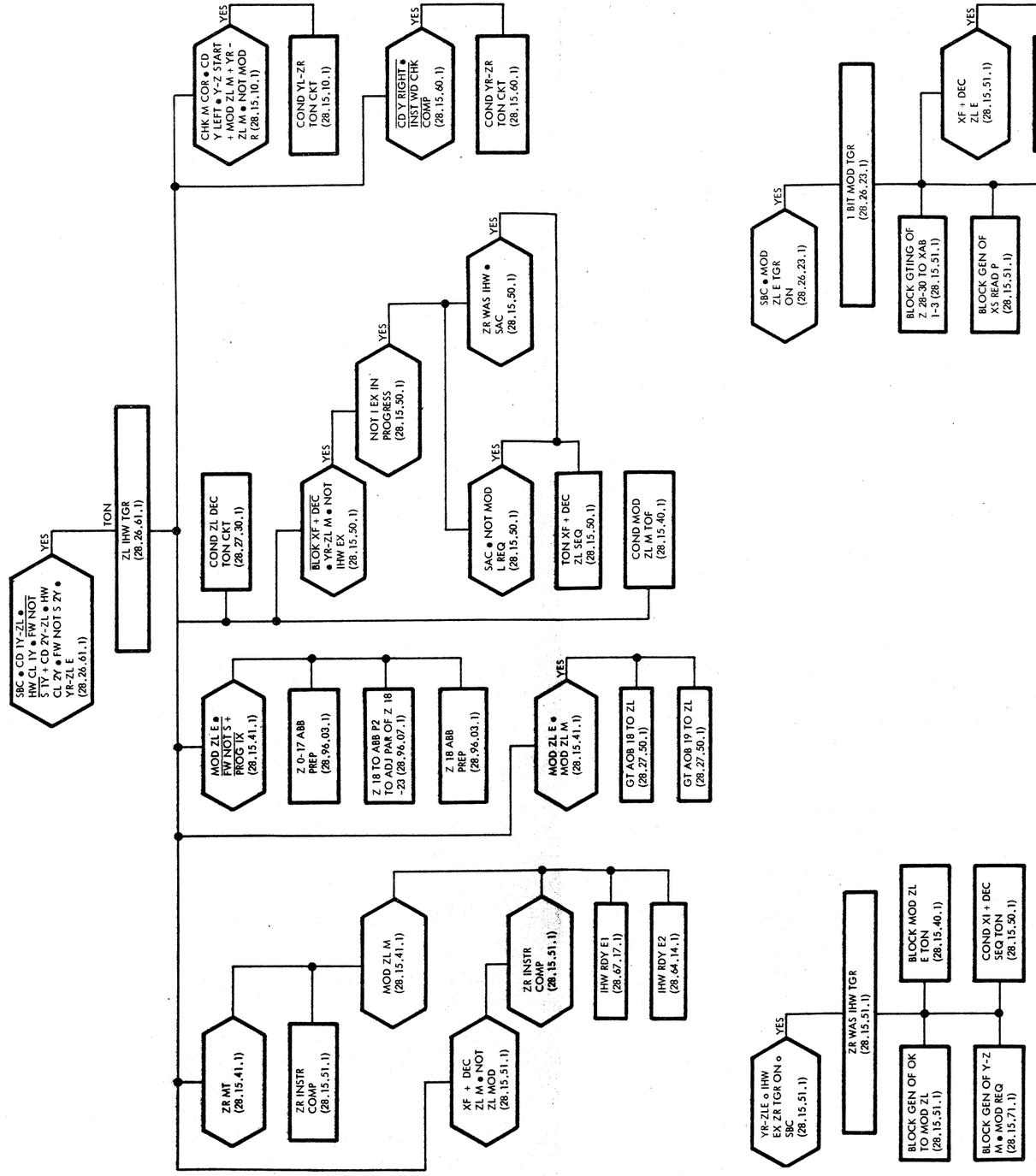


FIGURE 3.1.22. ZL IHW TRIGGER, ZR WAS IHW TRIGGER, 1 BIT MOD TRIGGER, AND FP Z ALT TRIGGER

CPU 7101
SER. NO. 30,004
AND HIGHER

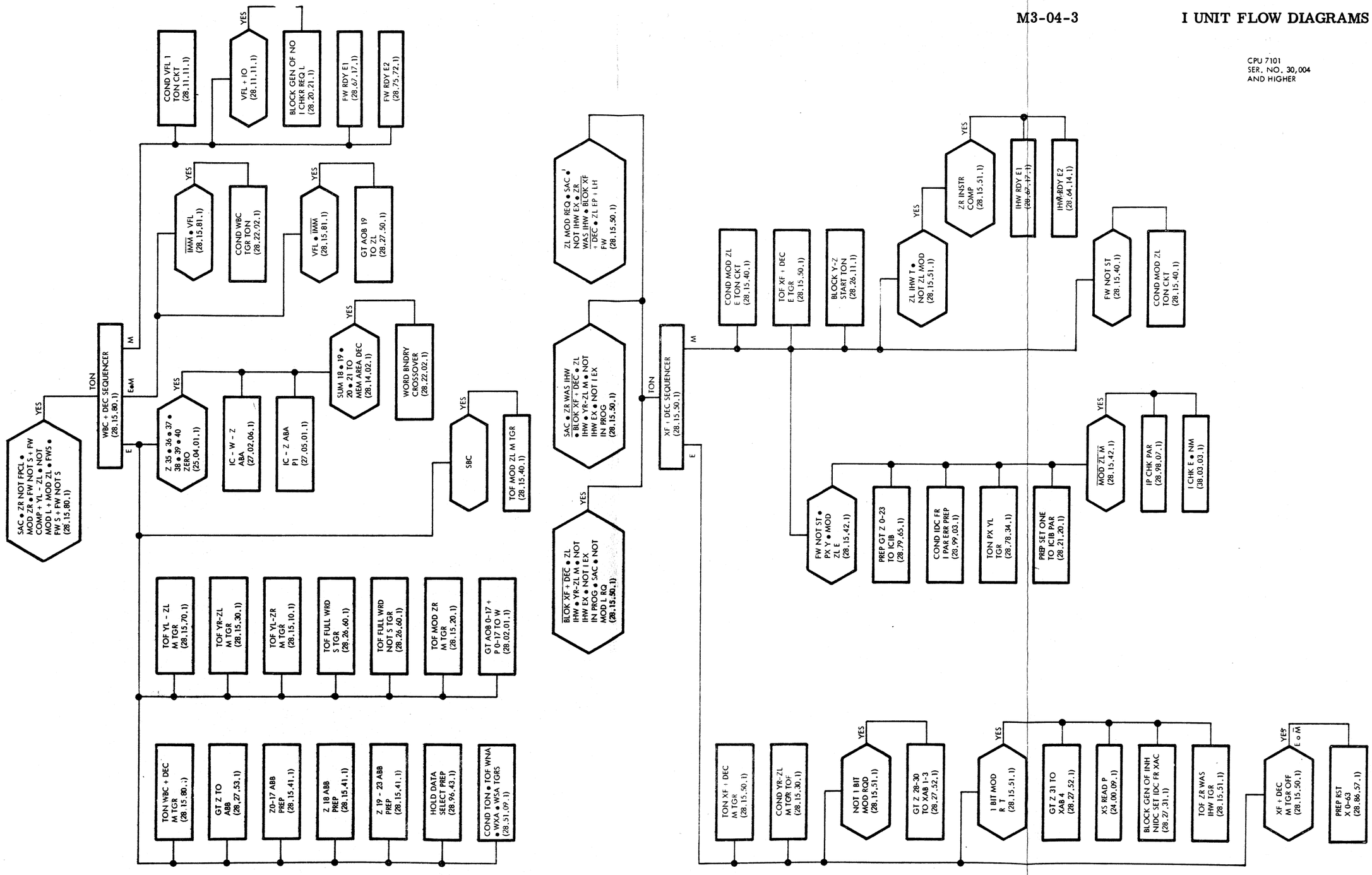


FIGURE 3.1.23. WBC + DEC SEQUENCER AND XF + DEC SEQUENCER

CPU 7101
SER. NO. 30,004
AND HIGHER

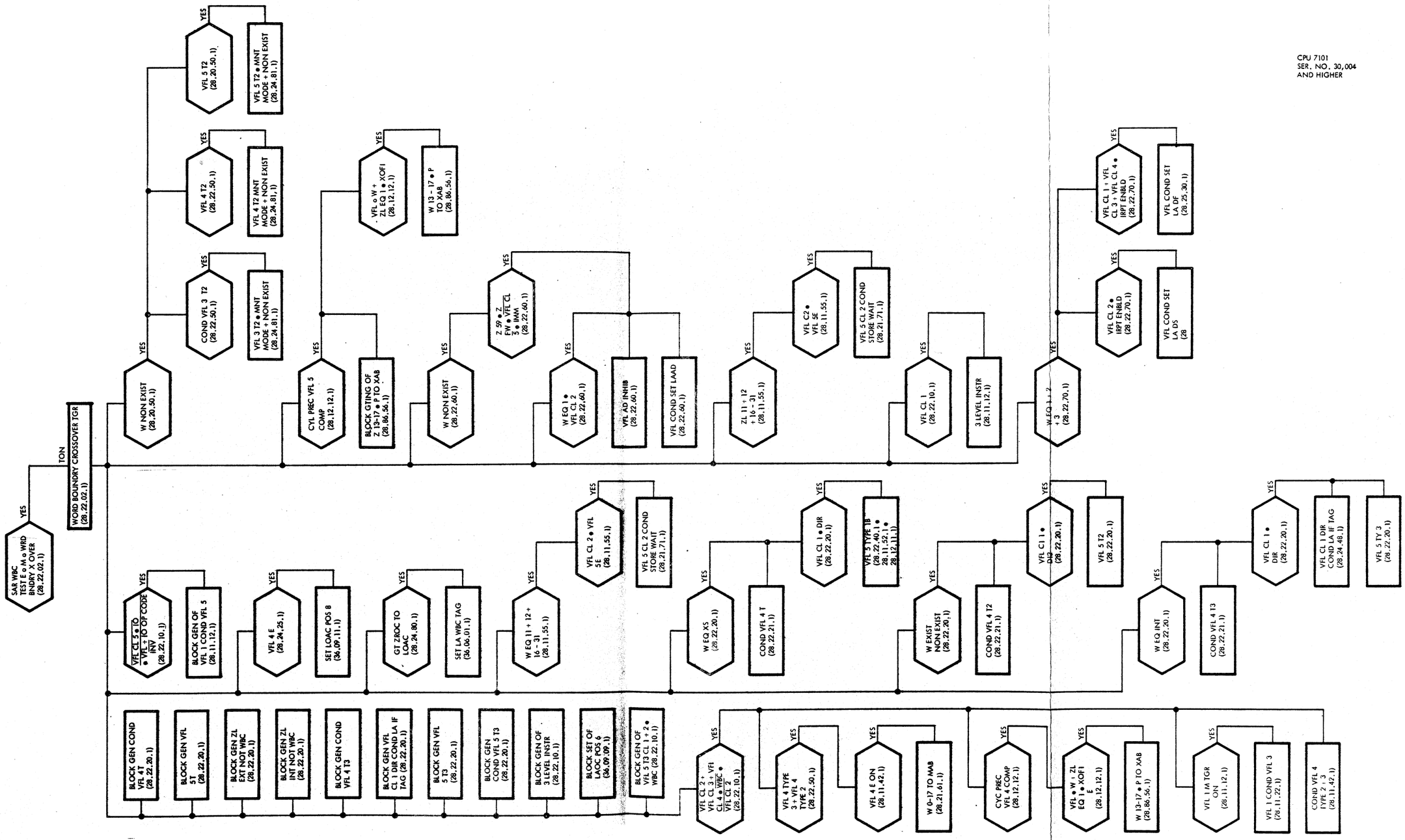


FIGURE 3.1.24. WBC TRIGGER

CPU 7101
SER. NO. 30,004
AND HIGHER

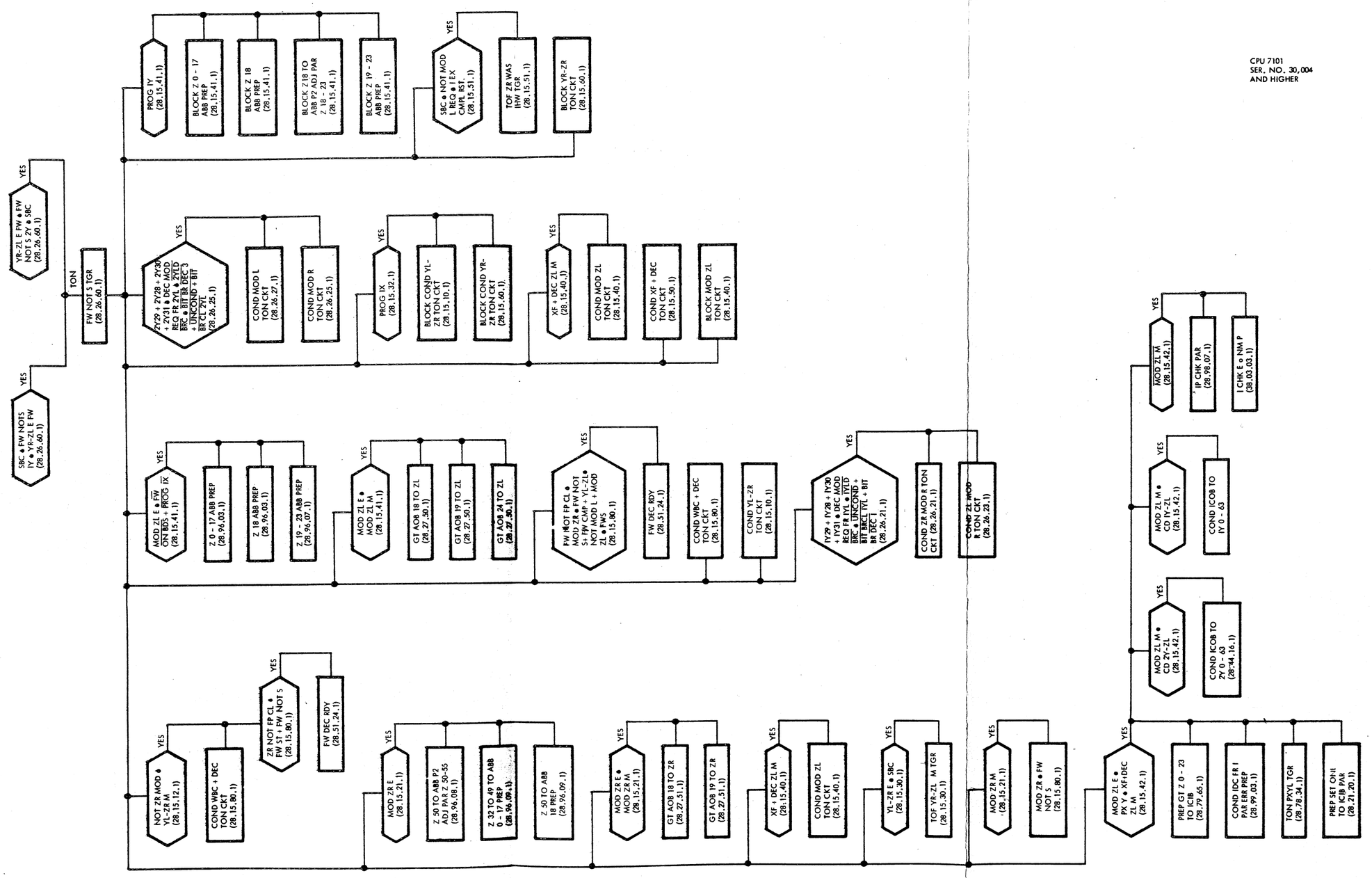
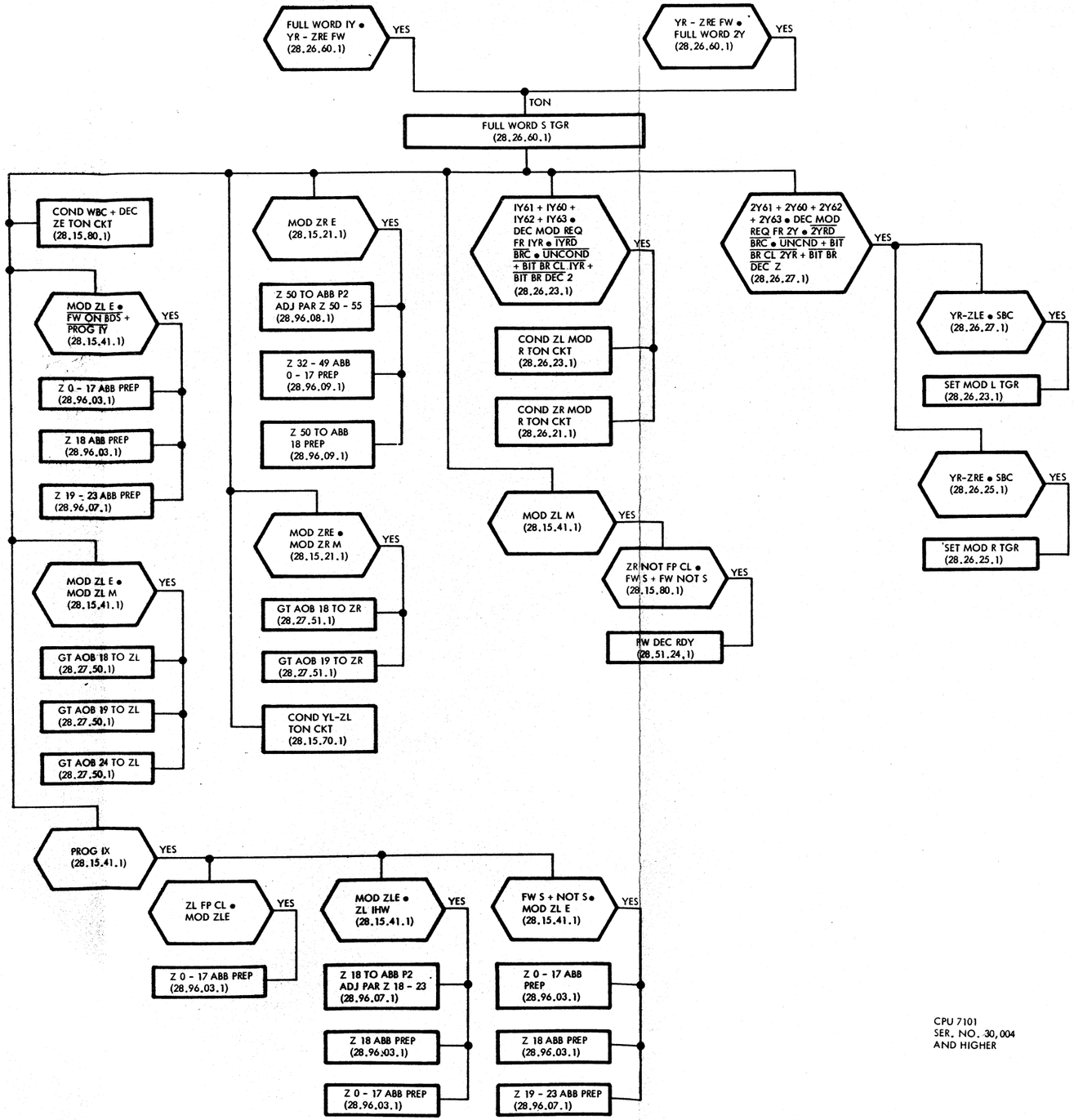


FIGURE 3.1.25. FW NOT S TRIGGER



CPU 7101
SER. NO. 30,004
AND HIGHER

FIGURE 3.1.26. FWS TRIGGER

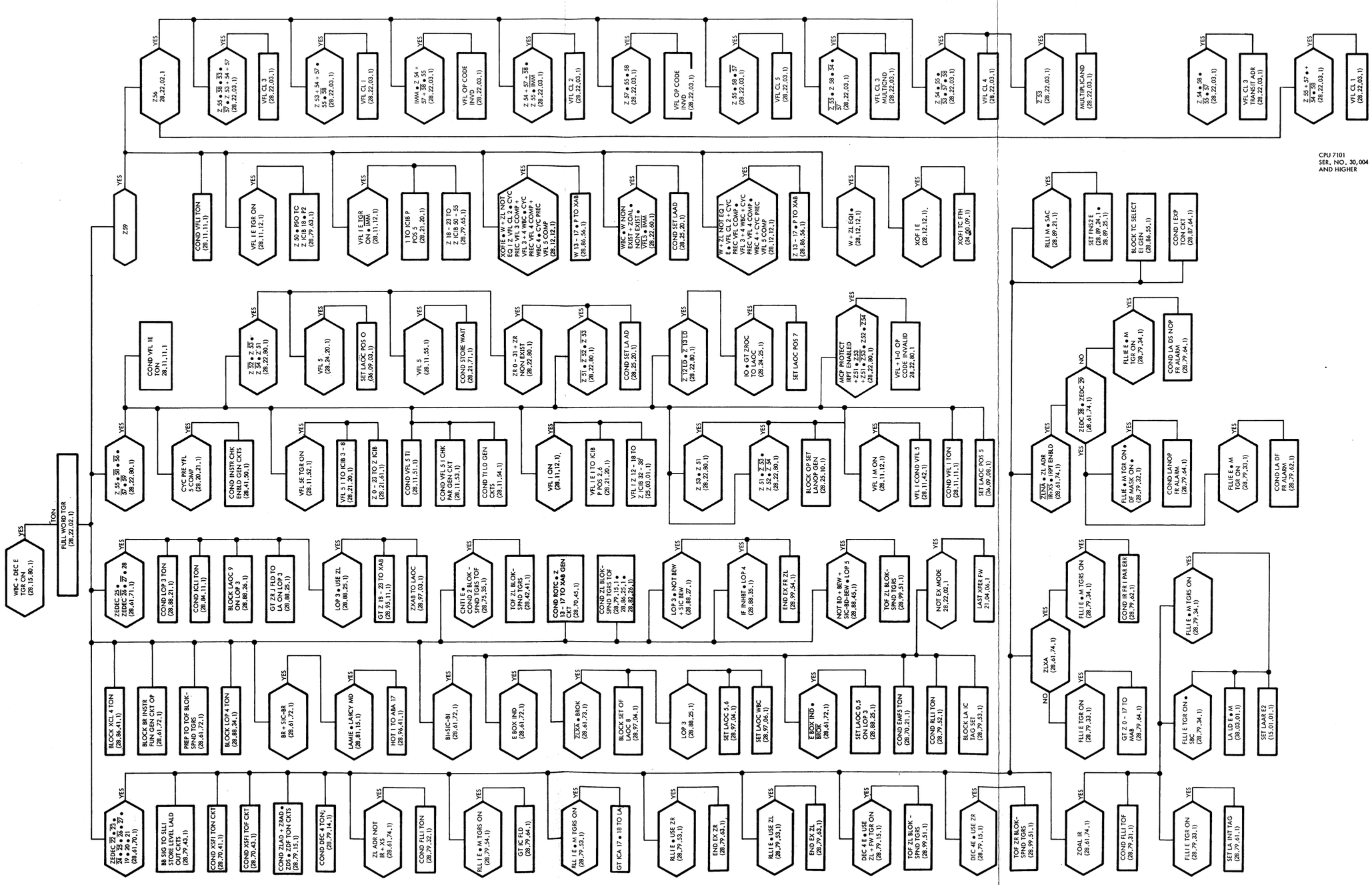


FIGURE 3.1.27. FW TRIGGER

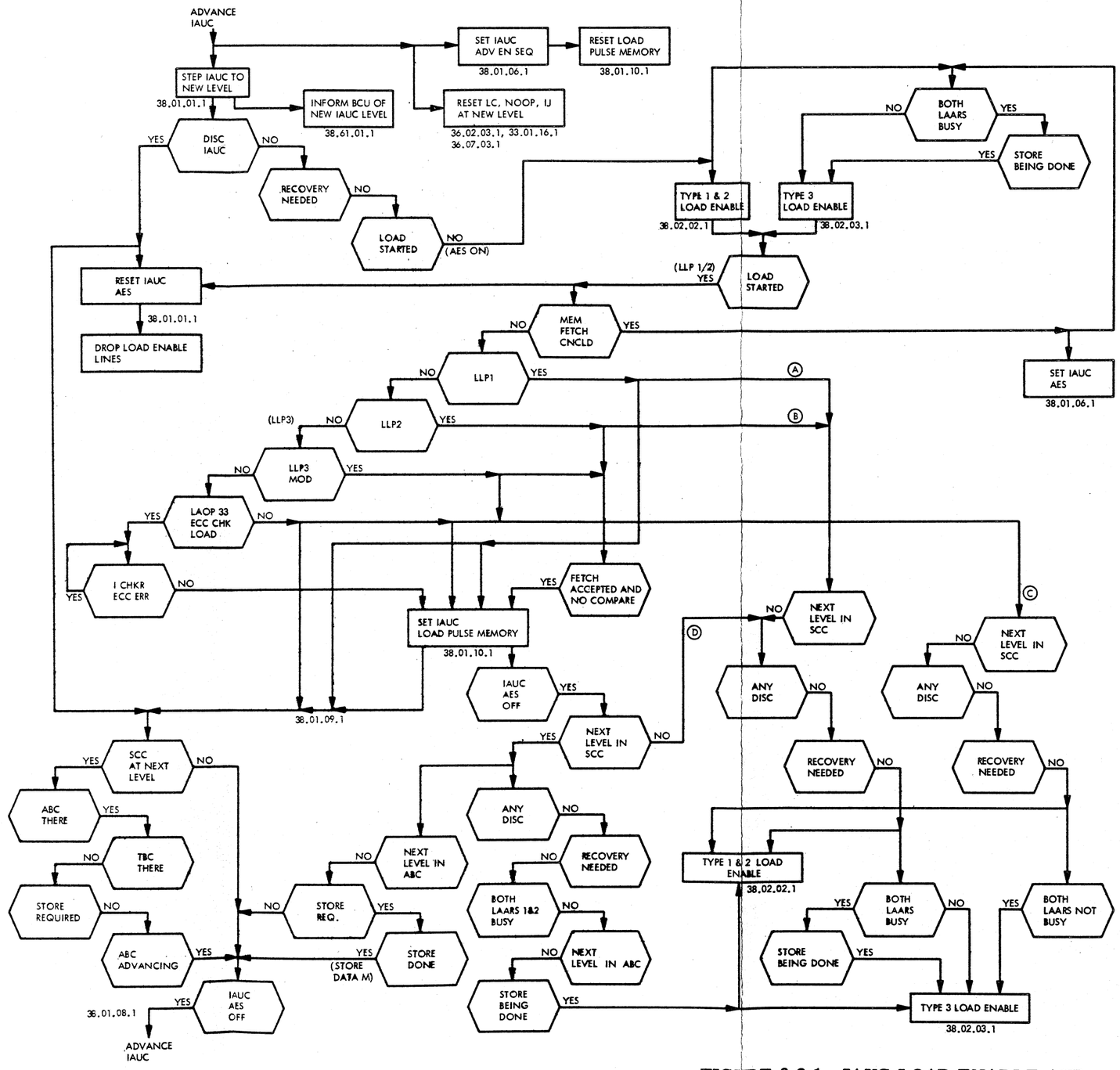


FIGURE 3.2.1. IAUC LOAD ENABLE AND ADVANCE CONDITIONS

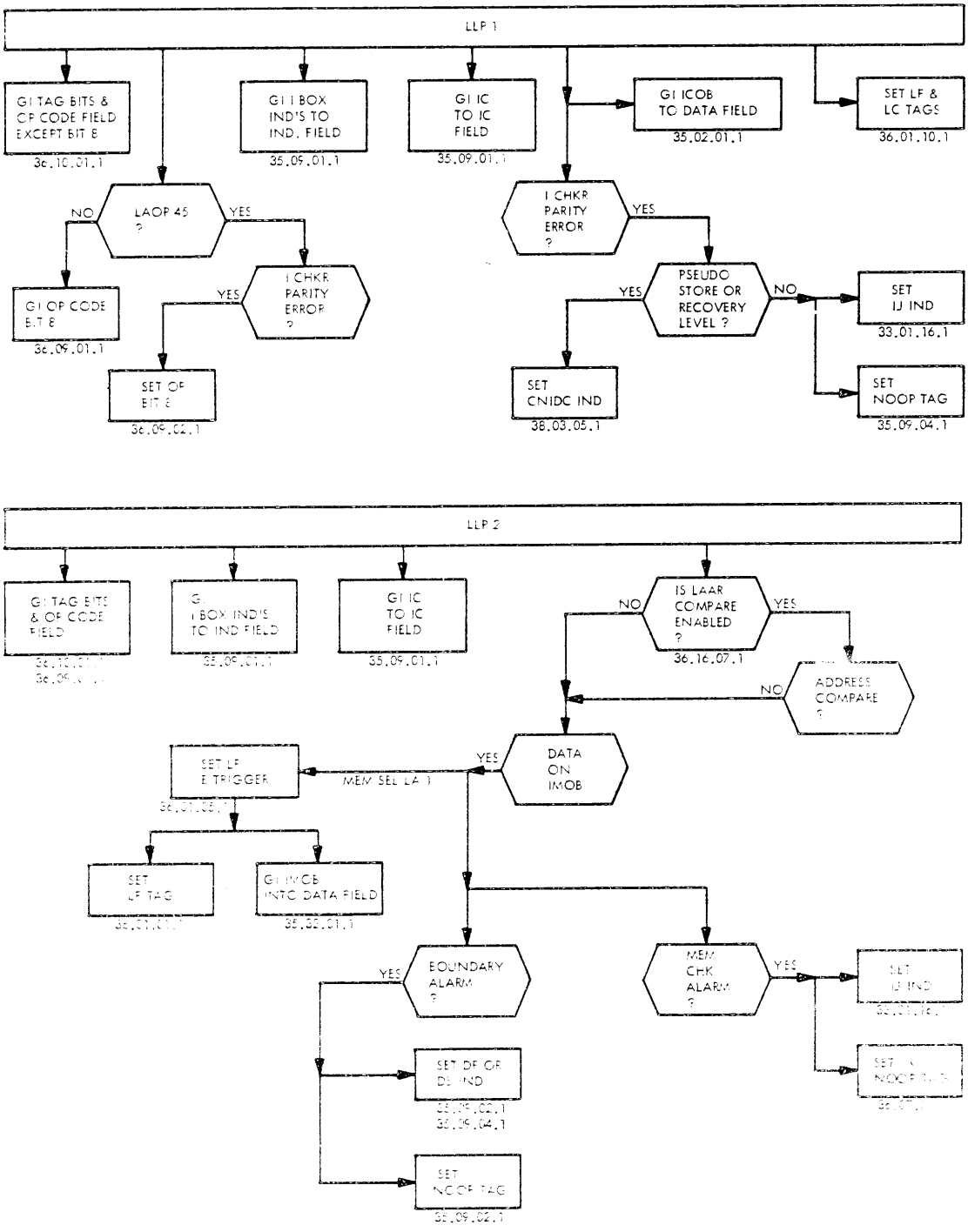


FIGURE 3.2.2. LOOKAHEAD LOAD PULSES (SHEET 1 OF 2)

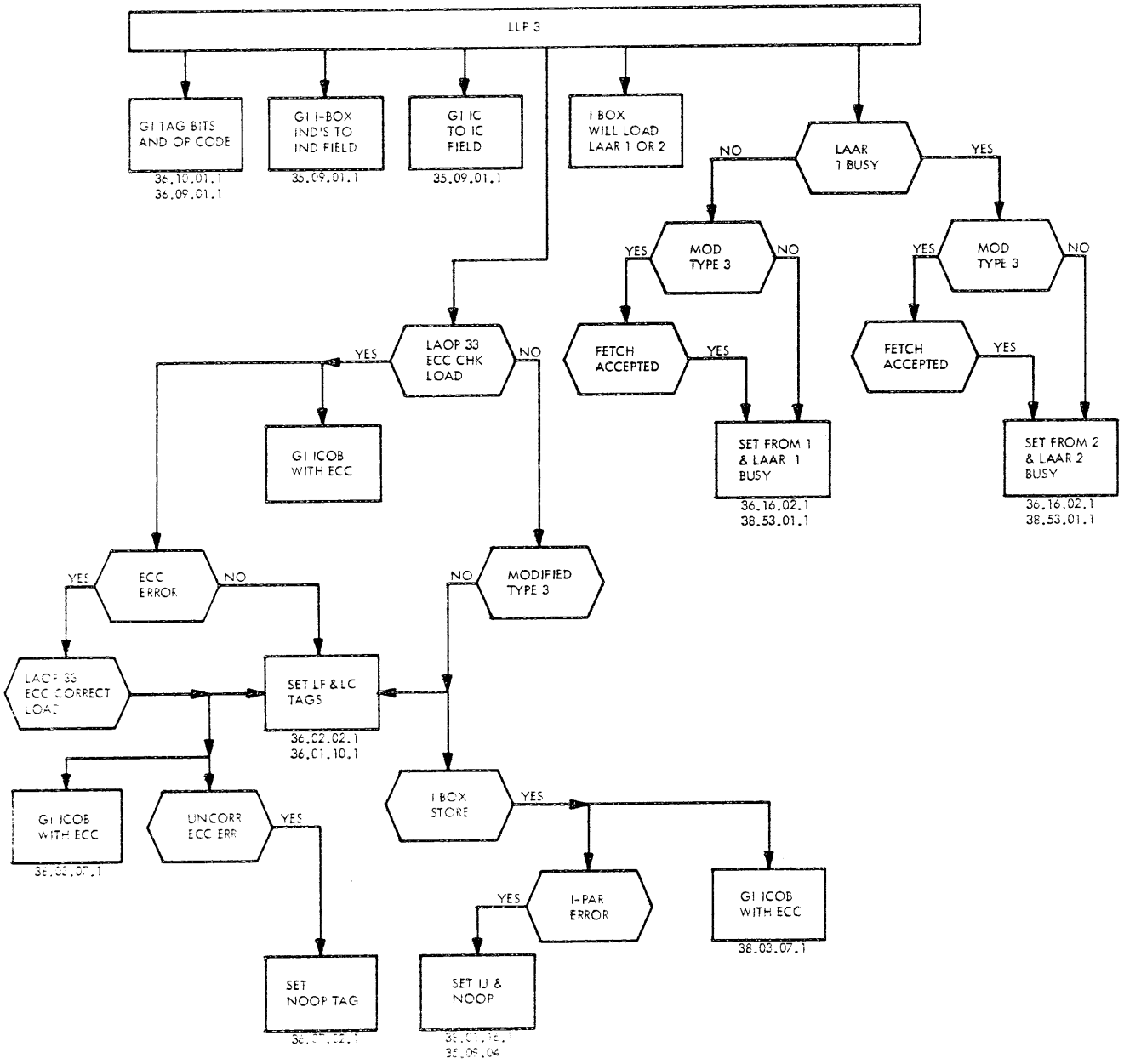


FIGURE 3.2.2. LOOKAHEAD LOAD PULSES (SHEET 2 OF 2)

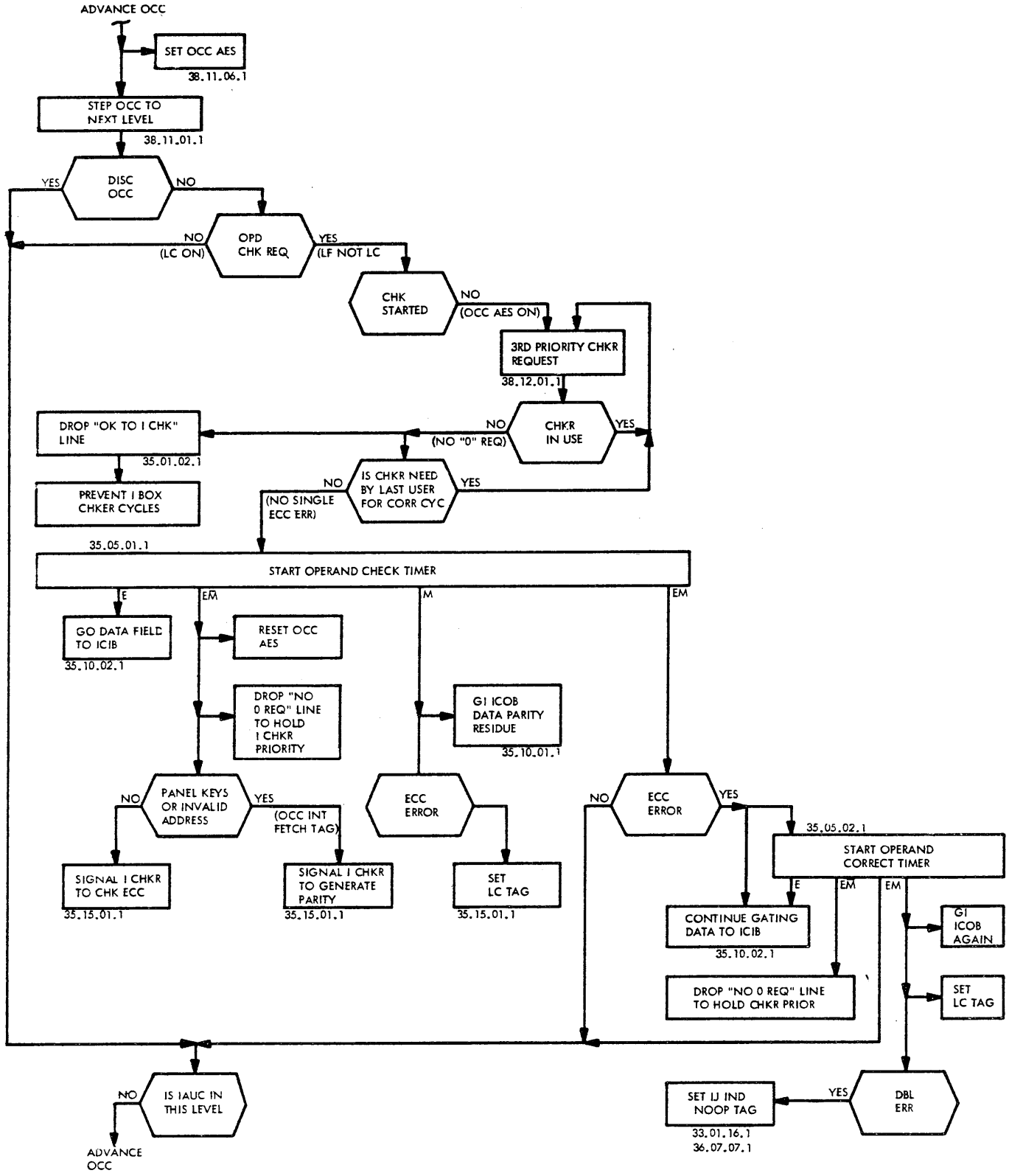


FIGURE 3.2.3. OPERAND CHECK AND CORRECT PHASE OF INSTRUCTION PREPARATION

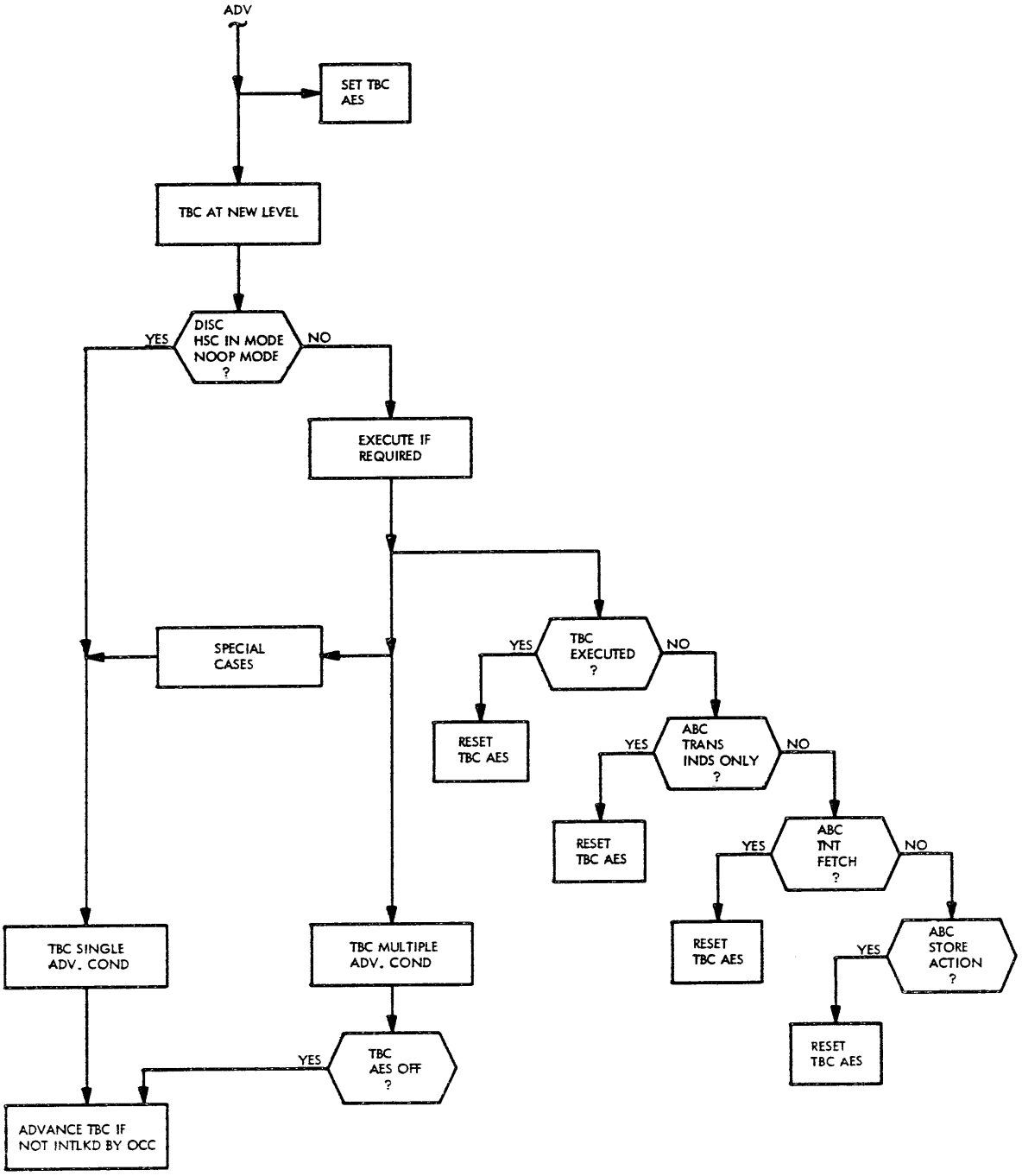


FIGURE 3.2.4. BASIC TBC ADVANCE CONDITIONS

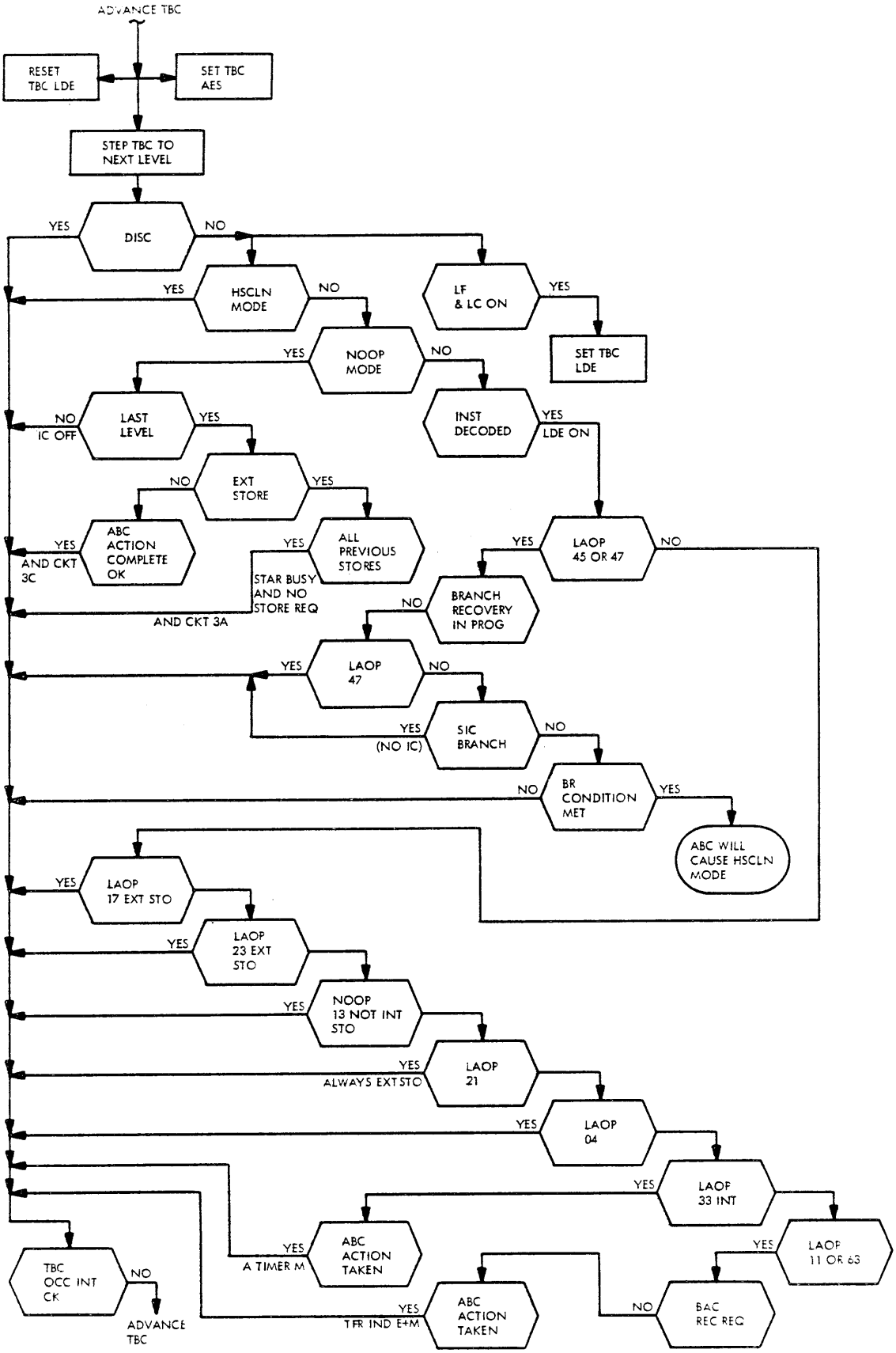


FIGURE 3.2.5. TBC SINGLE ADVANCE CONDITION

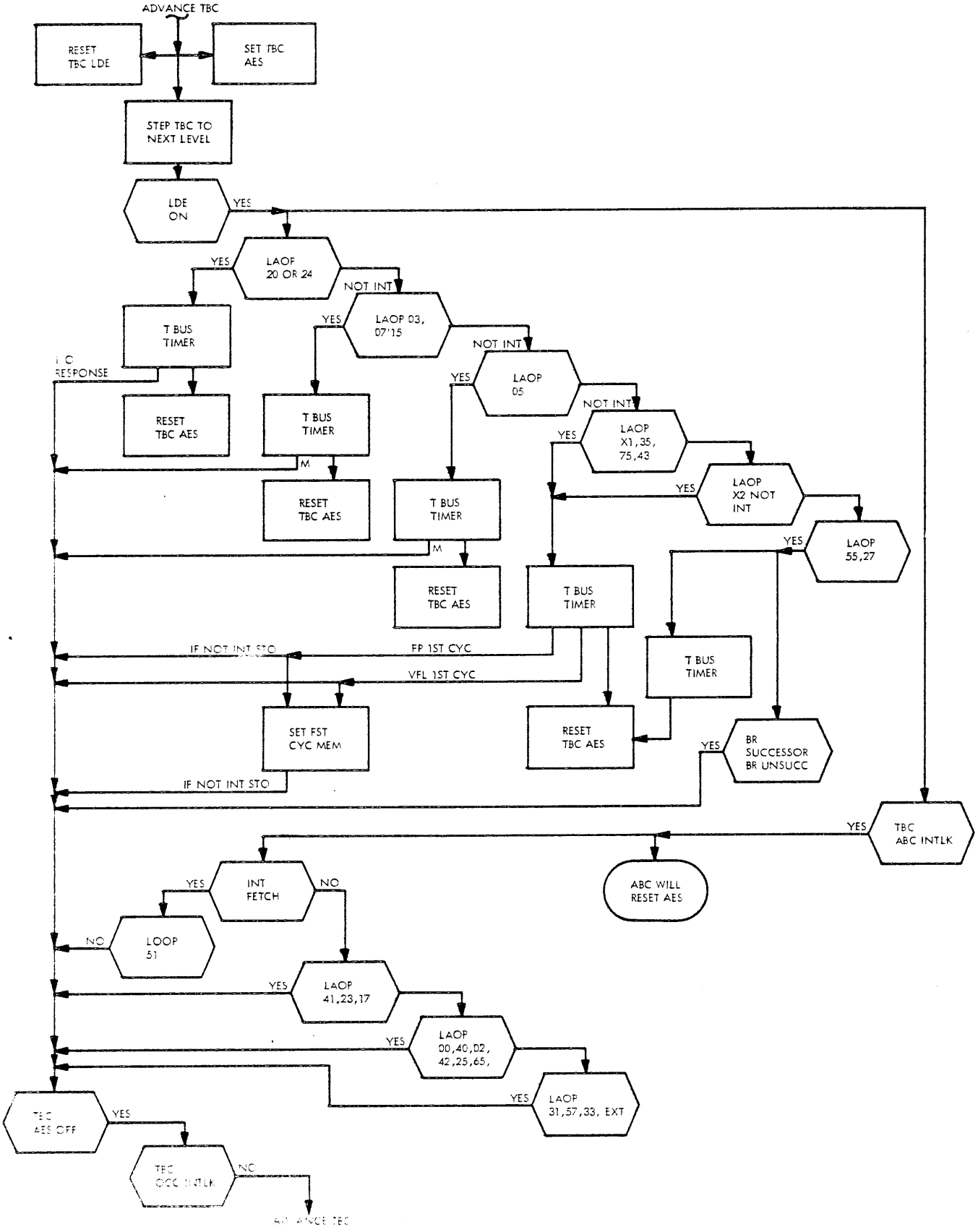


FIGURE 3.2.6. TBC MULTIPLE ADVANCE CONDITION

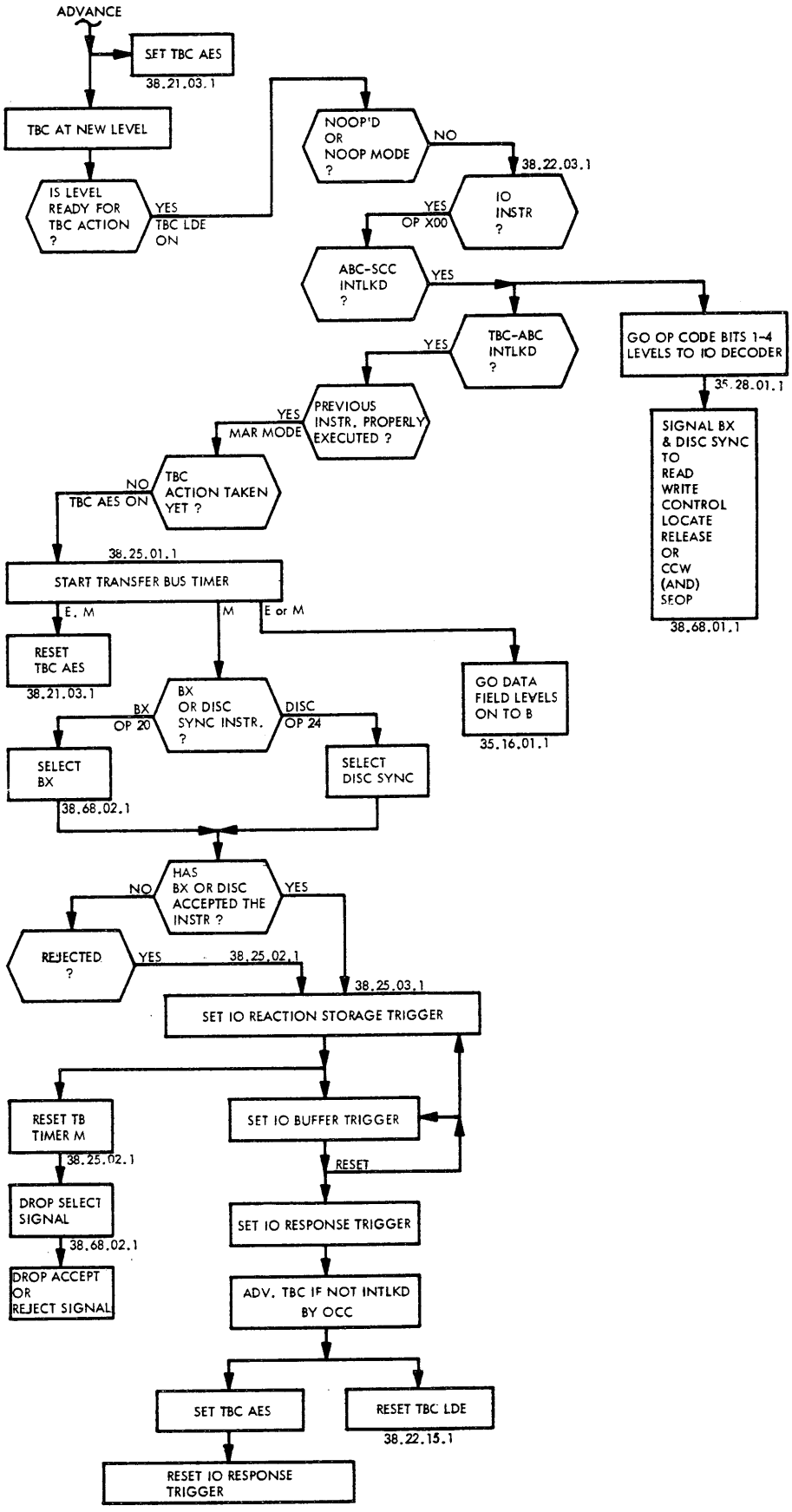


FIGURE 3.2.7. TBC I/O INSTRUCTIONS - OP 20 AND OP 24

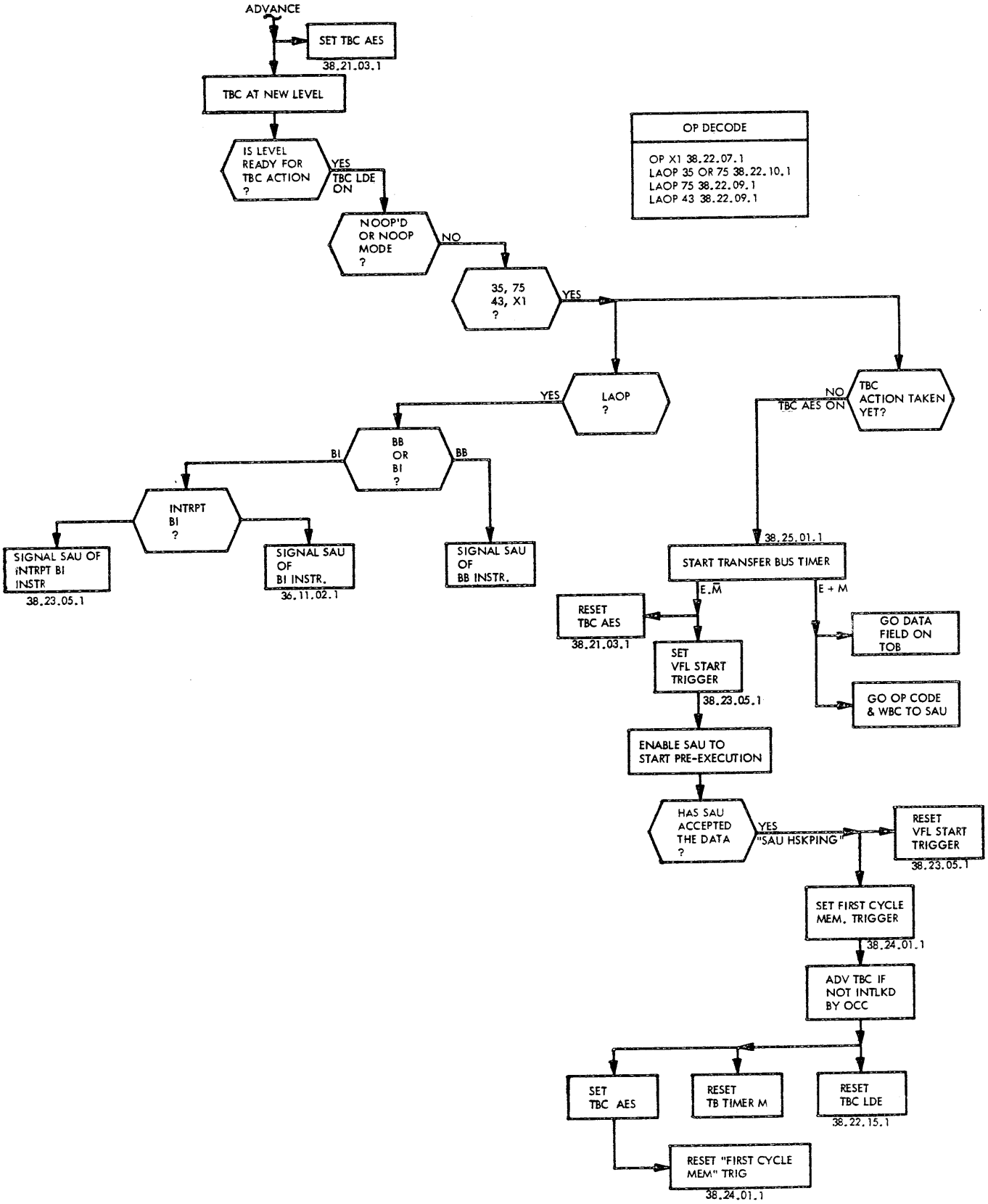


FIGURE 3.2.8. FIRST LEVEL OF SAU INSTRUCTIONS

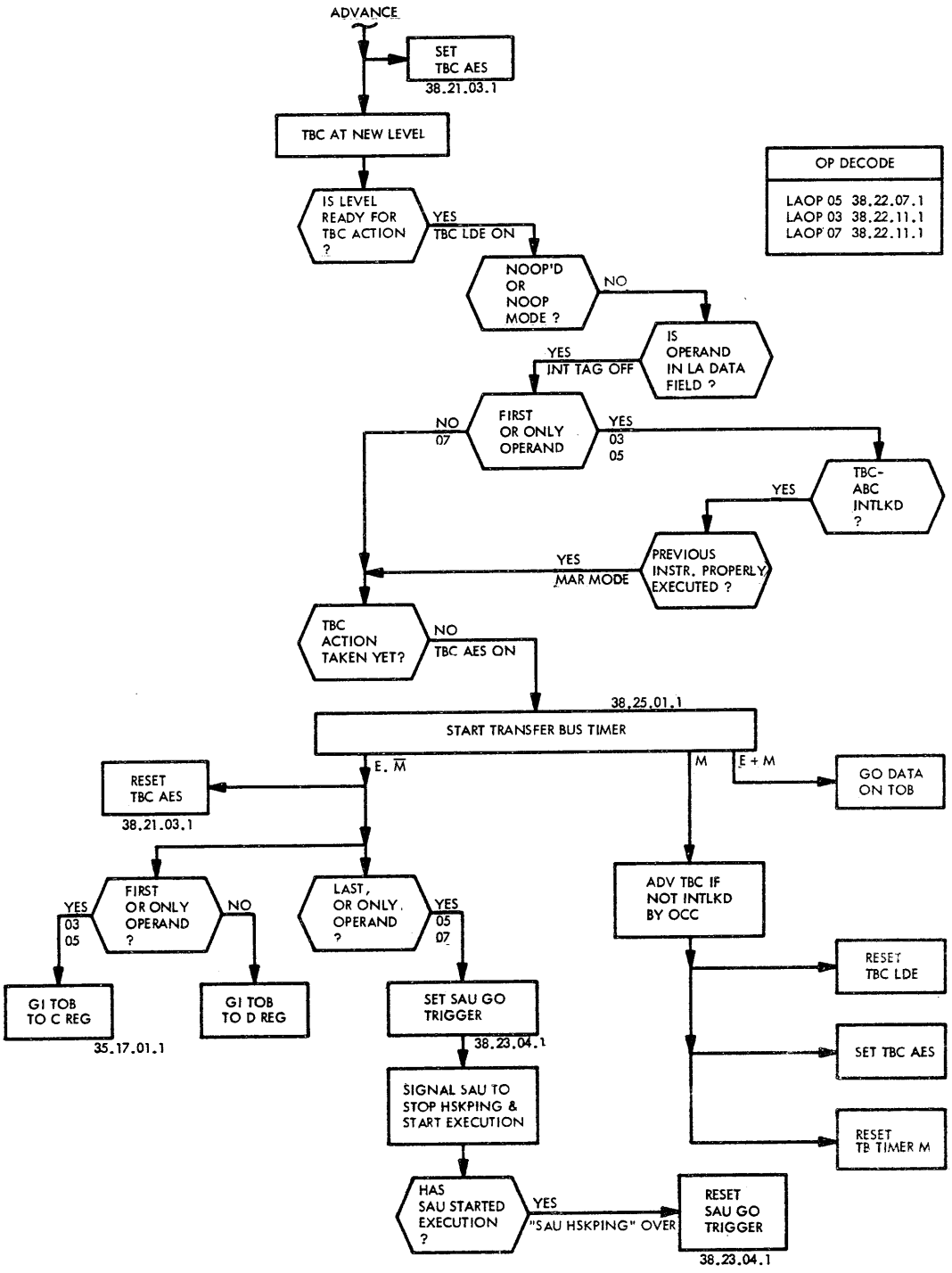


FIGURE 3.2.9. VFL OPERANDS LAOP 03, 05, AND 07

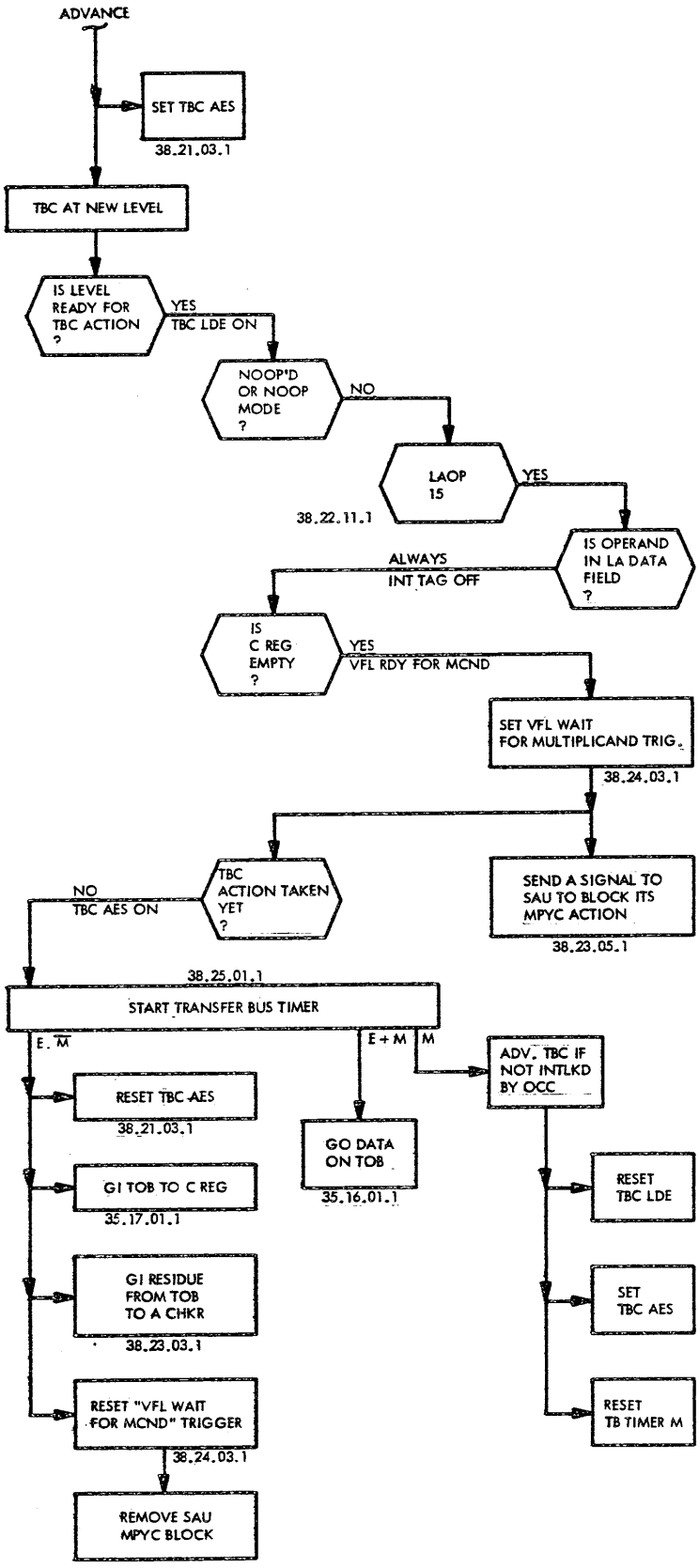


FIGURE 3.2.10. VFL SPECIAL OPERAND LAOP 15

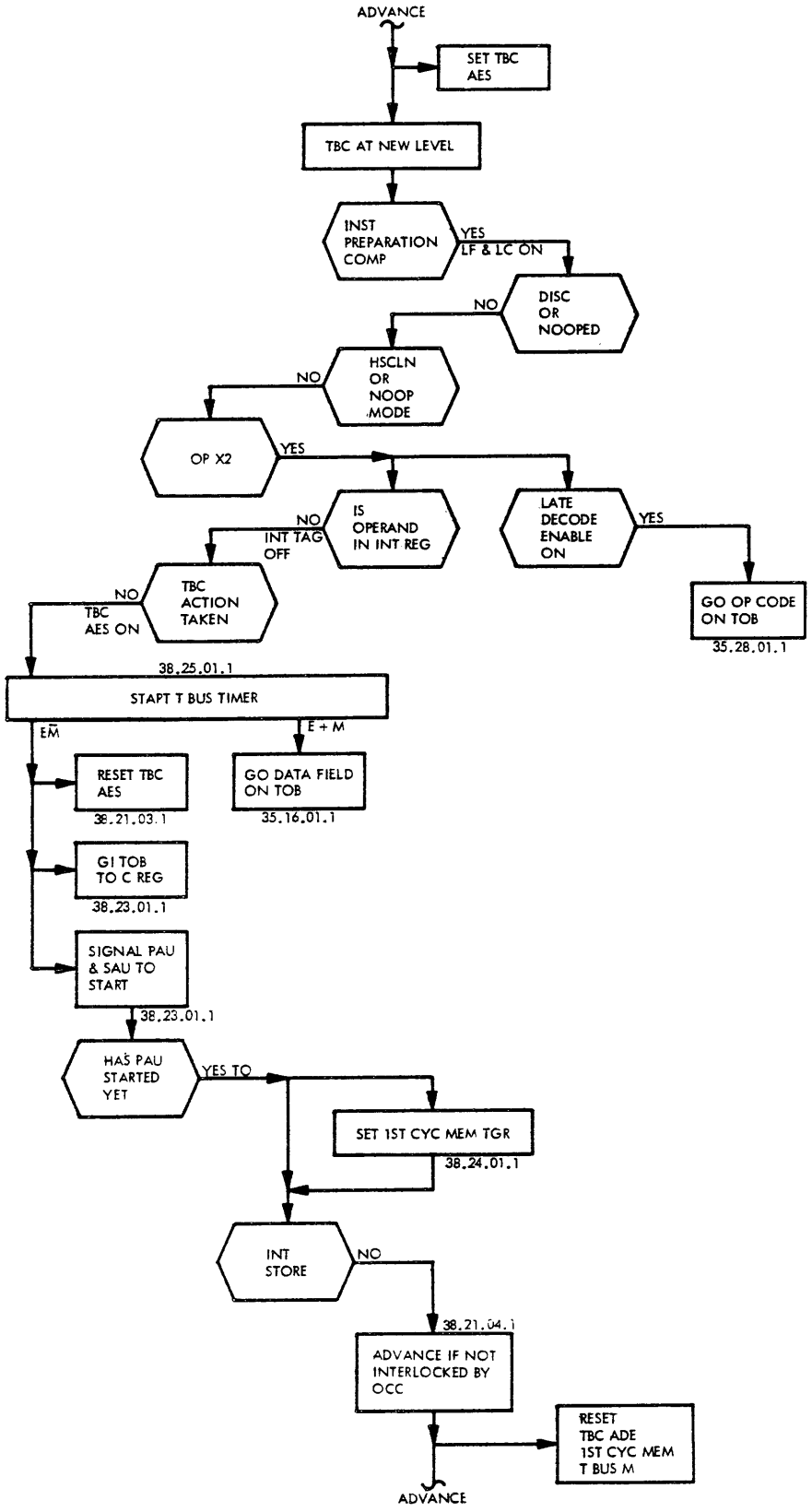


FIGURE 3.2.11. FP INSTRUCTION LEVEL OPX2

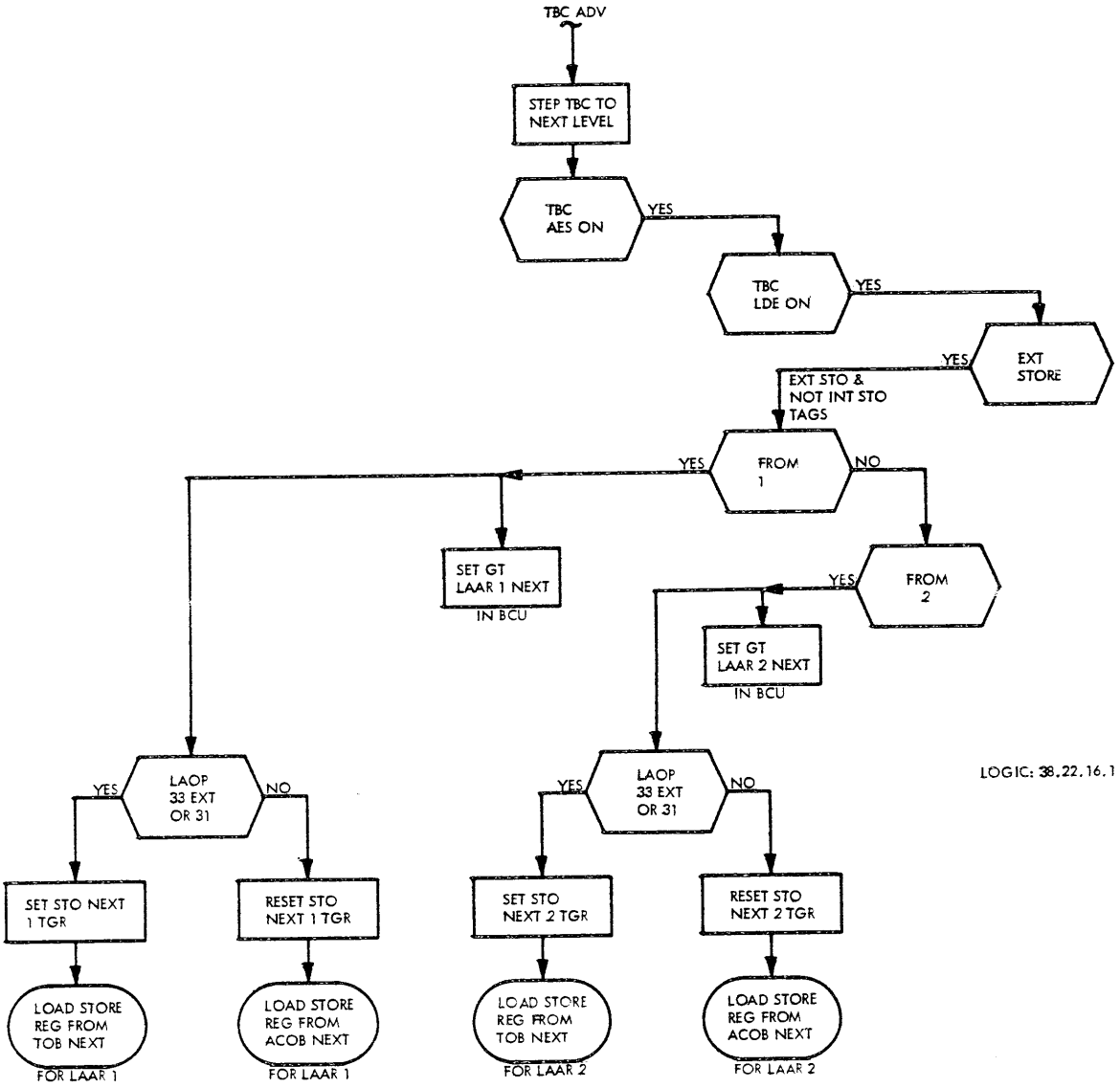


FIGURE 3.2.12. TBC STORE GATE CONTROL

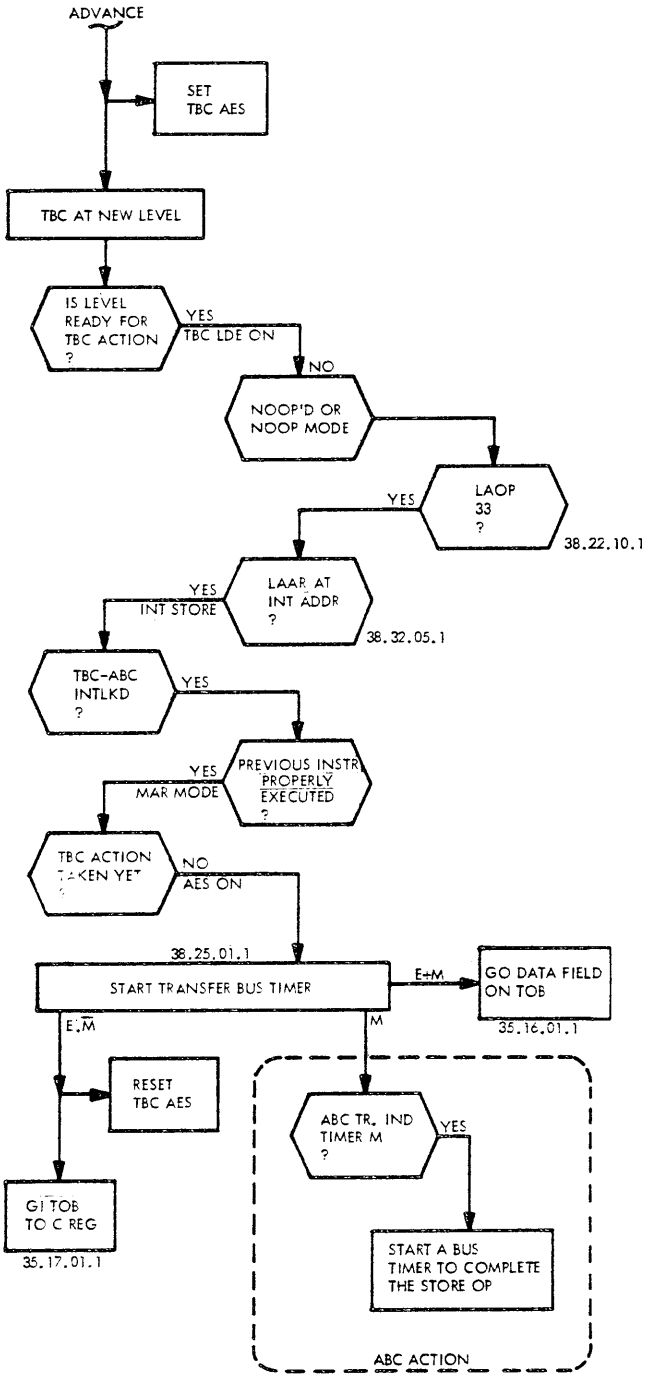


FIGURE 3.2.13. I BOX STORE TO INTERNAL ADDRESS, LAOP 33

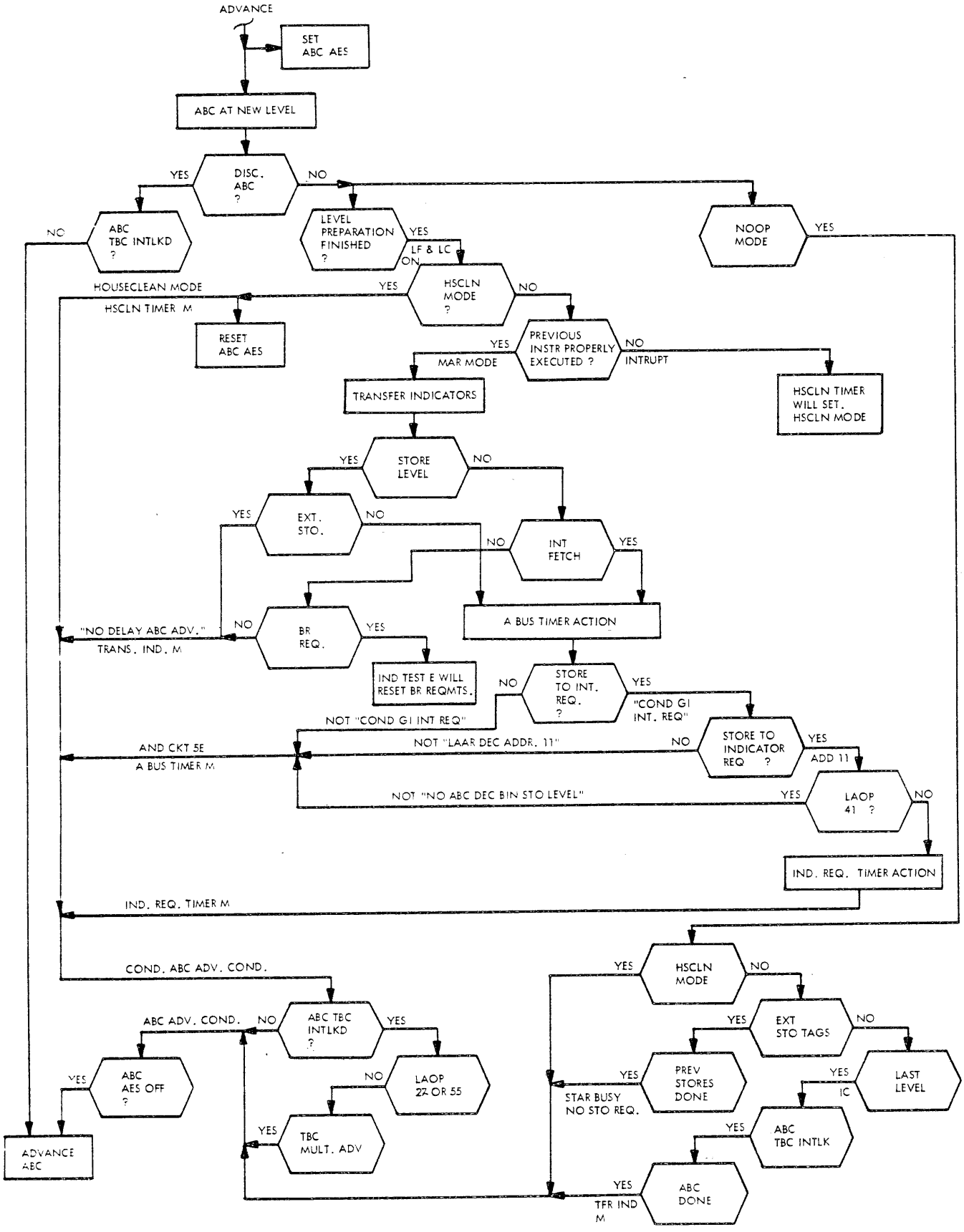


FIGURE 3.2.14. ABC ADVANCE

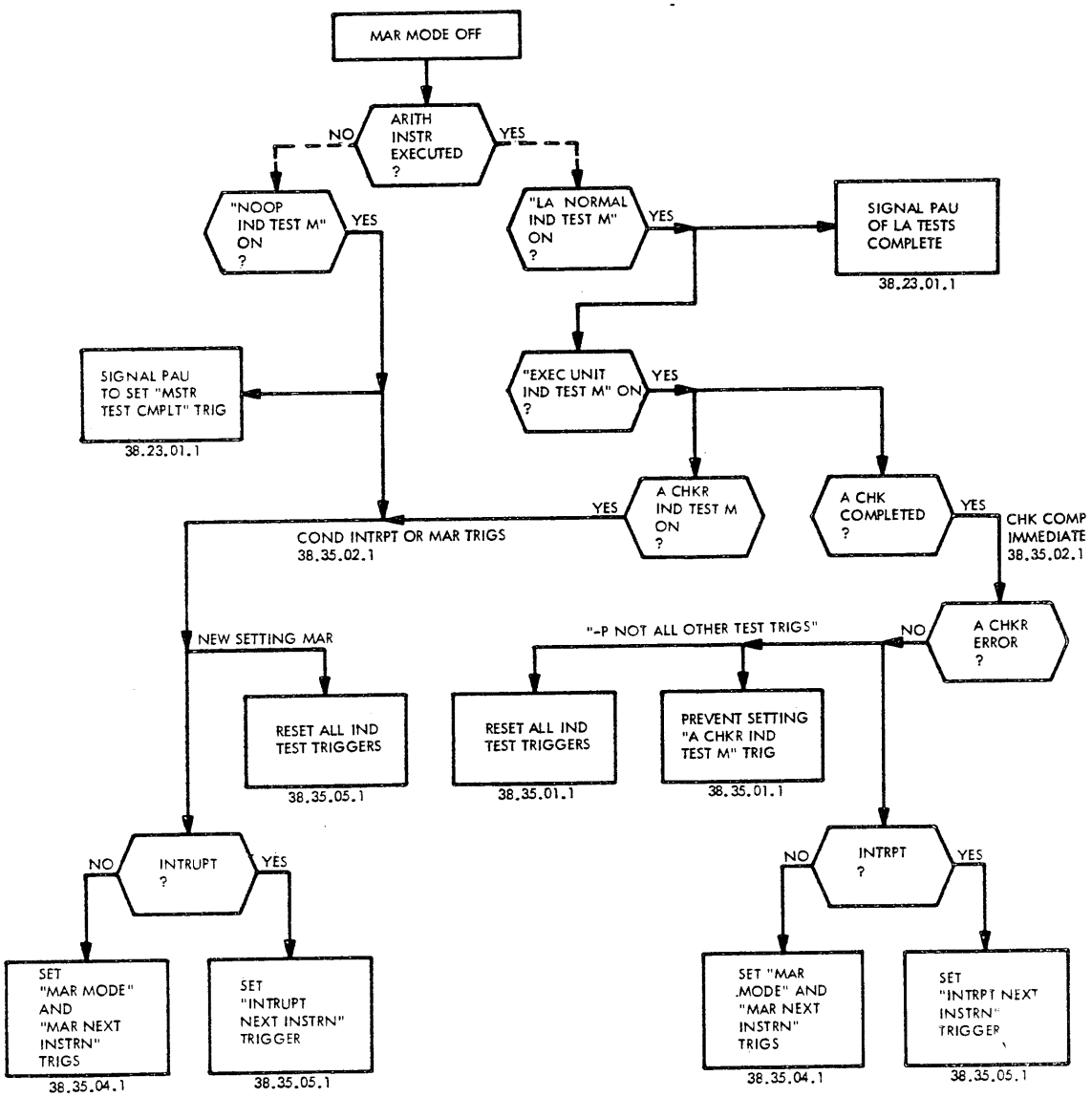


FIGURE 3.2.15. SETTING MAR MODE

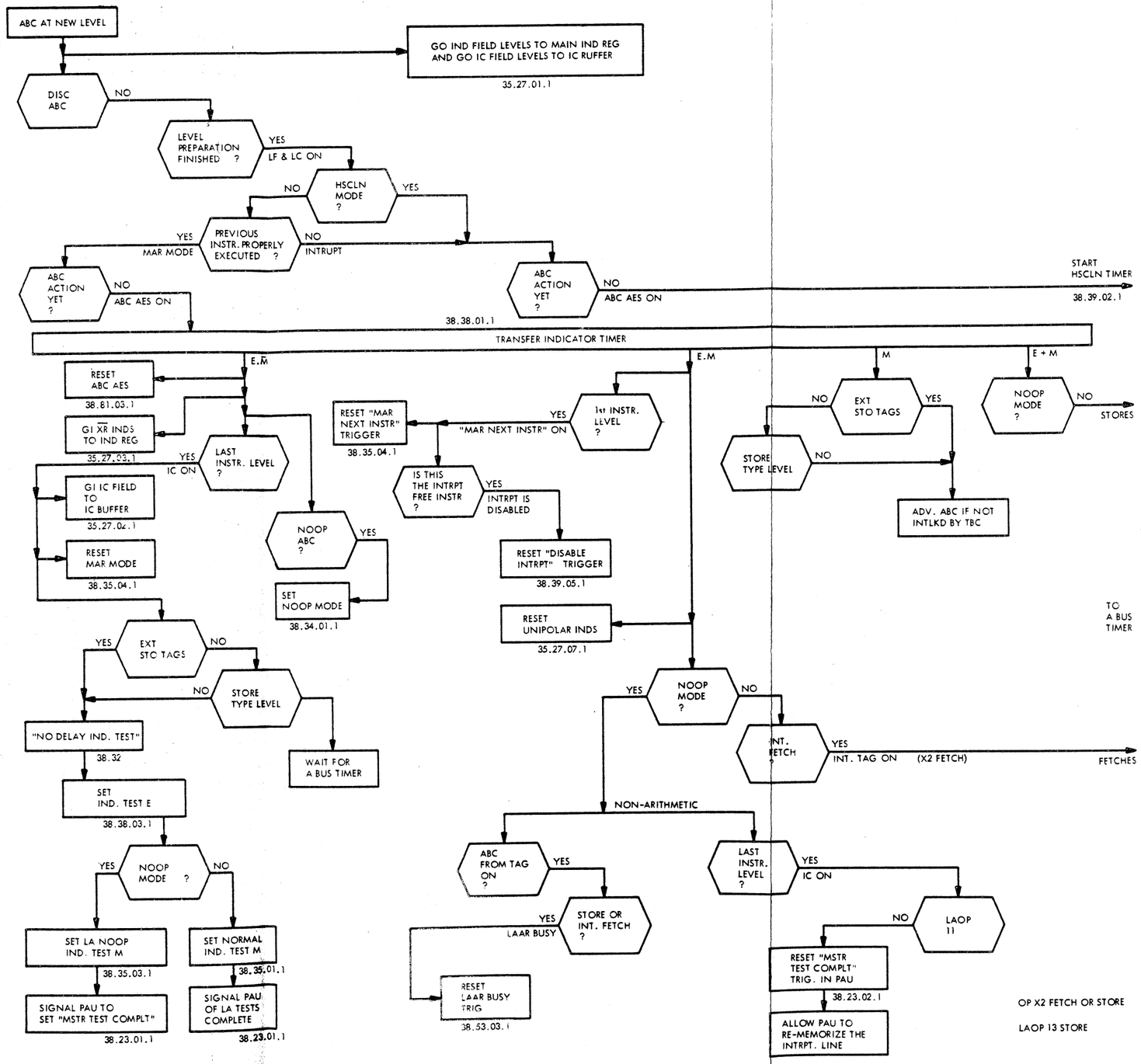


FIGURE 3.2.16. FP ABC ACTIONS-TRANSFER INDICATOR TIMER

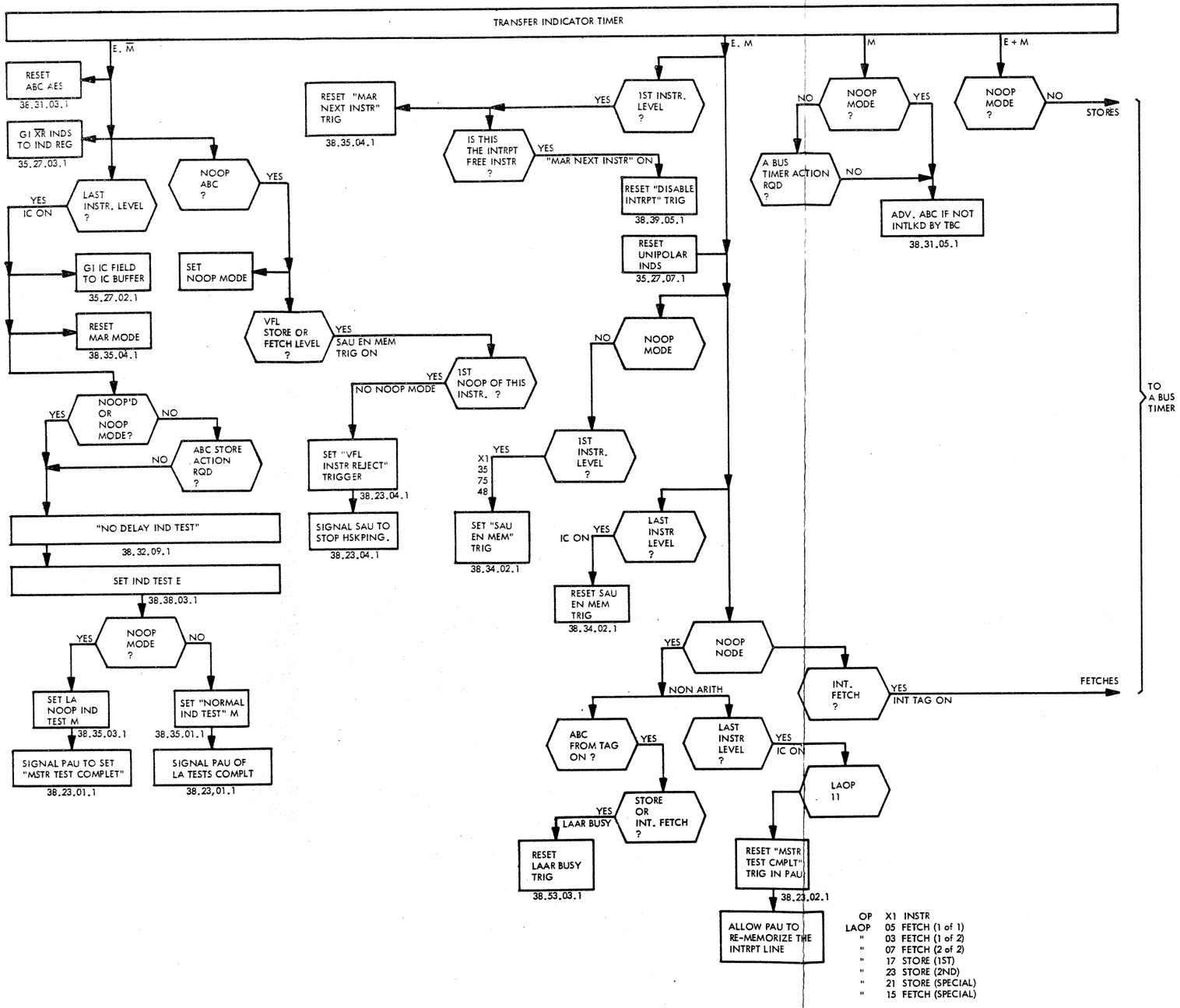


FIGURE 3.2.17. VFL ABC ACTIONS-TRANSFER INDICATOR TIMER

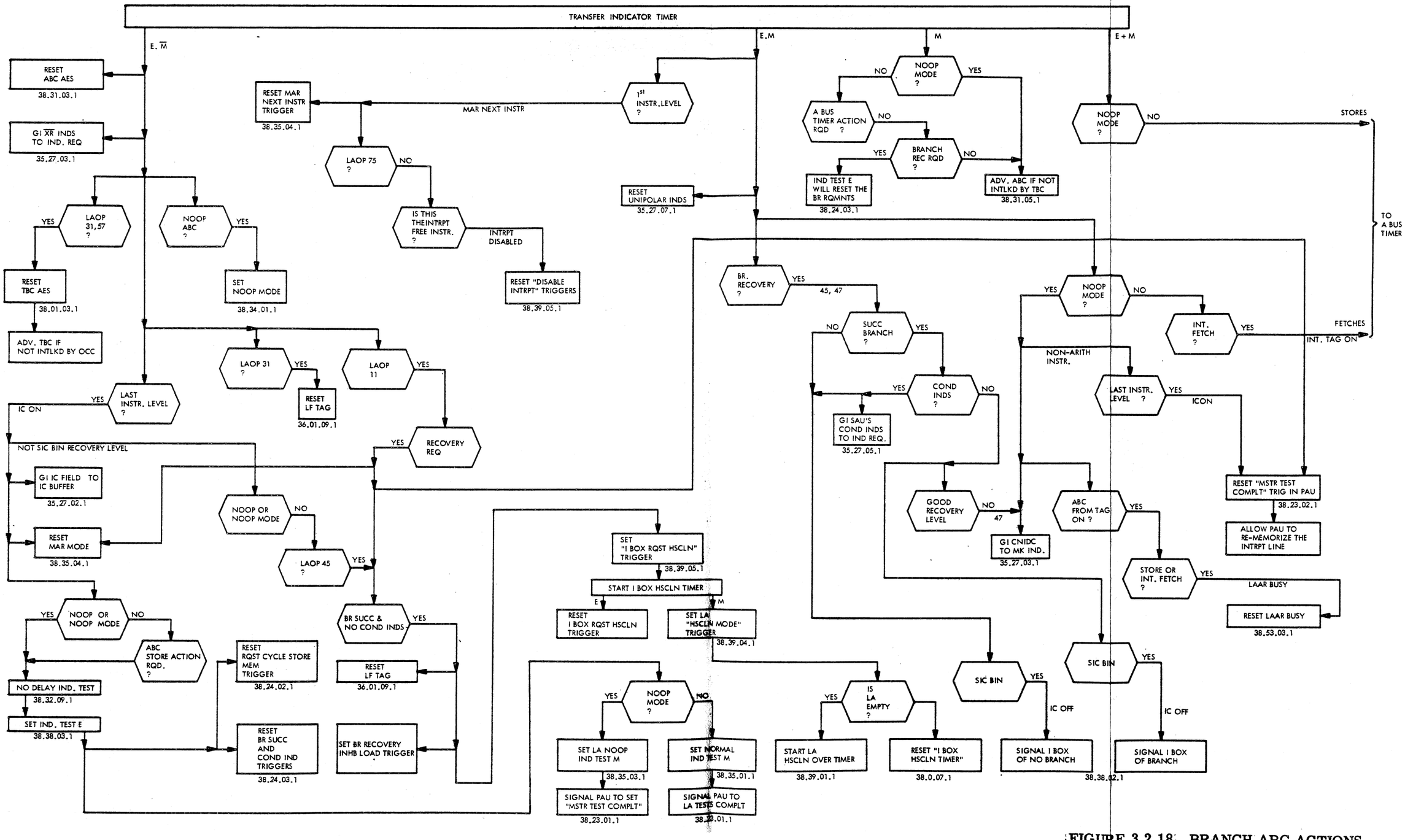
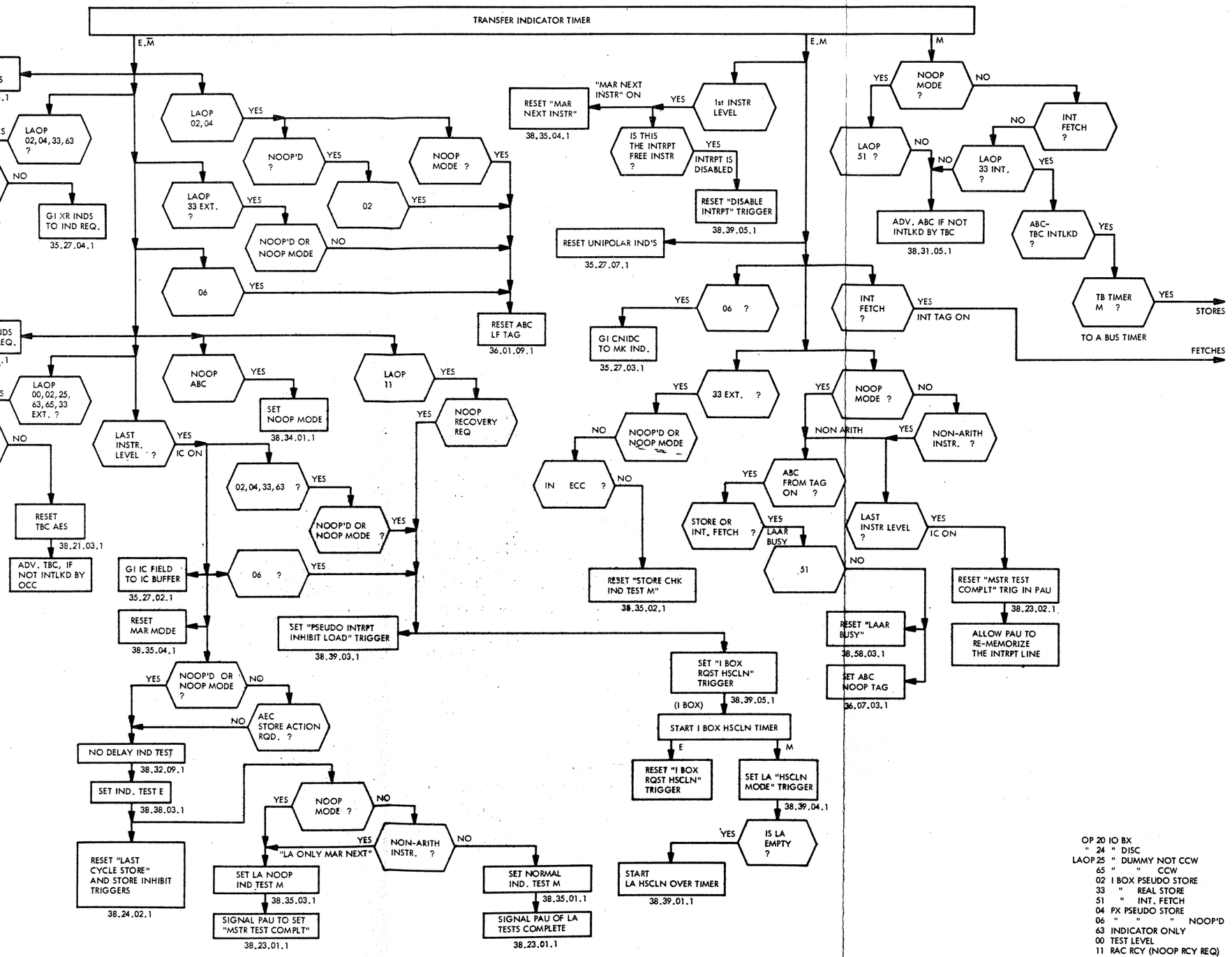


FIGURE 3.2.18. BRANCH ABC ACTIONS-TRANSFER INDICATOR TIMER



OP 20 IO BX
" 24 " DISC
LAOP 25 " DUMMY NOT CCW
65 " " CCW
02 I BOX PSEUDO STORE
33 " REAL STORE
51 " INT. FETCH
04 PX PSEUDO STORE
06 " " " NOOP'D
63 INDICATOR ONLY
00 TEST LEVEL
11 RAC RCY (NOOP RCY REQ)

FIGURE 3.2.19. I BOX AND I/O ABC ACTIONS-TRANSFER INDICATOR TIMER

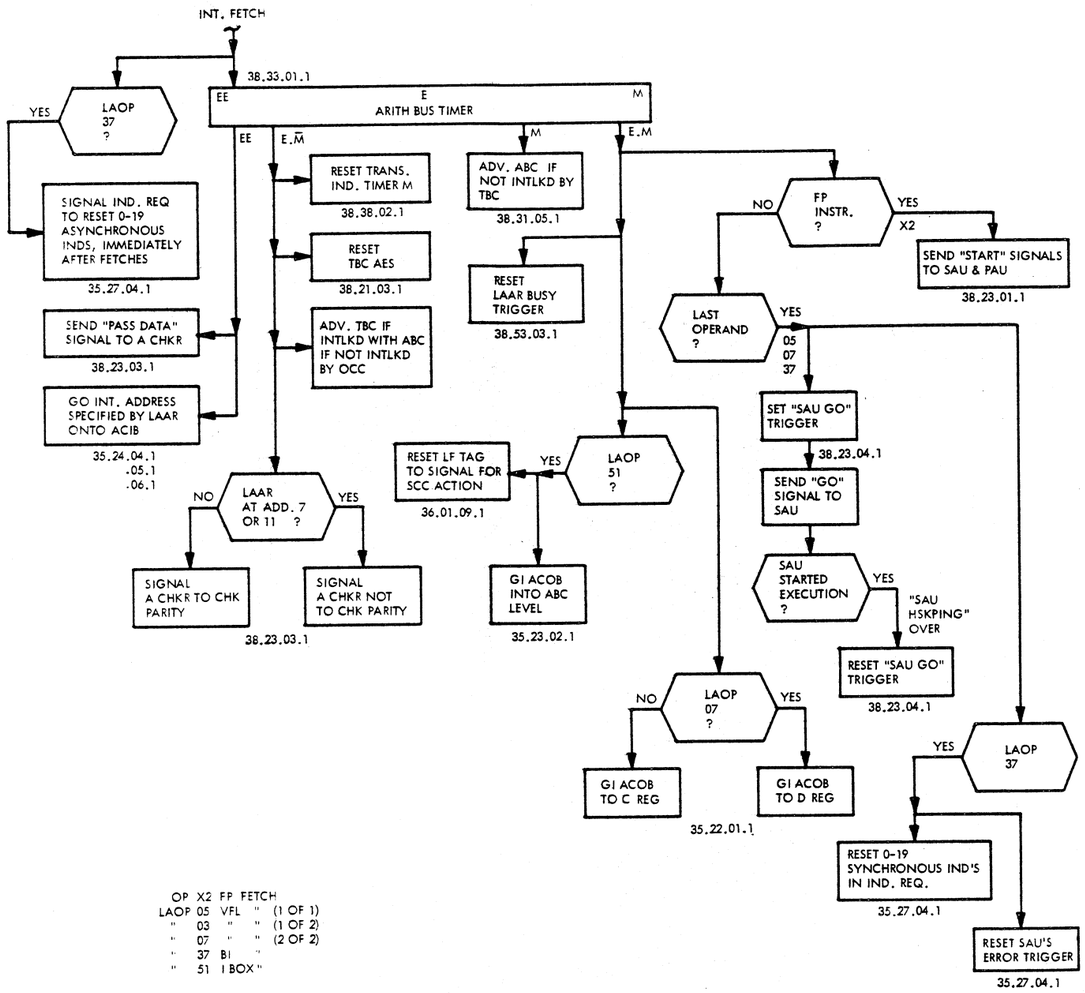


FIGURE 3.2.20. INTERNAL FETCH ABC ACTIONS-ARITHMETIC BUS TIMER

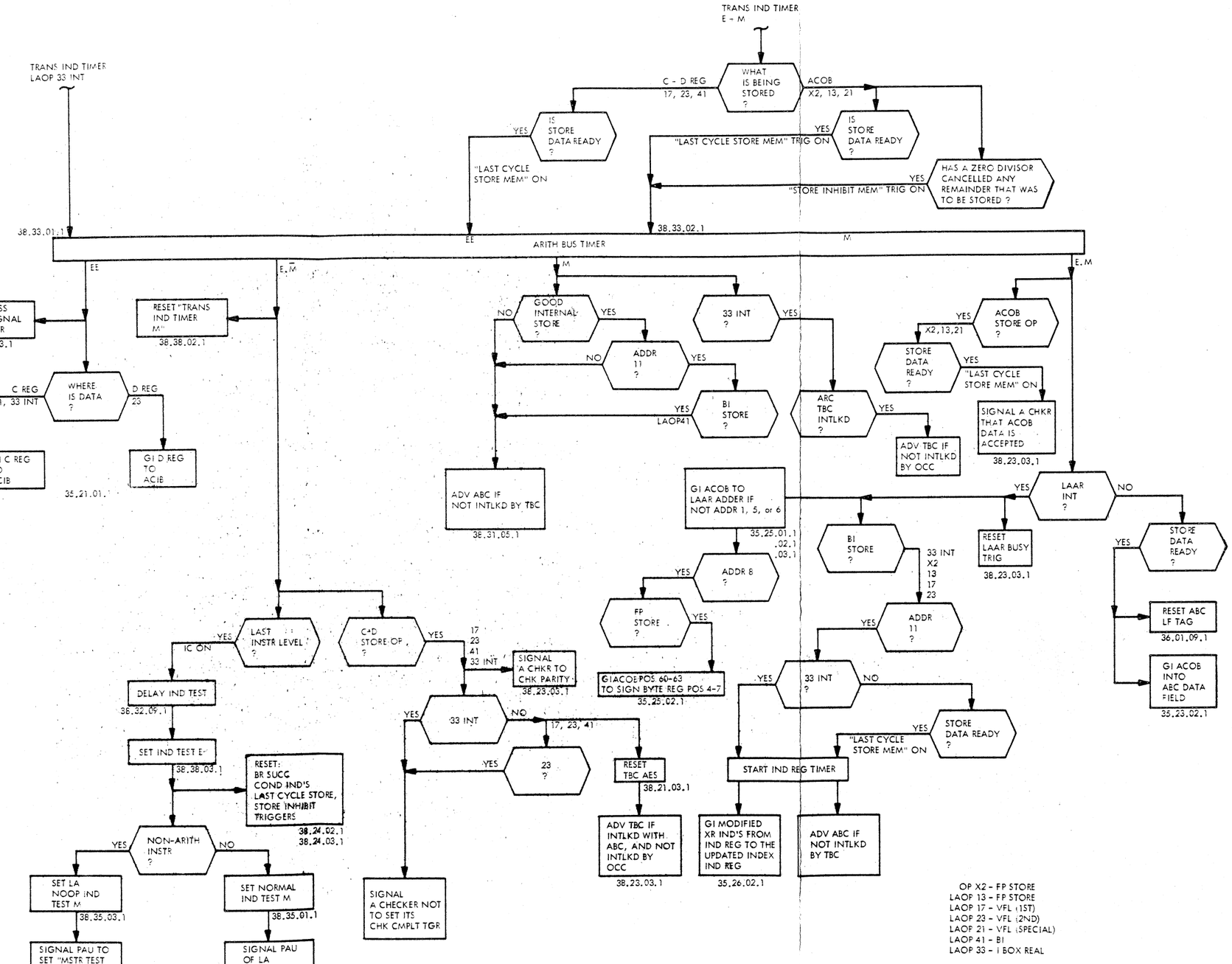


FIGURE 3.2.21. STORE ABC ACTIONS-ARITHMETIC BUS TIMER

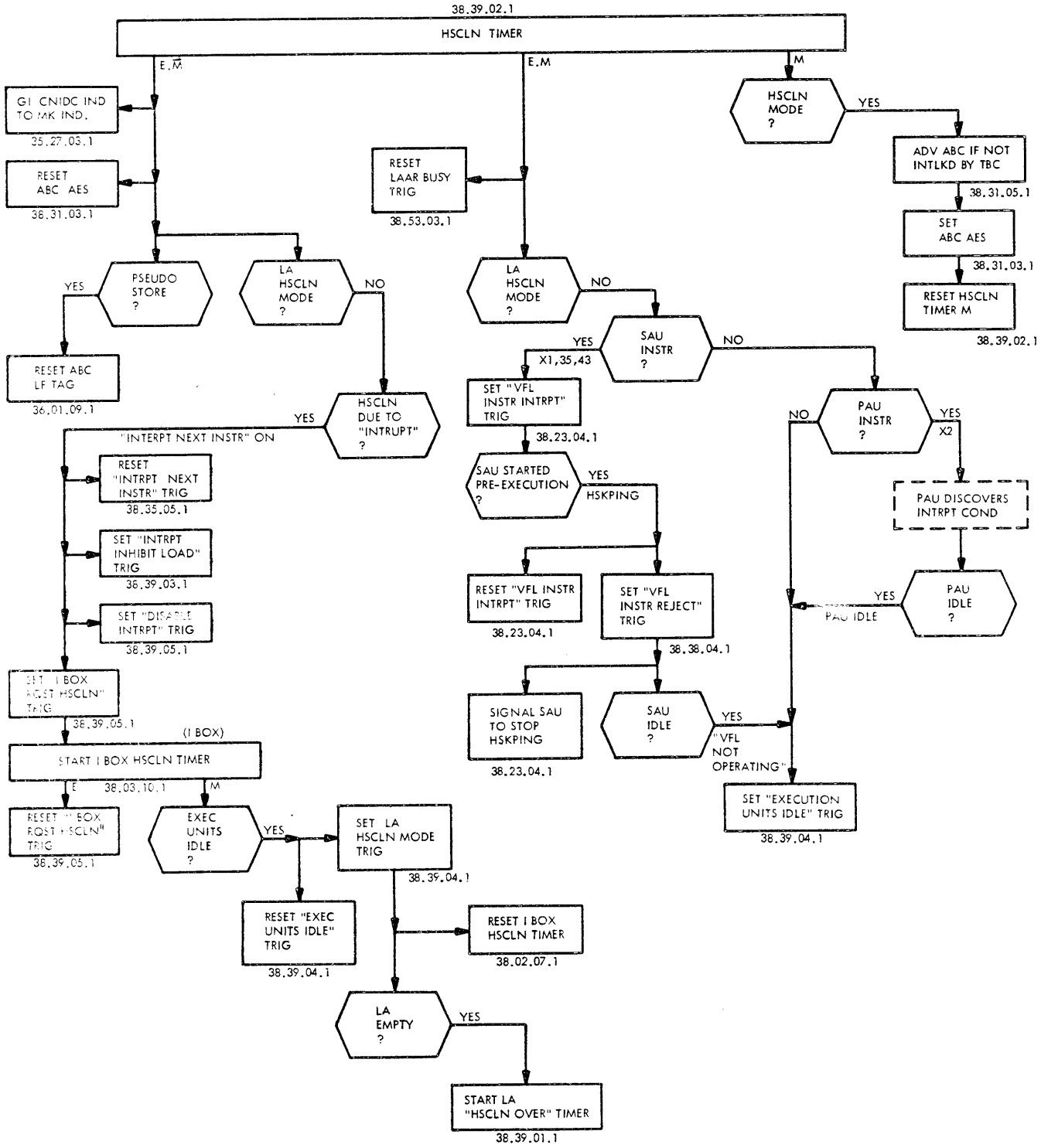


FIGURE 3.2.22. LA HOUSECLEAN TIMER

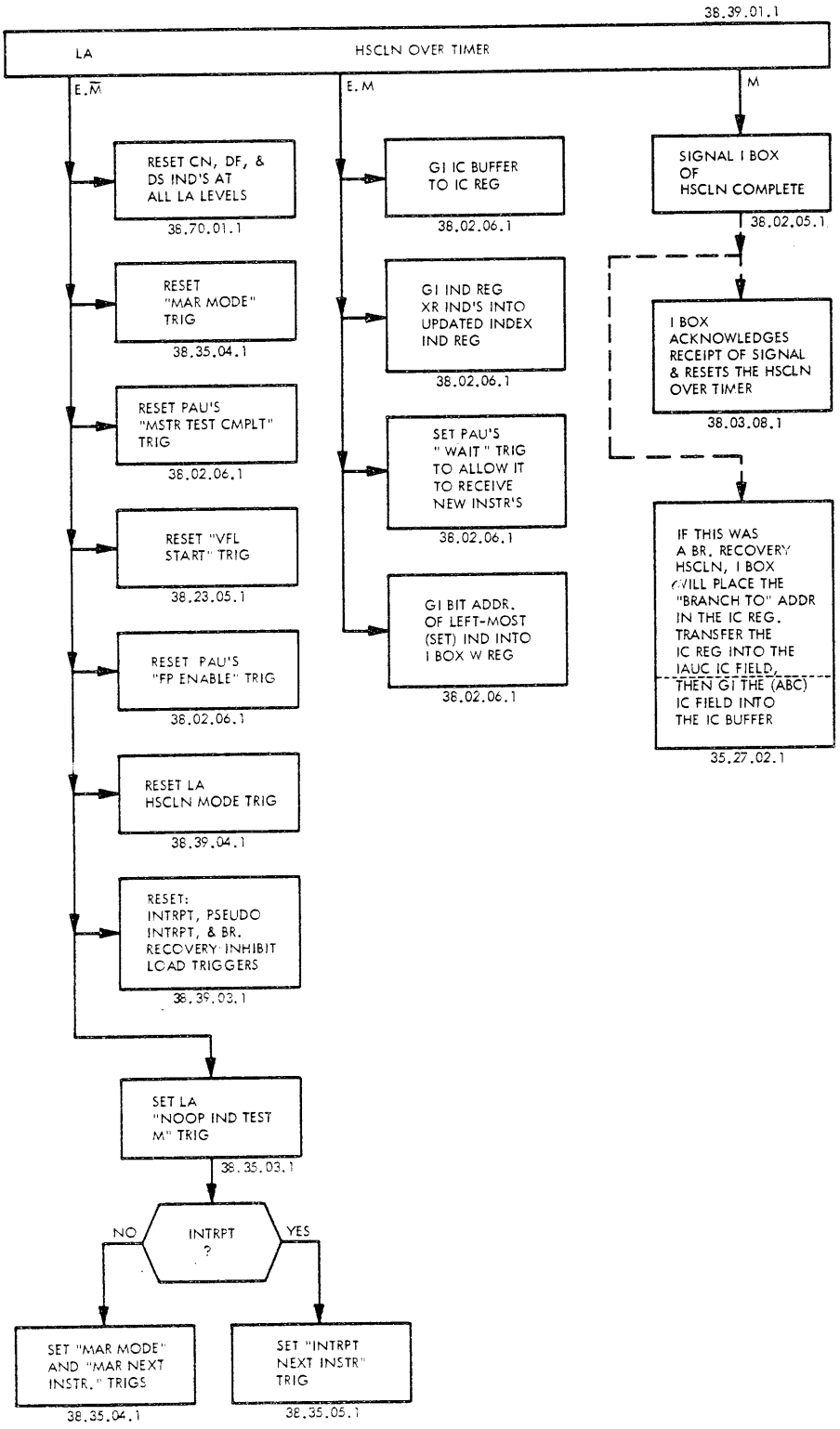
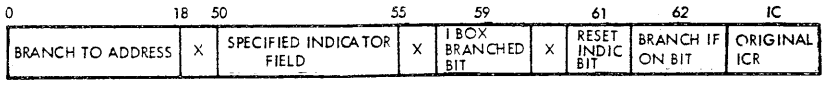


FIGURE 3.2.23. LA HOUSECLEAN OVER TIMER

BAC LOOK AHEAD DATA FIELD



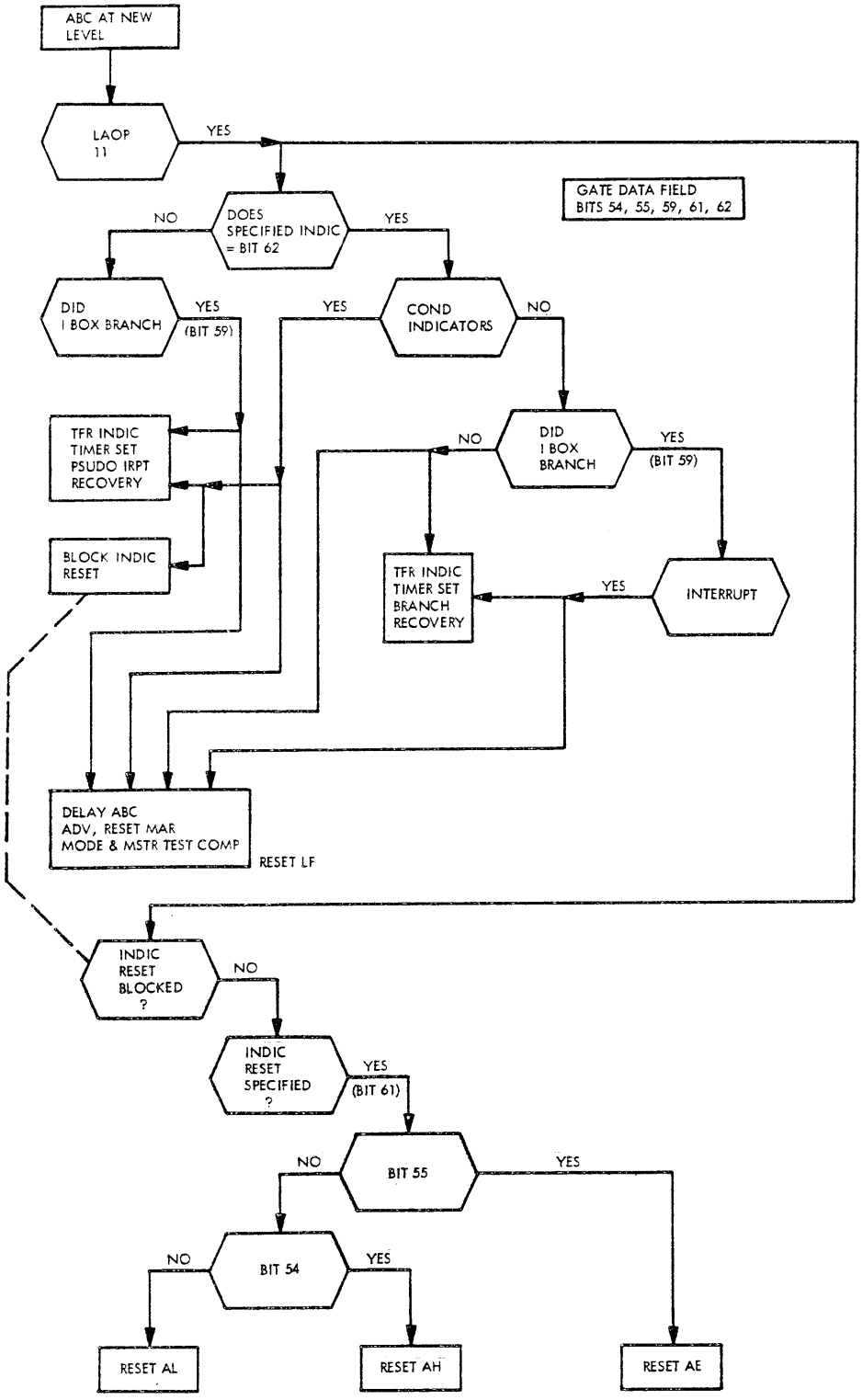


FIGURE 3.2.24. ABC ACTION ON BAC (LAOP 11)

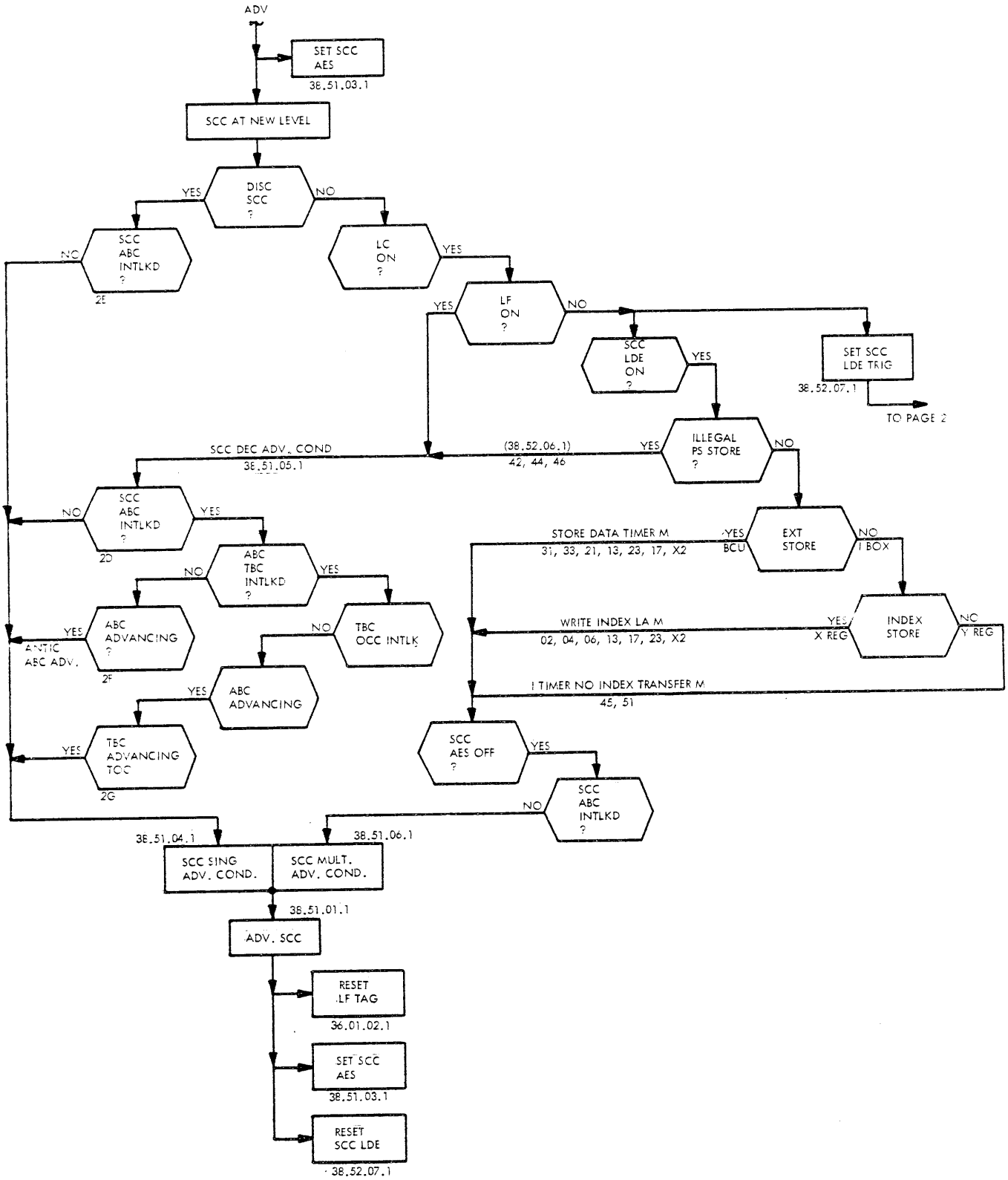


FIGURE 3.2.25. SCC ADVANCE

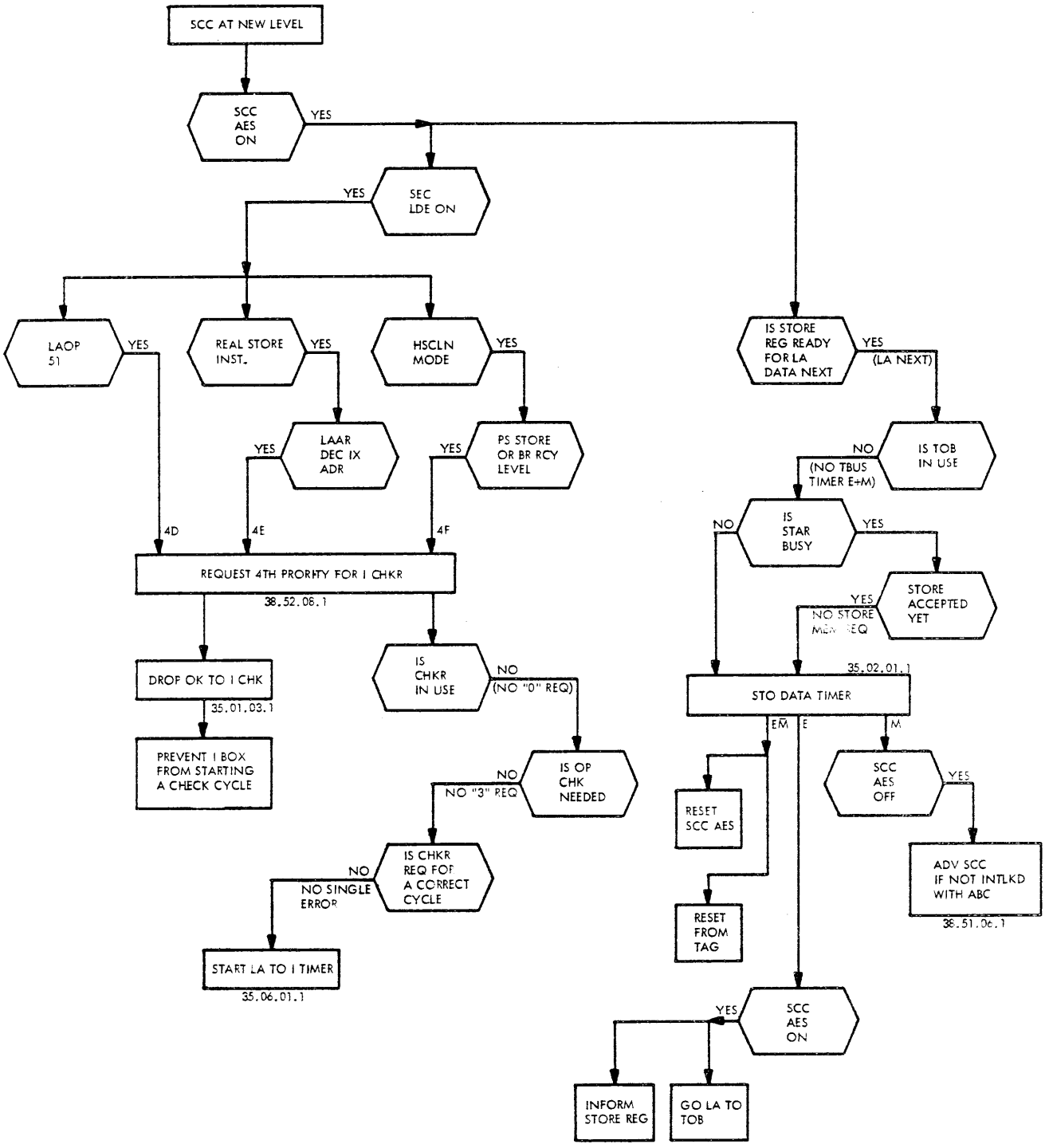


FIGURE 3.2.26. SCC ACTIONS

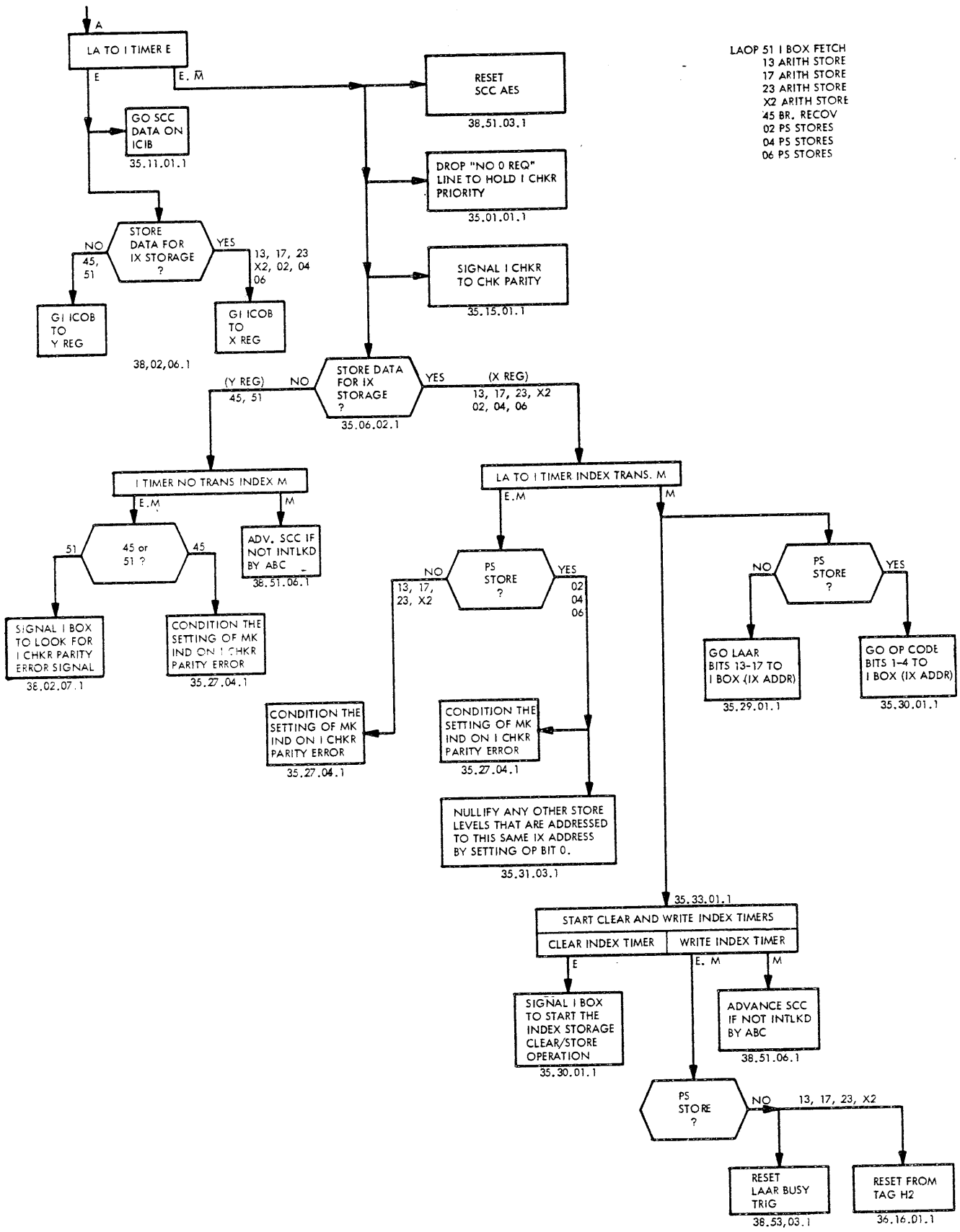


FIGURE 3.2.27. SCC STORES TO I BOX

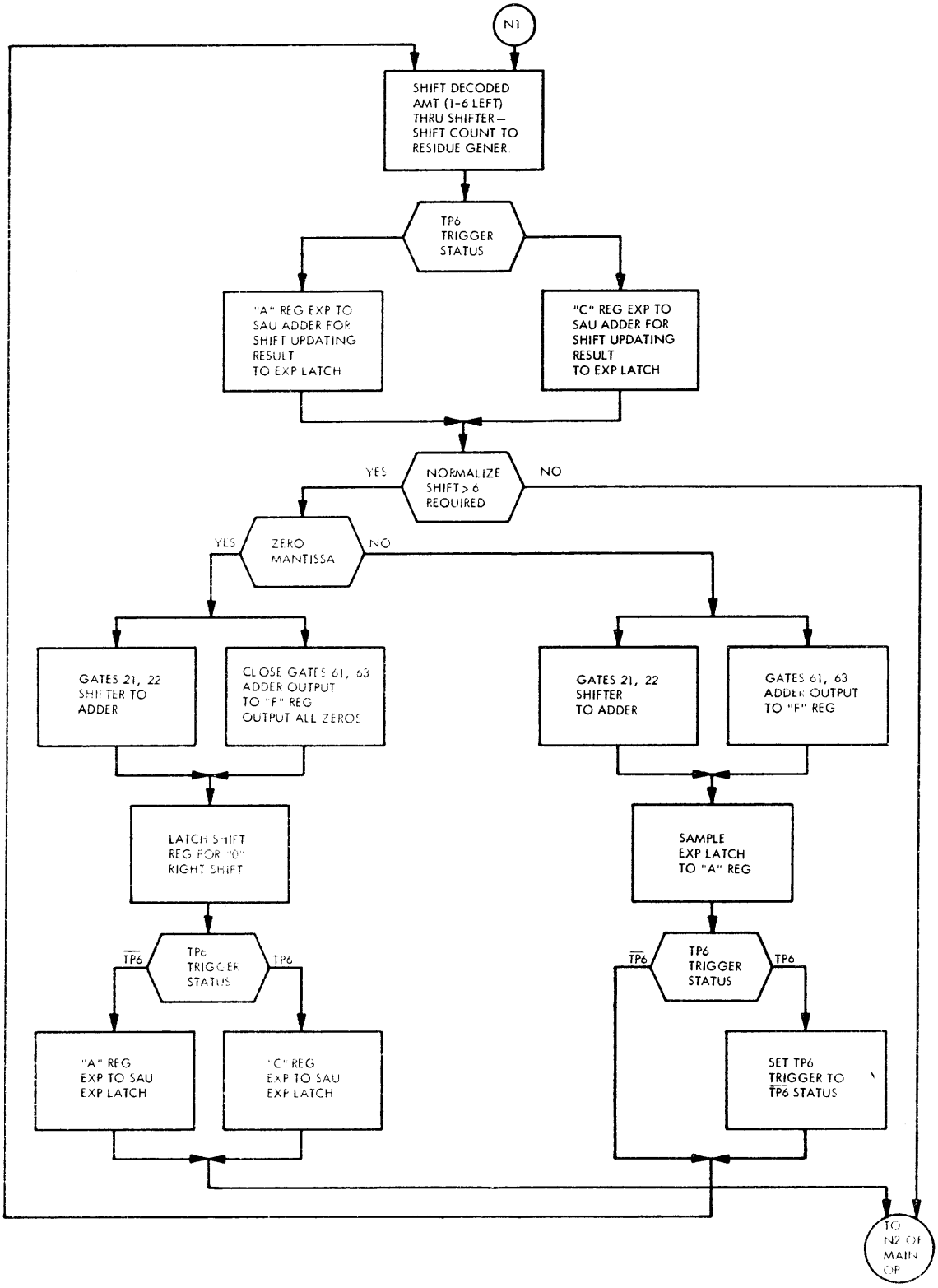


FIGURE 3.3.1. NORMALIZATION LOOP, TO-ACCUMULATOR OPERATION

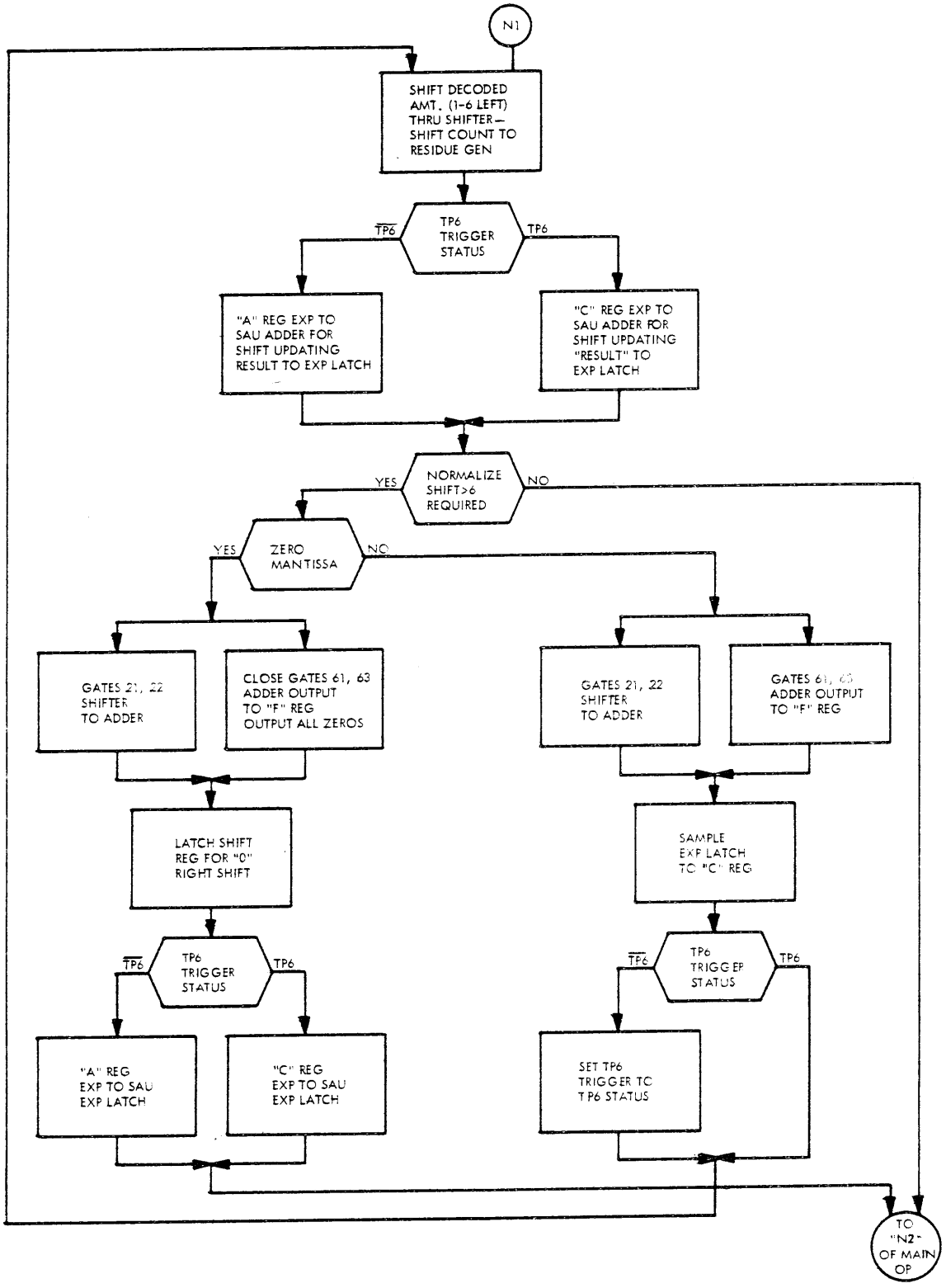


FIGURE 3.3.2. NORMALIZATION LOOP, TO-MEMORY OPERATION

*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
TF, UF, VF			X	
RLZ,RZ,RGZ,RN			X	
MOP	X			
XPFP,XPH,XPL,XPU				X

Refer to indicator section in Appendix for more detail.

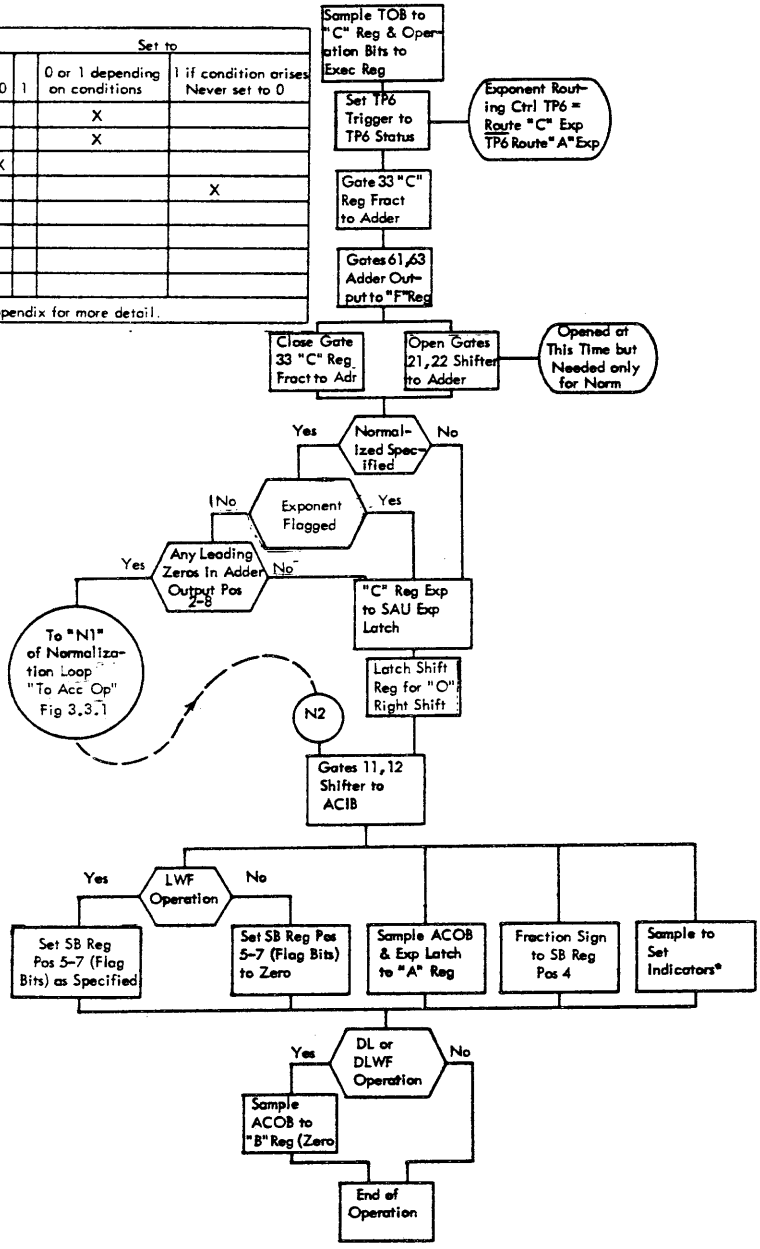


FIGURE 3.3.3. FLOATING POINT - LOAD (L), LOAD WITH FLAG (LWF), LOAD DOUBLE (DL), OR LOAD DOUBLE WITH FLAG (DLWF)

*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
TF, UF, VF			X	
MOF (0 on +, 1 on M+)			X	
RLZ, RZ, RGZ, RN			X	
LC				X
LS				X
PSH 48				X
XPFP, XPO, XPH, XPL, XPU				X

Refer to indicator section in Appendix for more detail.

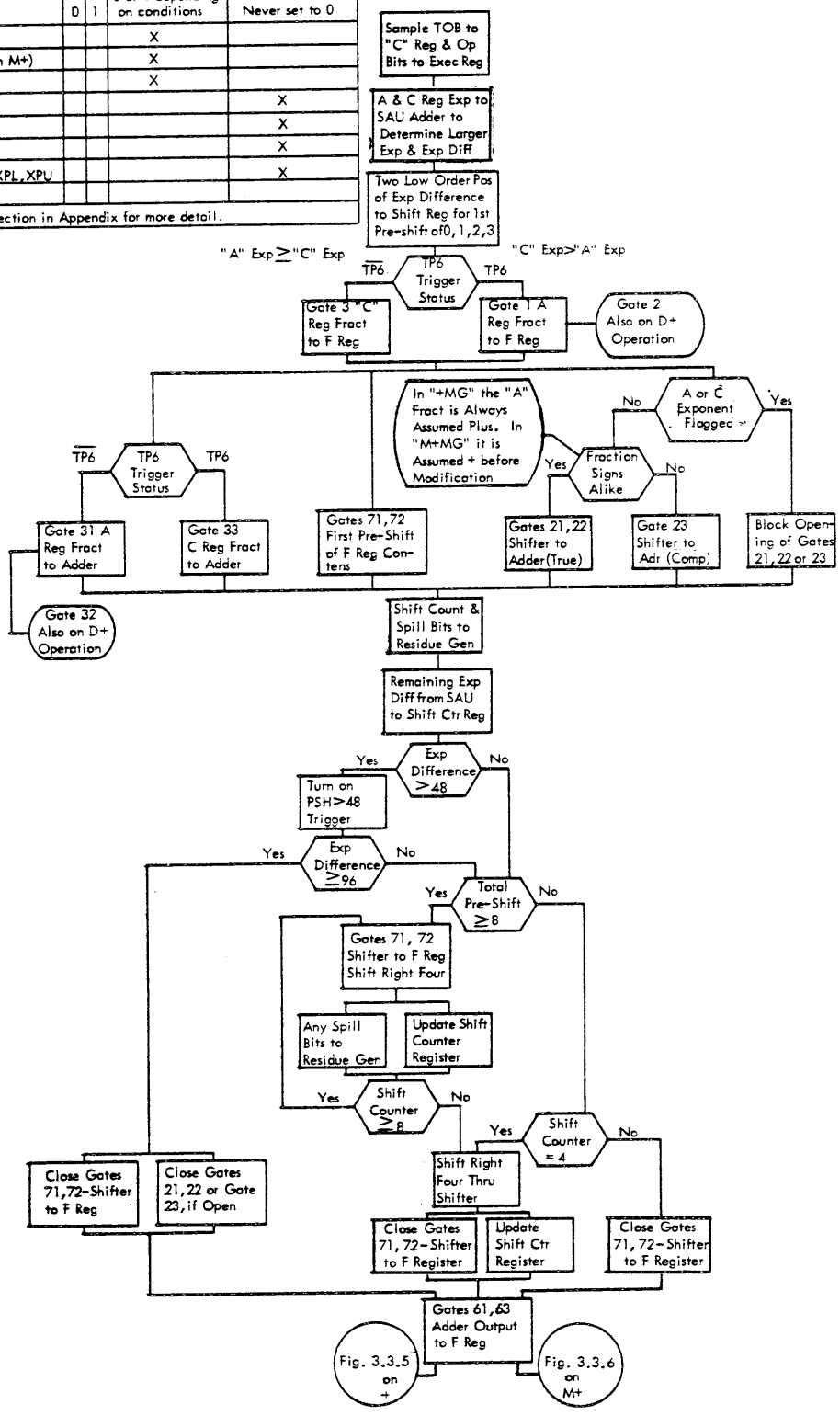


FIGURE 3.3.4. FLOATING POINT-ADD (+), ADD MAGNITUDE (+MG), ADD DOUBLE (D+), ADD MAGNITUDE DOUBLE (D+MG)

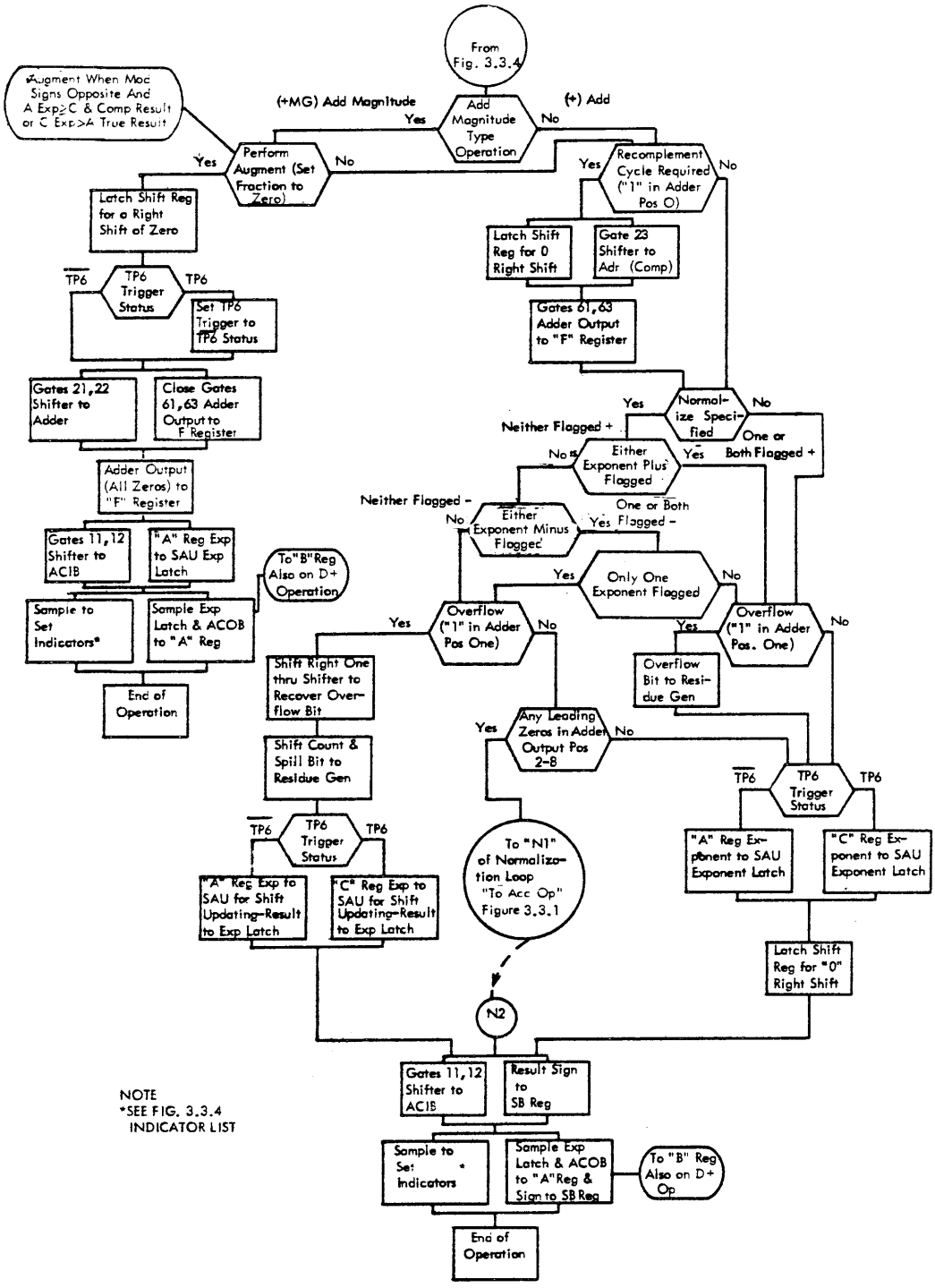


FIGURE 3.3.5. FLOATING POINT - ADD (+), ADD MAGNITUDE (+MG), ADD DOUBLE (D+), ADD MAGNITUDE DOUBLE (D+MG)

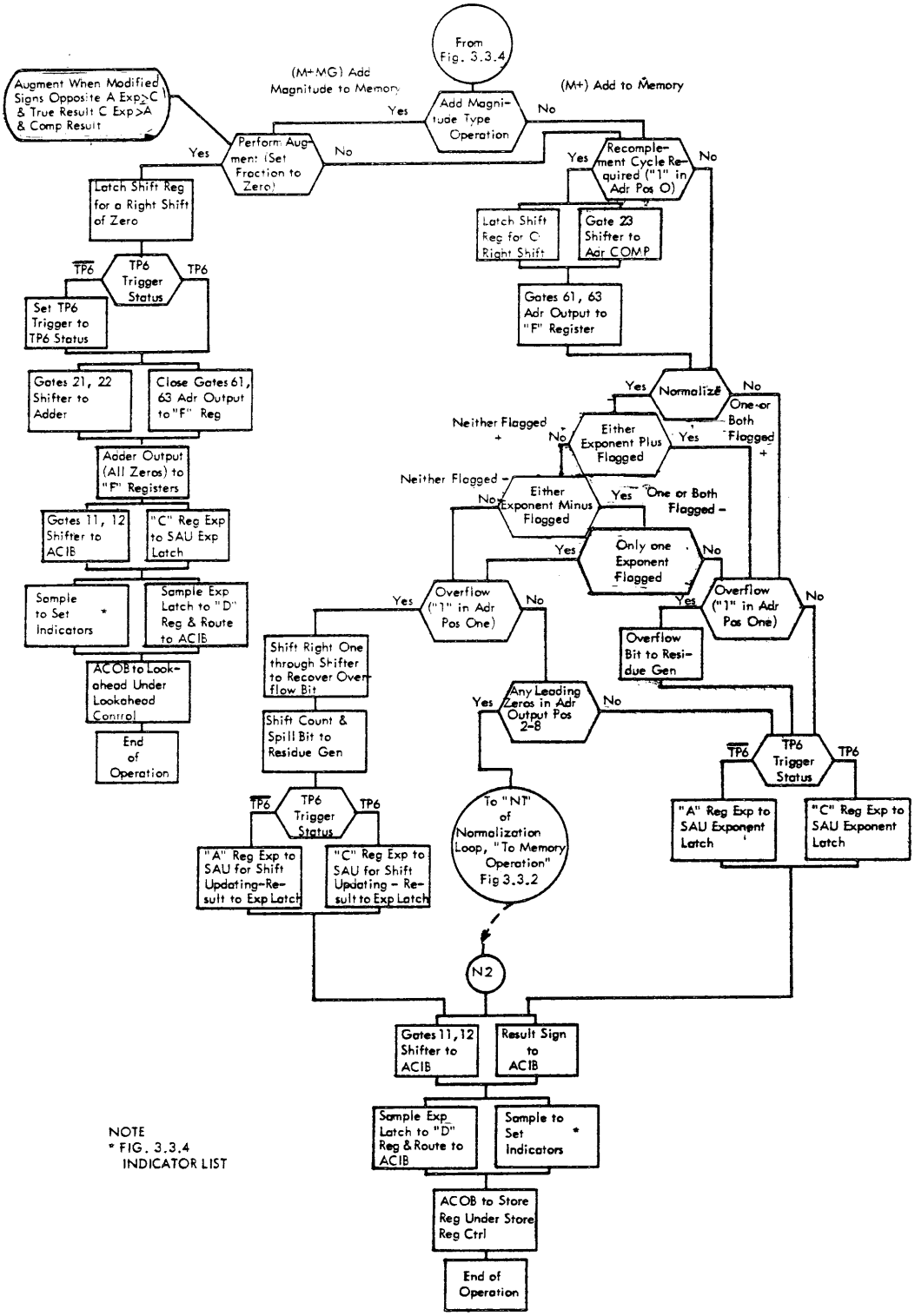


FIGURE 3.3.6. FLOATING POINT - ADD TO MEMORY (M+), ADD MAGNITUDE TO MEMORY (M+MG)

*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
TF, UF, VF			X	
MOP	X			
AL, AE, AH			X	
PSH 48				X
Refer to indicator section in Appendix for more detail.				

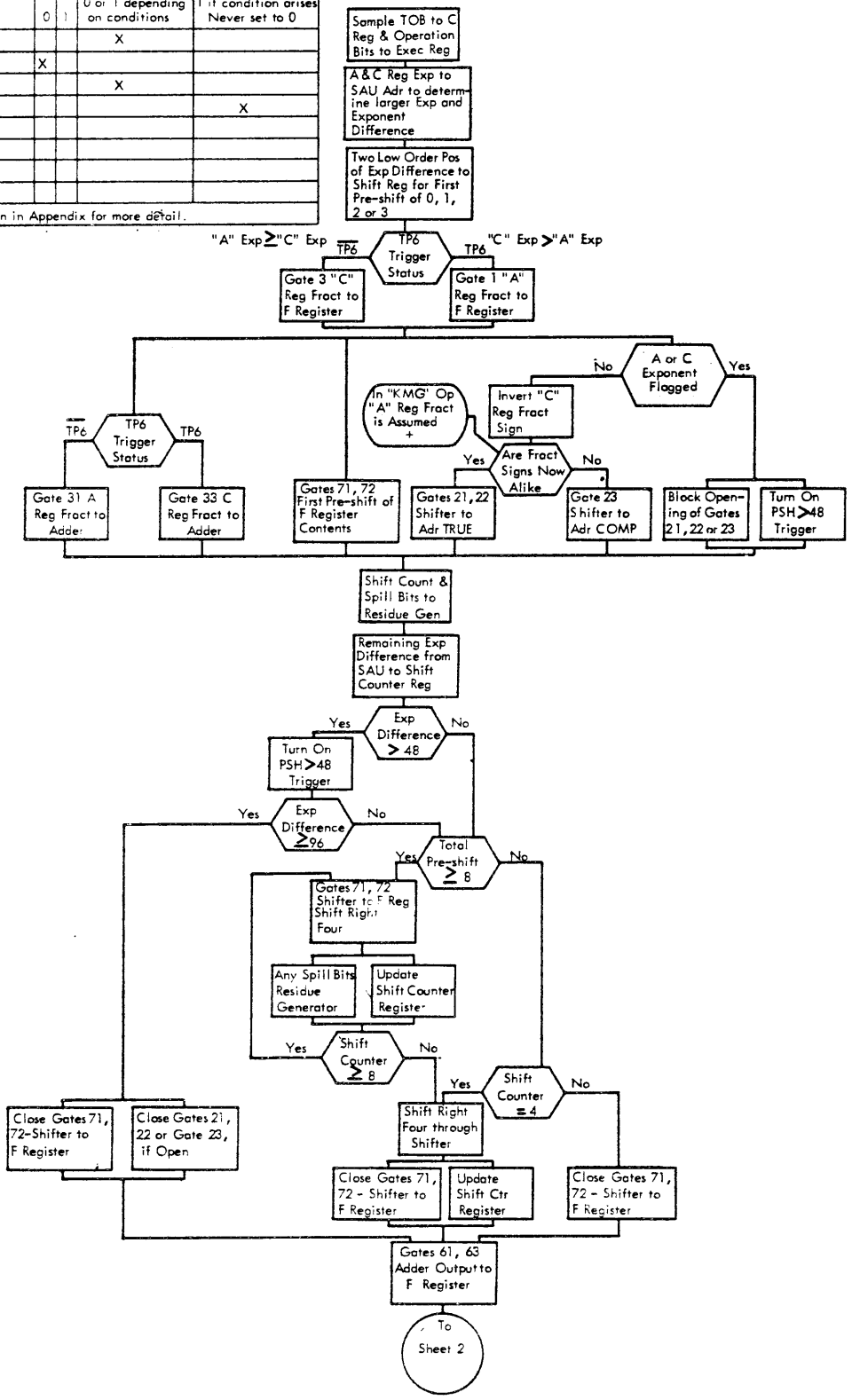


FIGURE 3.3.7. COMPARE (K), COMPARE FOR RANGE (KR), COMPARE MAGNITUDE (KMG), COMPARE MAGNITUDE FOR RANGE (KMGR) (SHEET 1 OF 3)

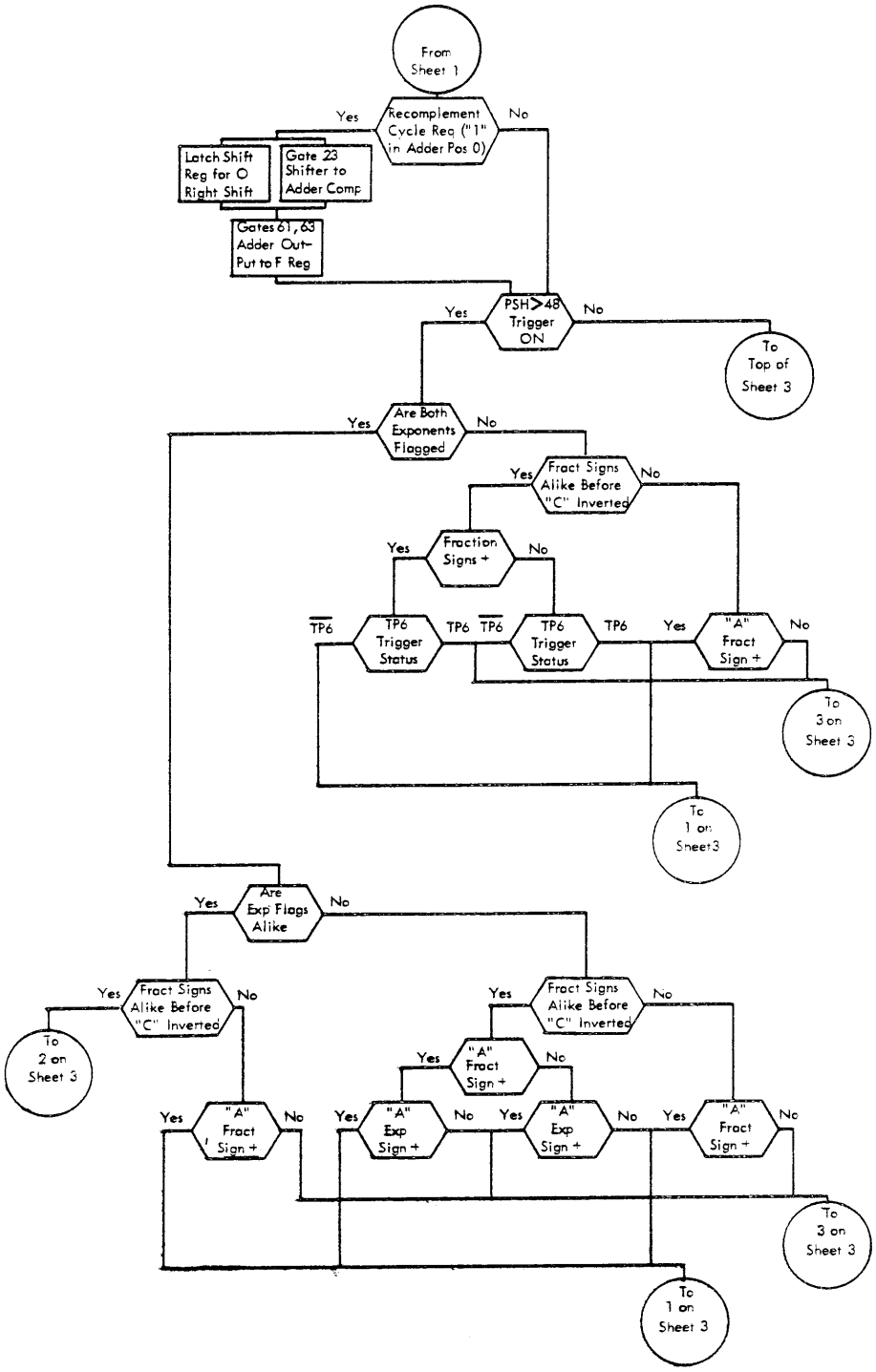


FIGURE 3.3.7. COMPARE (K), COMPARE FOR RANGE (KR), COMPARE MAGNITUDE (KMG), COMPARE MAGNITUDE FOR RANGE (KMGR) (SHEET 2 OF 3)

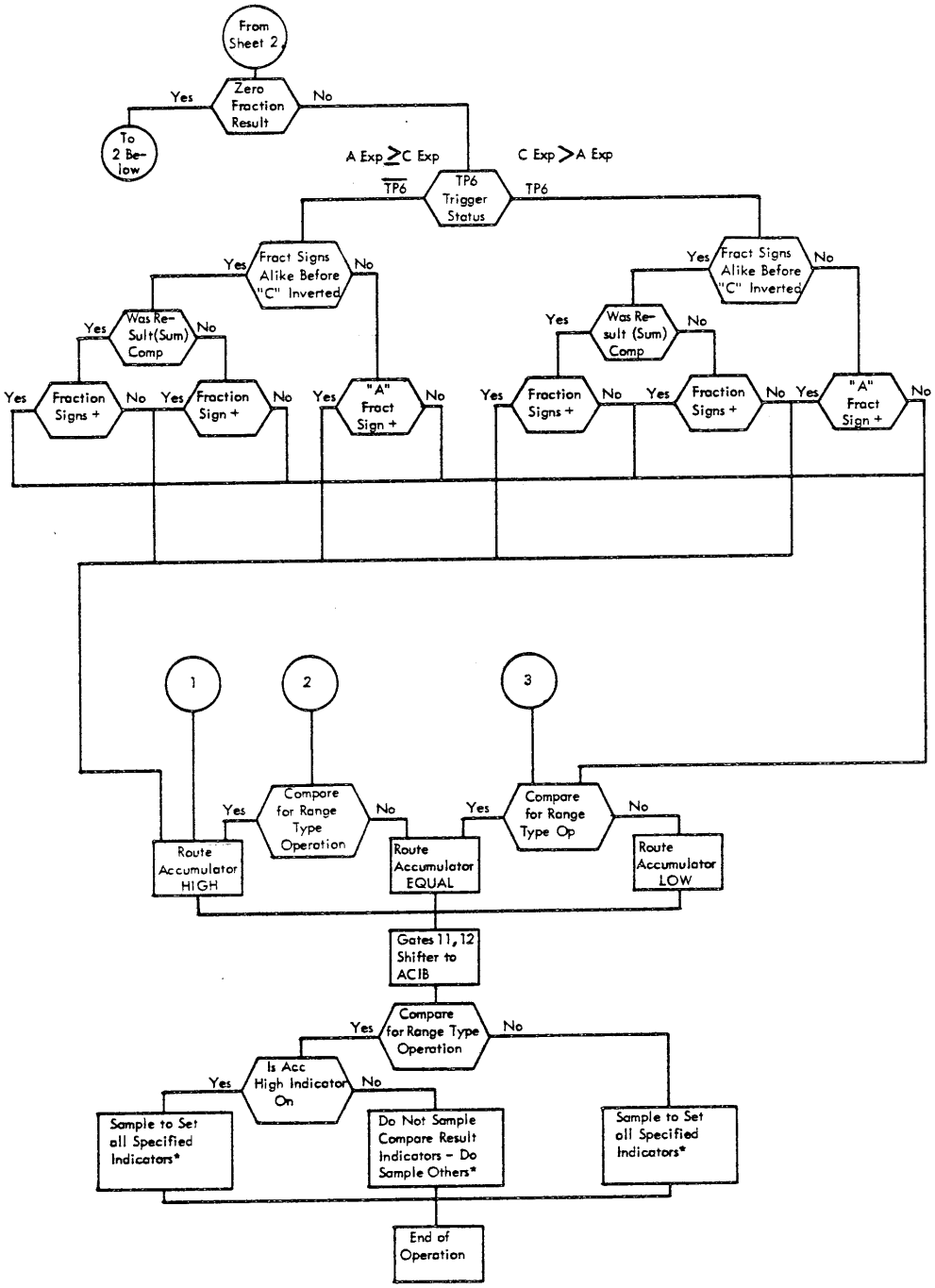


FIGURE 3.3.7. COMPARE (K), COMPARE FOR RANGE (KR), COMPARE MAGNITUDE (KMG), COMPARE MAGNITUDE FOR RANGE (KMGR) (SHEET 3 OF 3)

*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
TF,UF,VF			X	
RLZ,RZ,RGZ,RN			X	
MOP	X			
LC				X
LS				X
XPFP,XPO,XPH,XPL,XPU				X
Refer to indicator section in Appendix for more detail.				

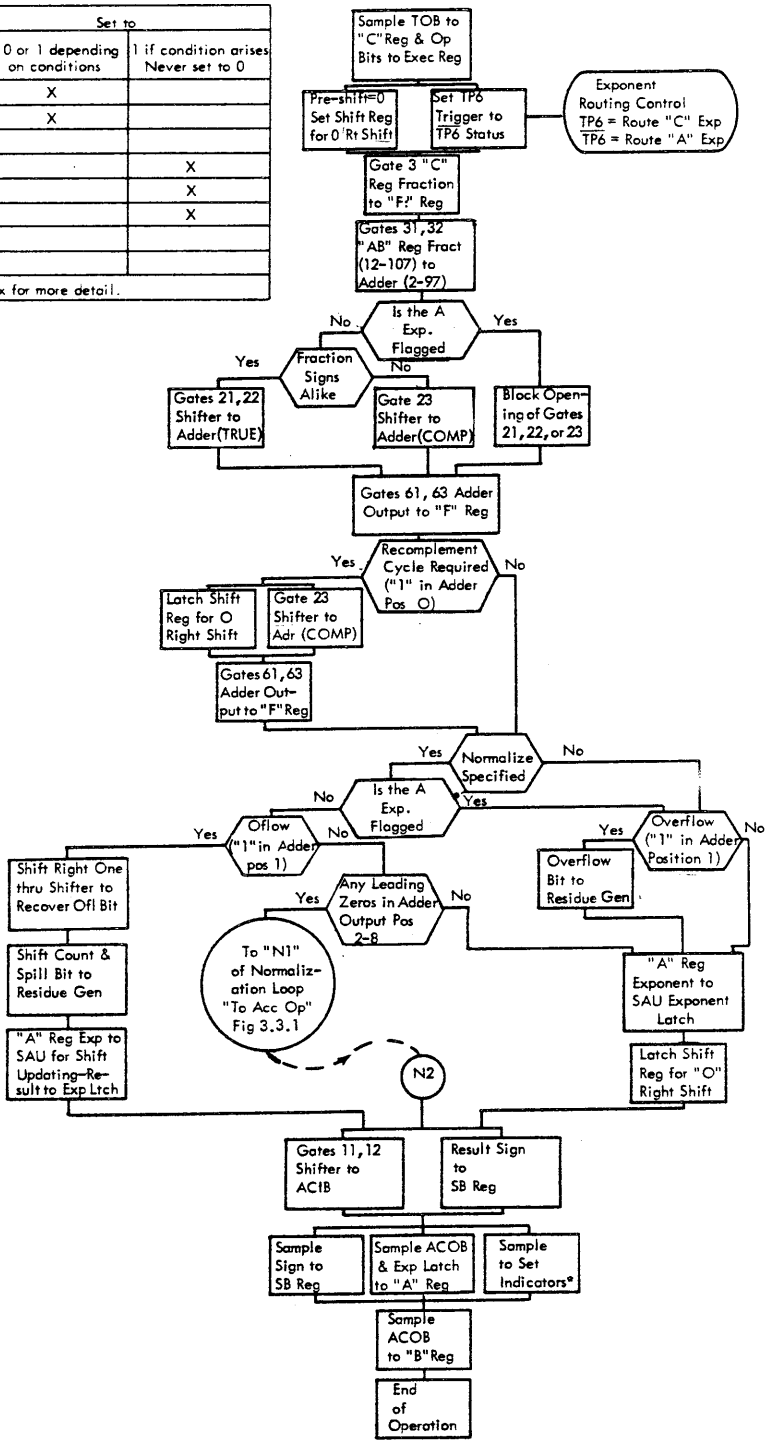


FIGURE 3.3.8. FLOATING POINT - ADD TO FRACTION (FT)

*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
RLZ,RZ,RGZ,RN			X	
LC				X
MOP	X			
XPFP,XPH,XPL				X

Refer to indicator section in Appendix for more detail.

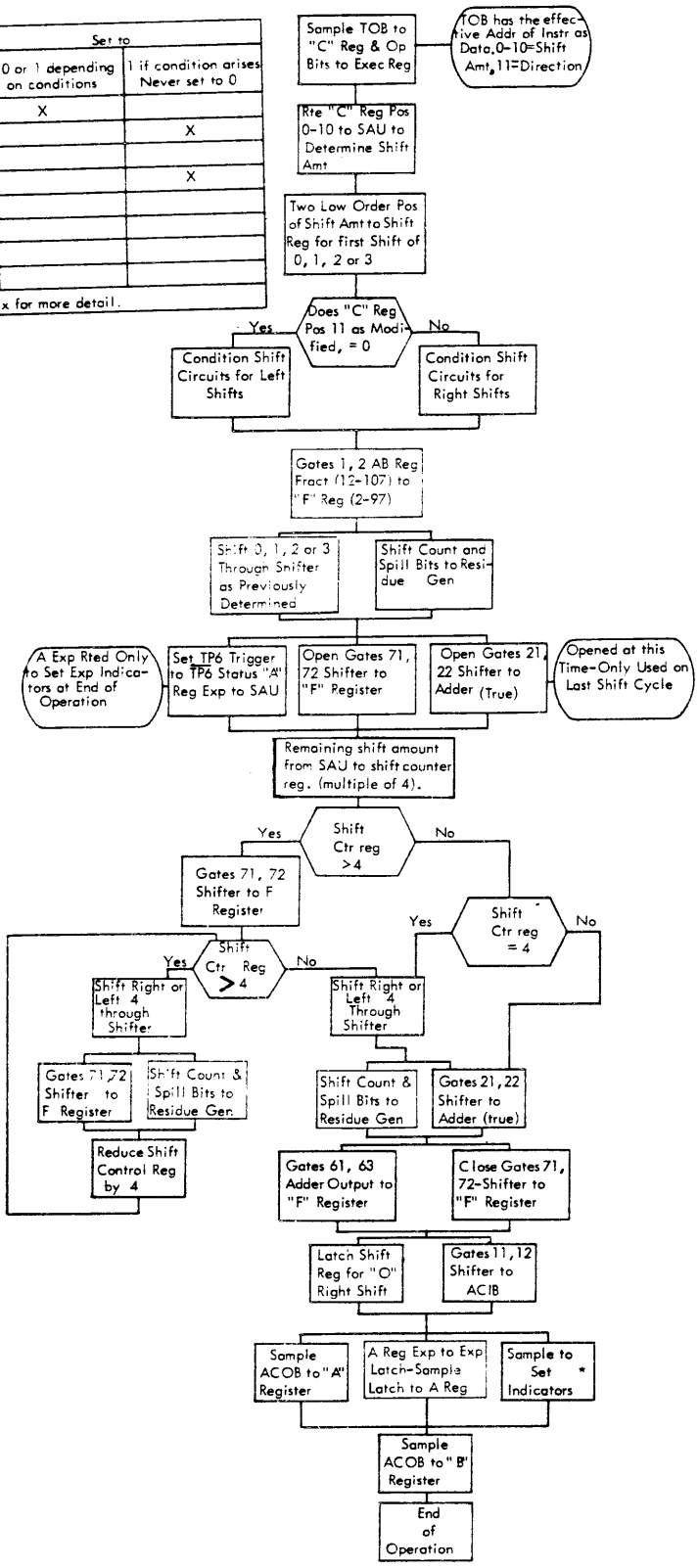


FIGURE 3.3.9. FLOATING POINT - SHIFT FRACTION (SHF)

*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
RLZ,RZ,RGZ,RN			X	
MOP		X		
XPFP,XPH,XPL,XPU				X

Refer to indicator section in Appendix for more detail.

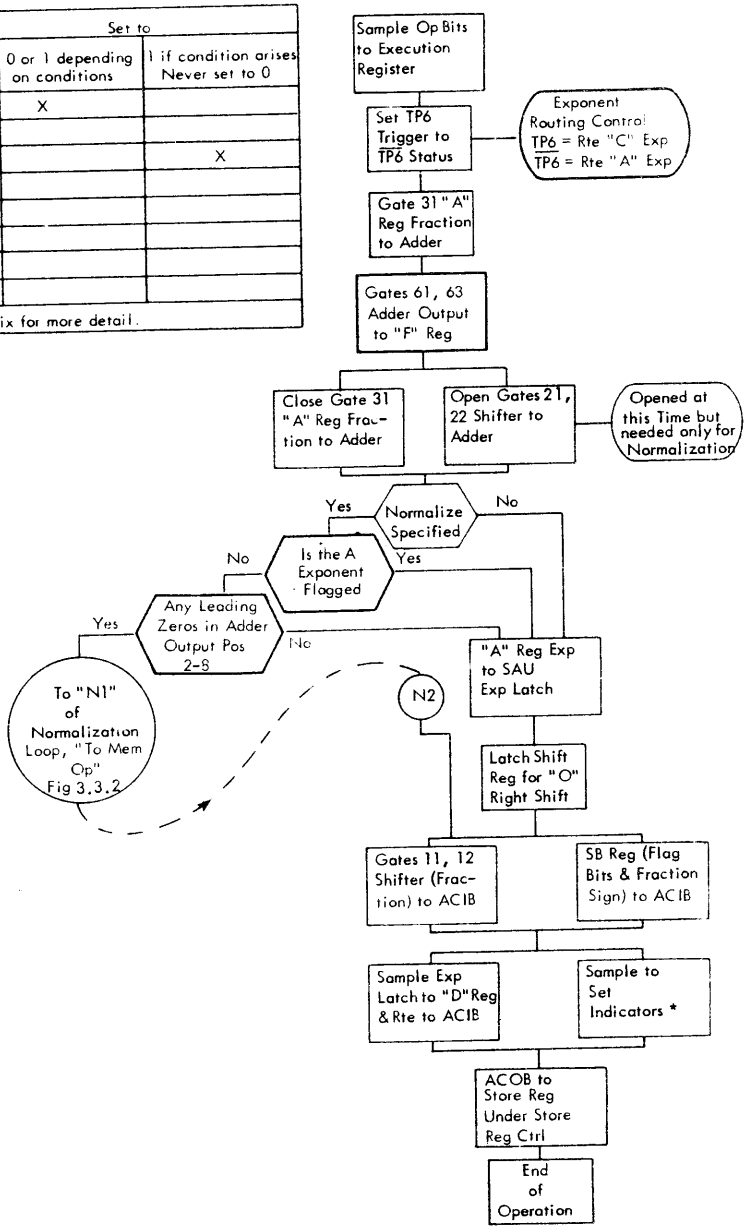


FIGURE 3.3.10. FLOATING POINT – STORE (ST)

*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
MOP		X		
RLZ,RZ,RGZ,RN			X	
LC				X
XPFP,XPO,XPH,XPL,XPU				X

Refer to indicator section in Appendix for more detail.

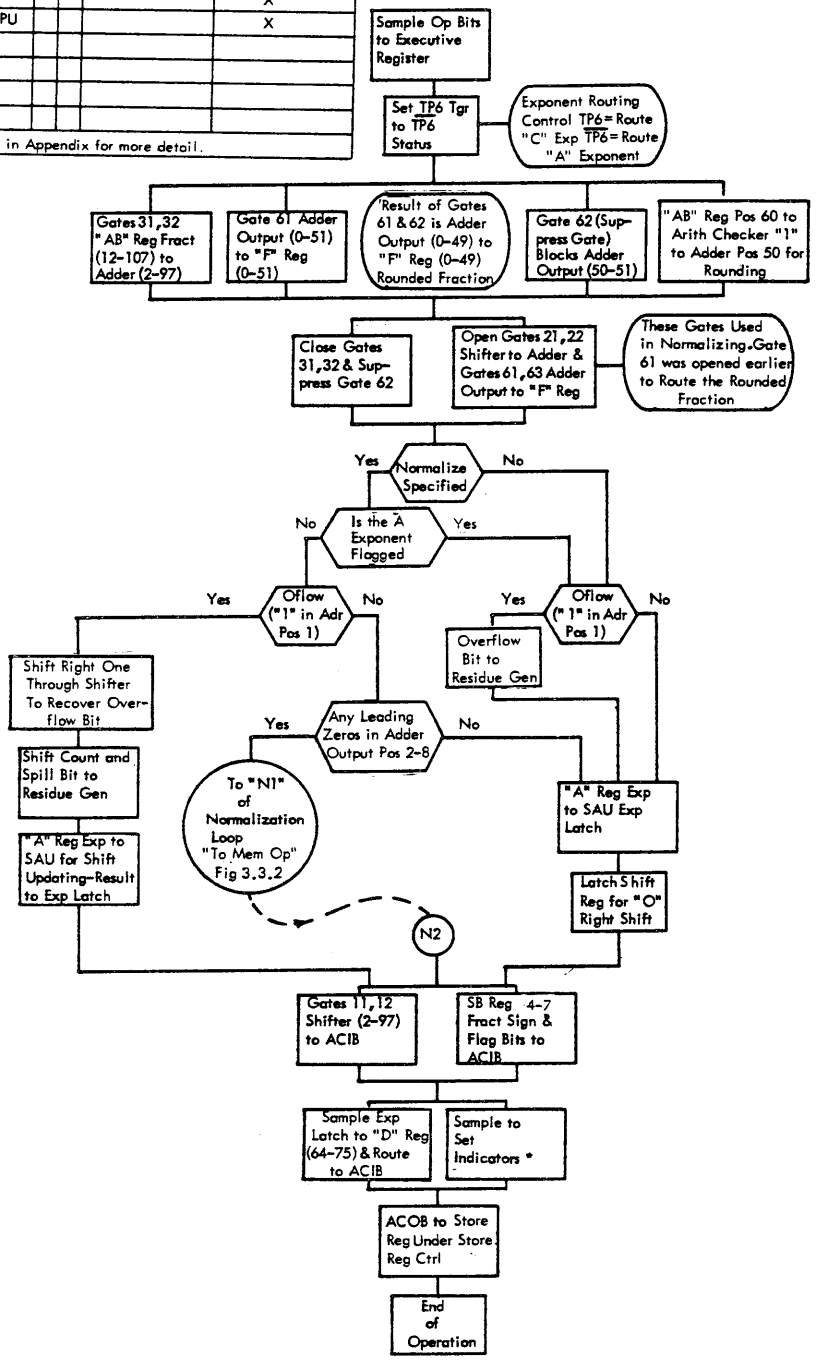


FIGURE 3.3.11. FLOATING POINT – STORE ROUNDED (SRD)

*Indicators	Set to			
	0	1	0 or 1 depending on conditions	1 if condition arises. Never set to 0
RLZ,RZ,RGZ,RN				X
MOP			X	
XPF,XPO,XPH,XPL,XPU				X
Refer to indicator section in Appendix for more detail.				

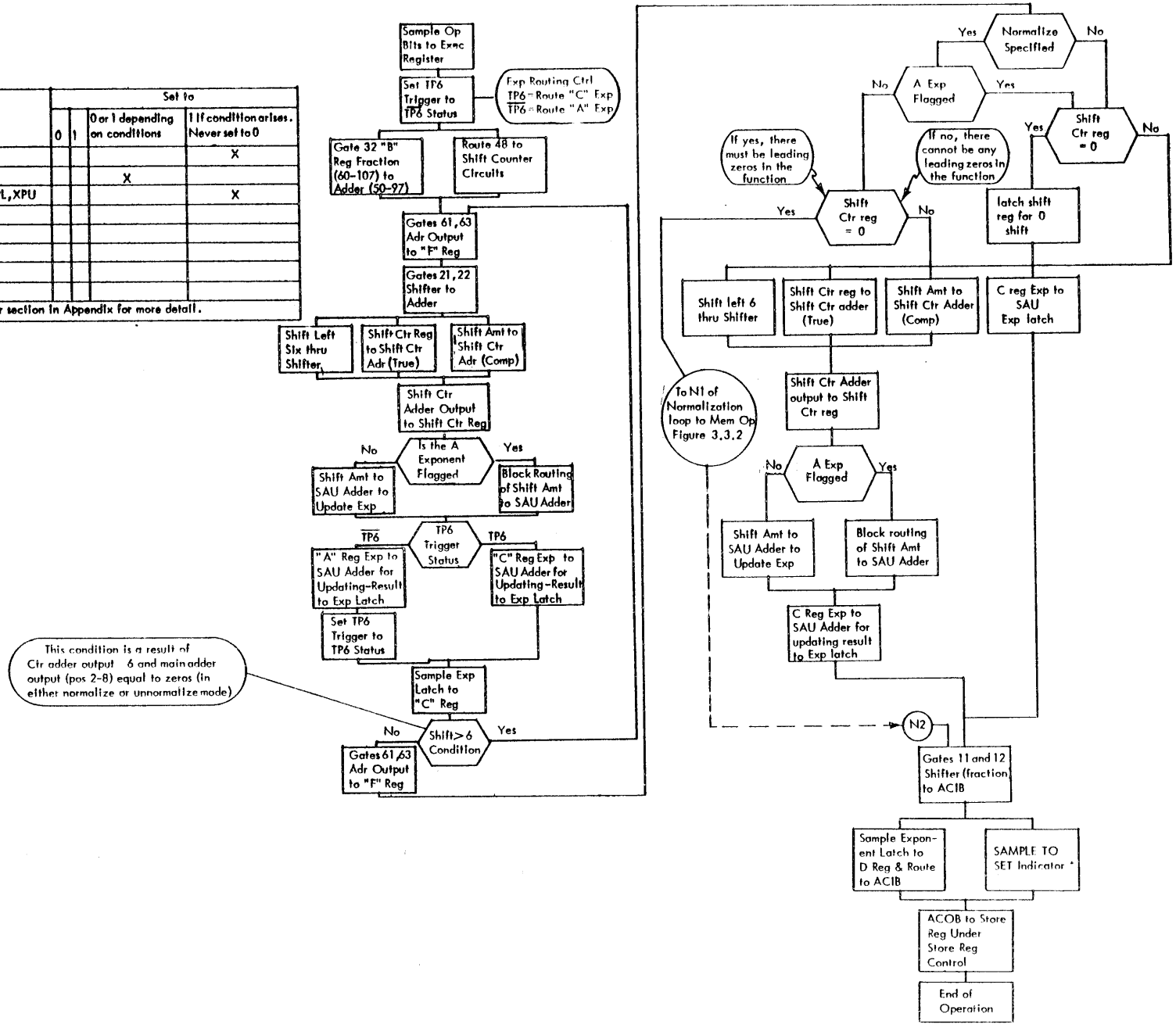
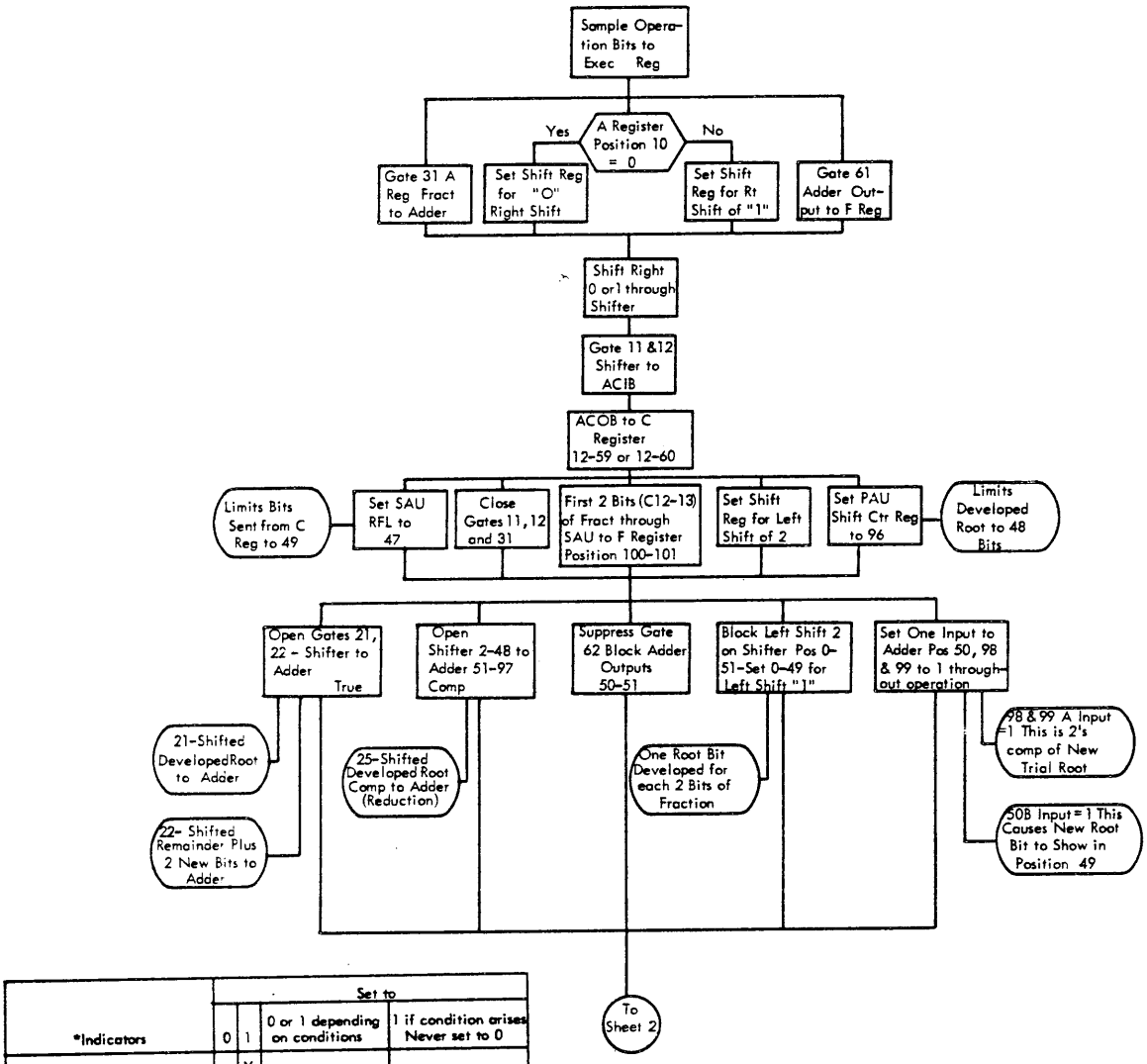


FIGURE 3.3.12. FLOATING POINT – STORE LOW ORDER (SLO)



*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
MOP		X		
RLZ, RZ, RGZ, RN			X	
IR				X
XPFP,XPH,XPL,XPU				X

Refer to indicator section in Appendix for more detail.

FIGURE 3.3.13. FLOATING POINT – STORE ROOT (SRT) (SHEET 1 OF 3)

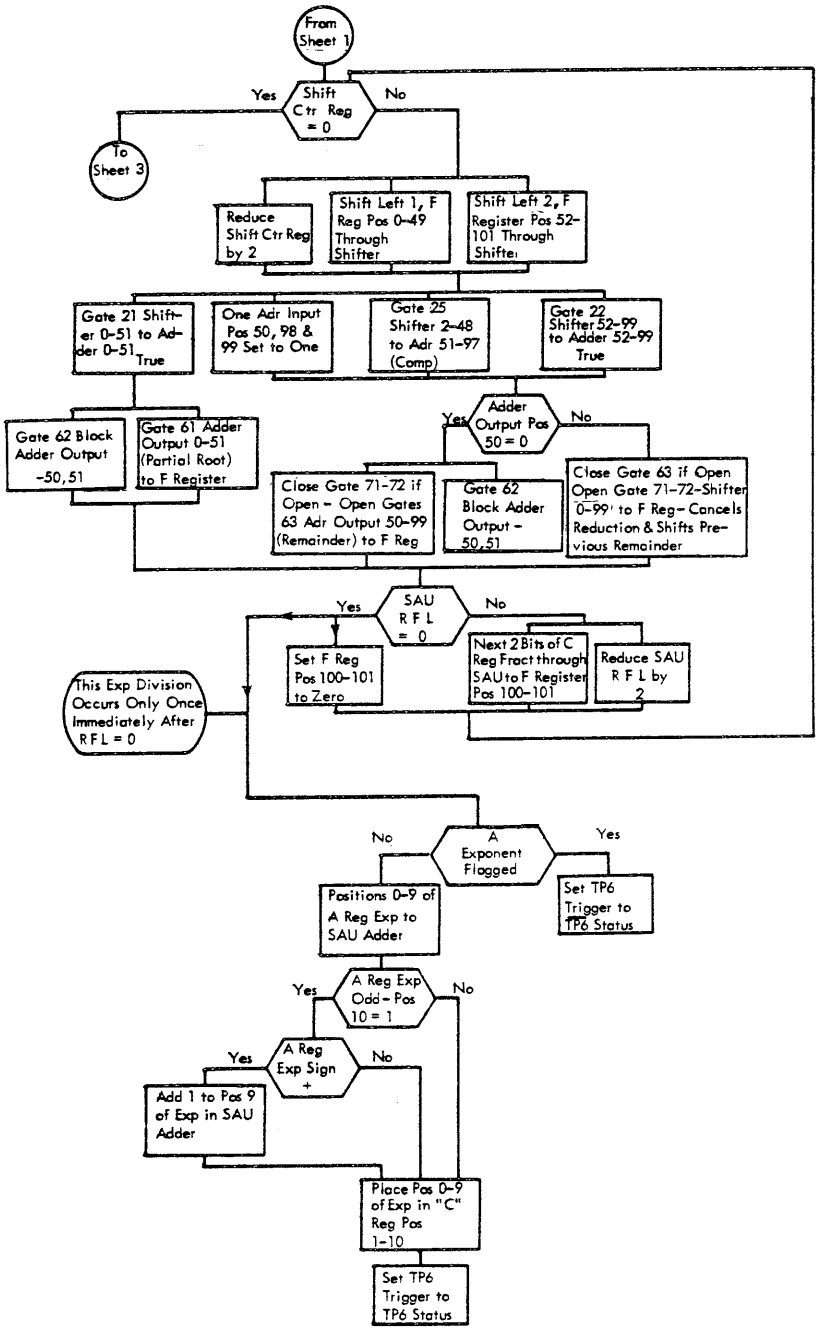


FIGURE 3.3.13. FLOATING POINT –STORE ROOT (SRT)
(SHEET 2 OF 3)

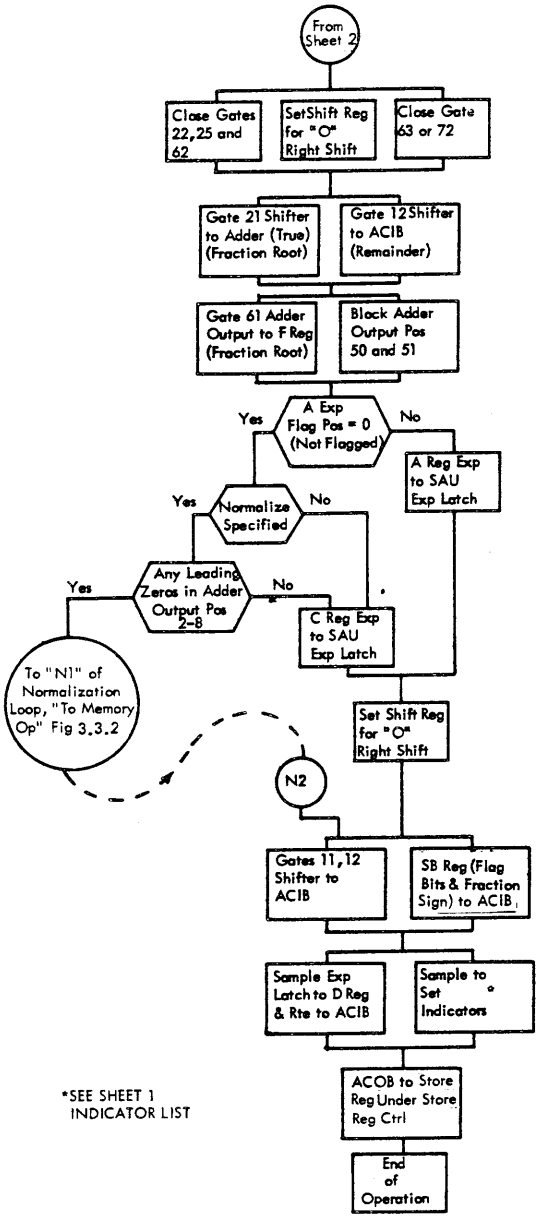


FIGURE 3.3.13. FLOATING POINT—STORE ROOT (SRT)
(SHEET 3 OF 3)

*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
TF, UF, VF			X	
RLZ, RZ, RGZ, RN			X	
MOP	X			
XPFP, XPO, XPH, XPL, XPU				X
Refer to indicator section in Appendix for more detail.				

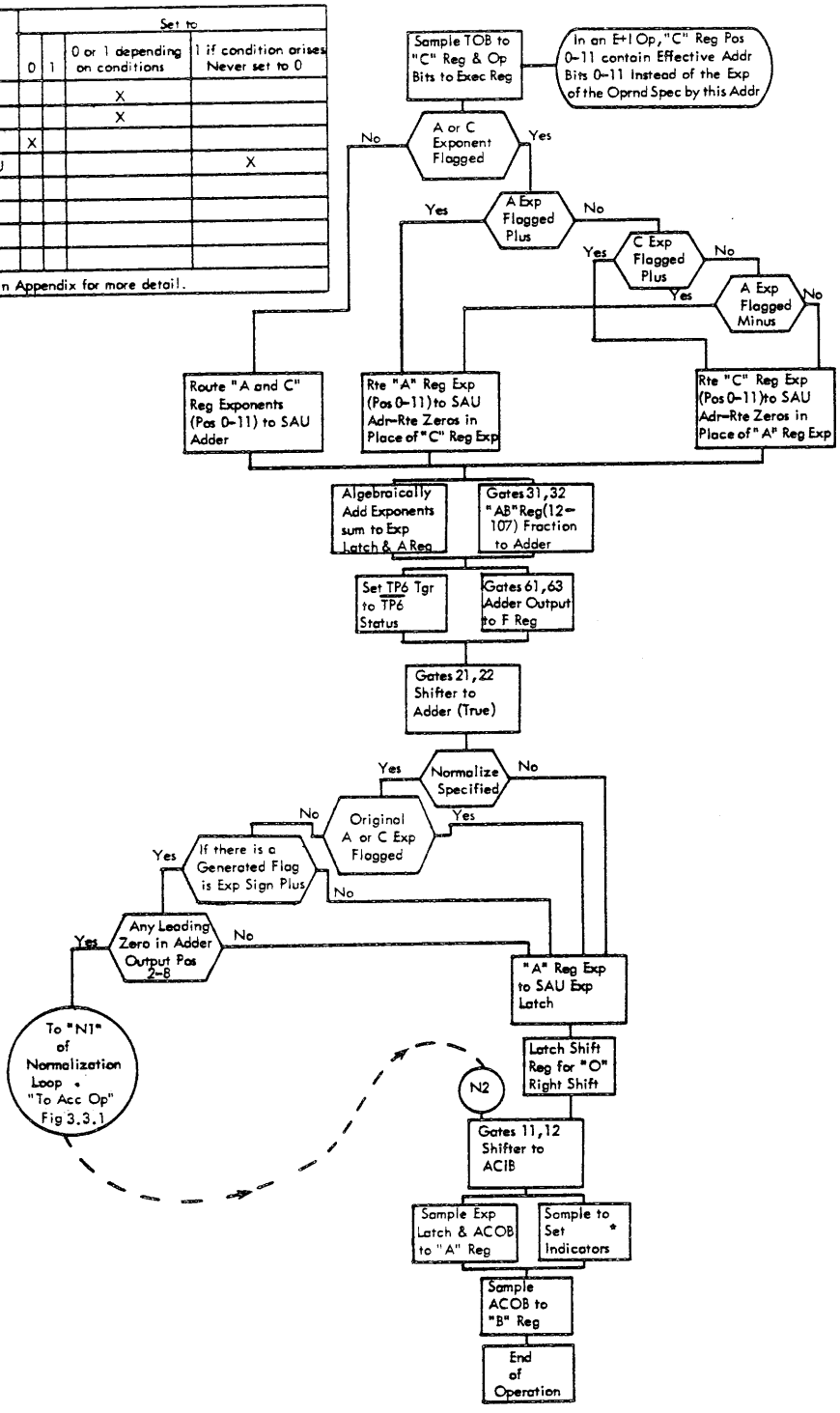


FIGURE 3.3.14. FLOATING POINT – ADD TO EXPONENT (E+), ADD IMMEDIATE TO EXPONENT (E+I)

*Indicators	Set to 0	Set to 1	0 or 1 depending on conditions	1 if condition arises Never set to 0
TF, UF, VF			X	
RLZ, RZ, RGZ, RN			X	
MOP	X			
XPFP, XPH, XPL, XPU				X

Refer to indicator section in Appendix for more detail.

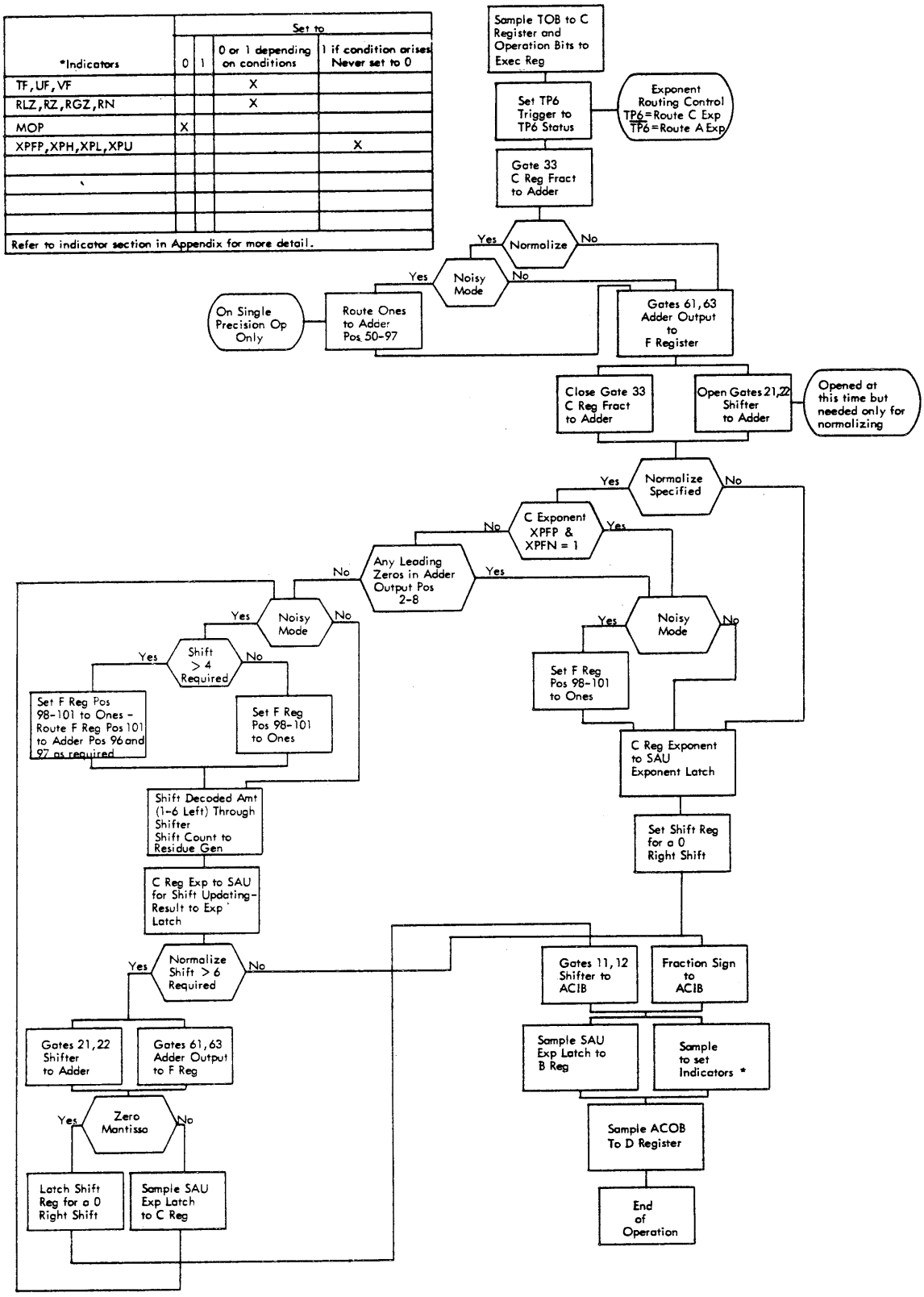


FIGURE 3.3.15. FLOATING POINT – LOAD MULTIPLIER REGISTER (LMR)

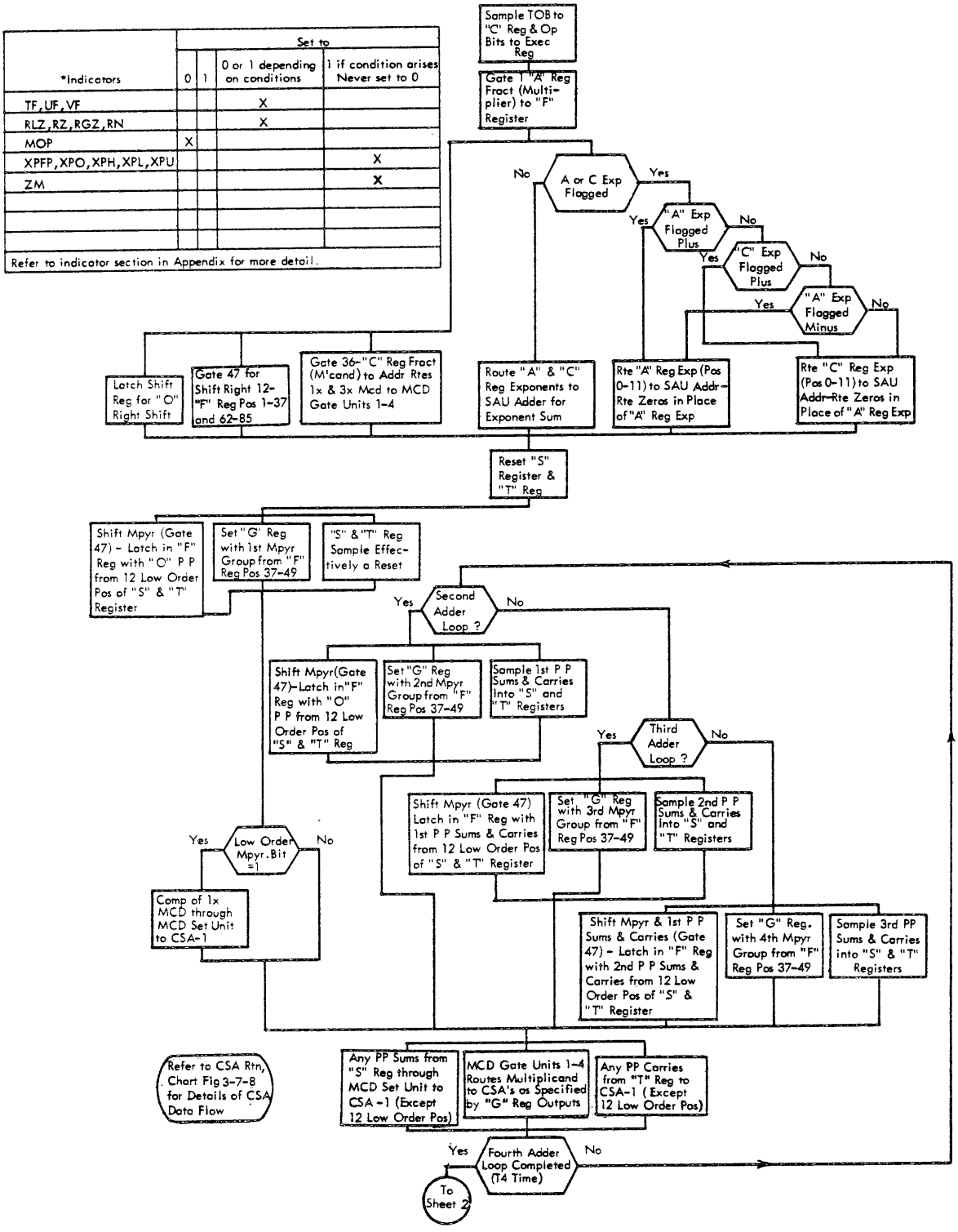


FIGURE 3.3.16. FLOATING POINT – MULTIPLY (*), MULTIPLY DOUBLE (D*) (SHEET 1 OF 2)

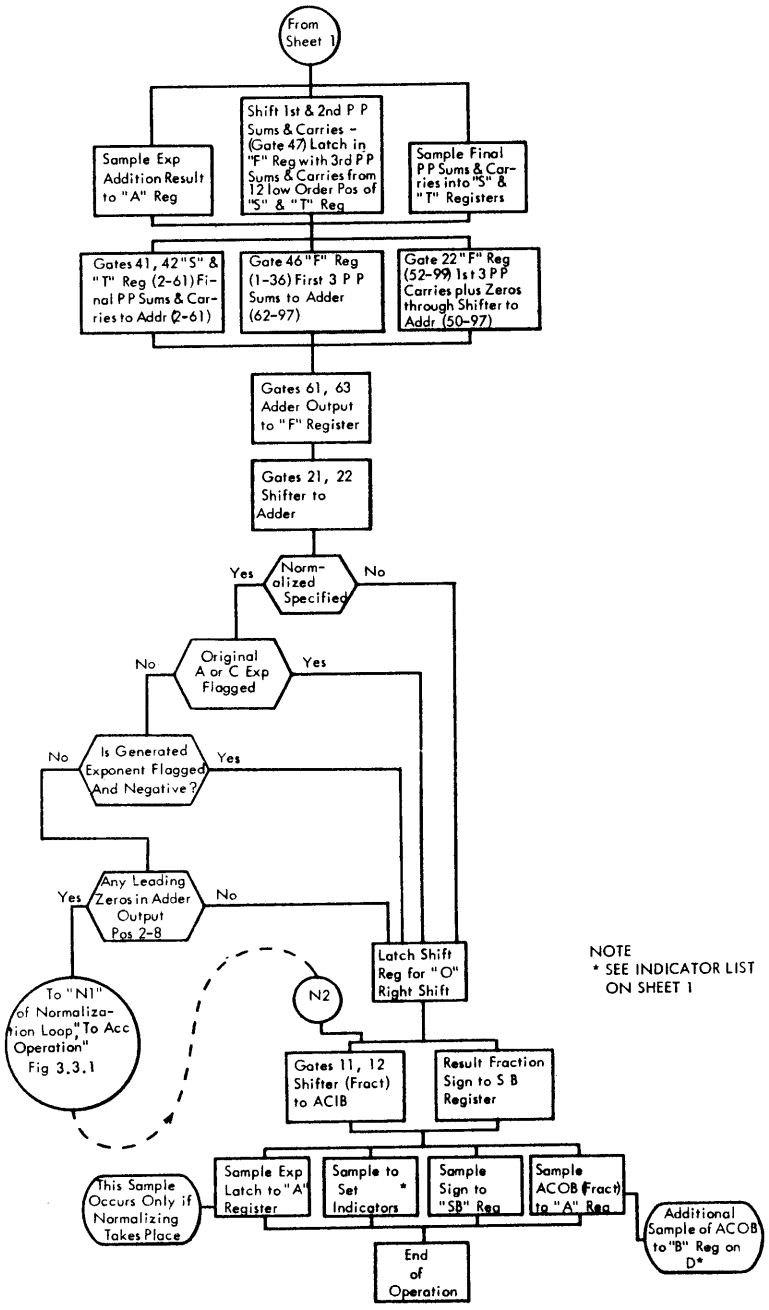


FIGURE 3.3.16. FLOATING POINT – MULTIPLY (*), MULTIPLY DOUBLE (D*) (SHEET 2 OF 2)

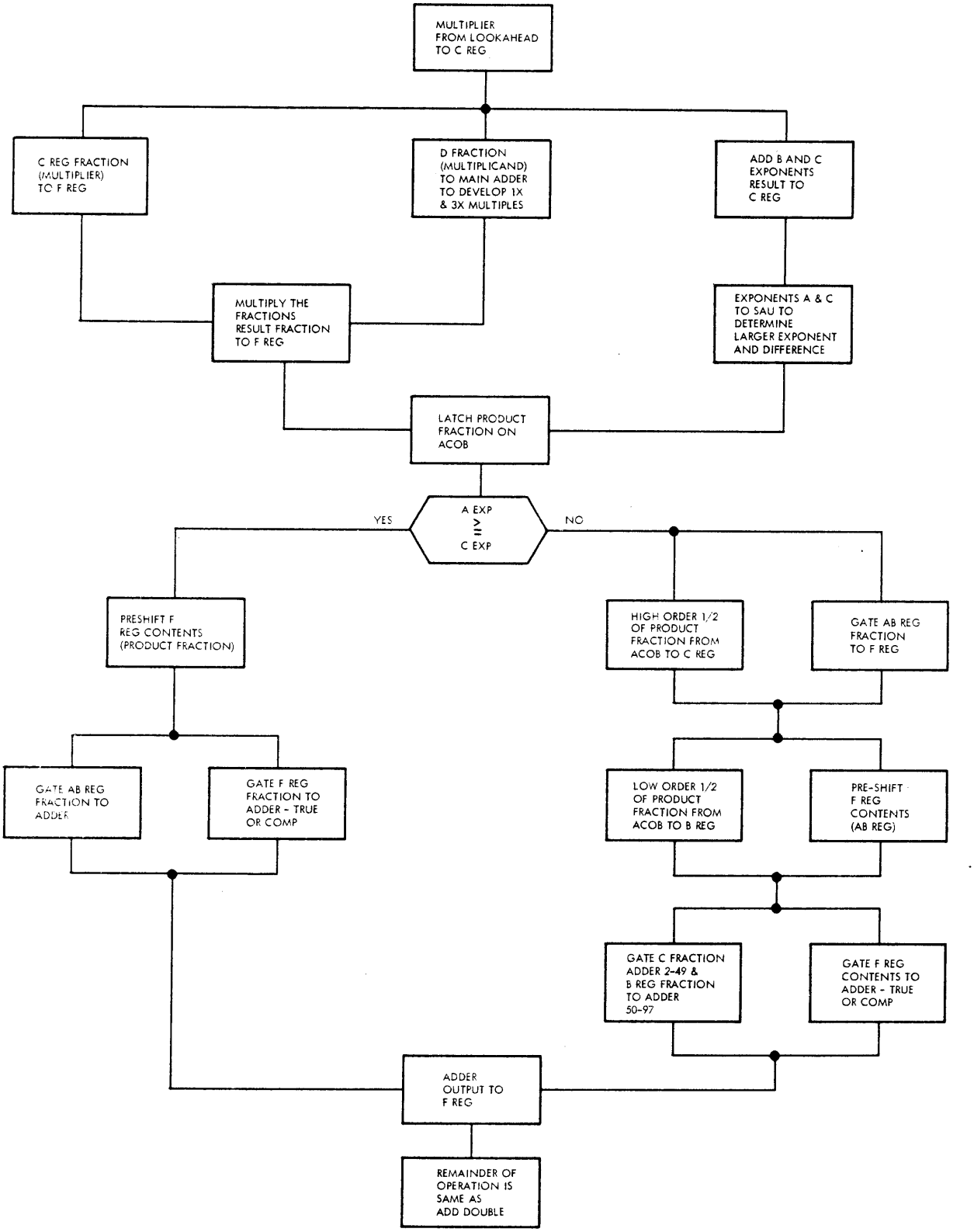


FIGURE 3.3.17. MULTIPLY AND ADD (*+)

*Indicators	Set to 0	1	0 or 1 depending on conditions	1 if condition arises Never set to 0
TF,UF,VF			X	
MOP	X			
RLZ,RZ,RGZ,RN			X	
PF				X
ZD				X
XPFP,XPO,XPH,XPU				X
RU (divide double only)				X

Refer to indicator section in Appendix for more detail.

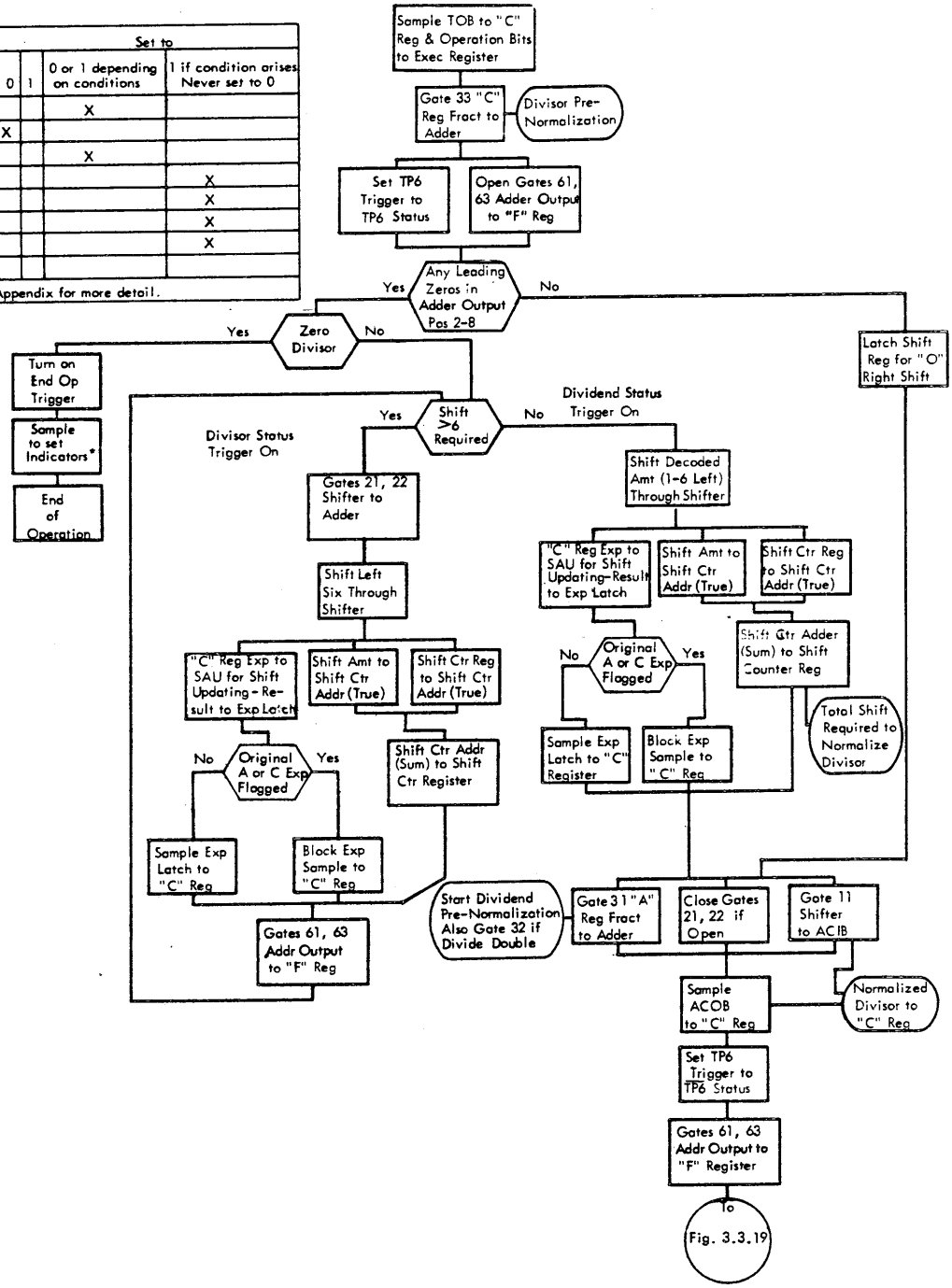


FIGURE 3.3.18. FLOATING-POINT DIVIDE (/), DIVISOR PRENORMALIZATION

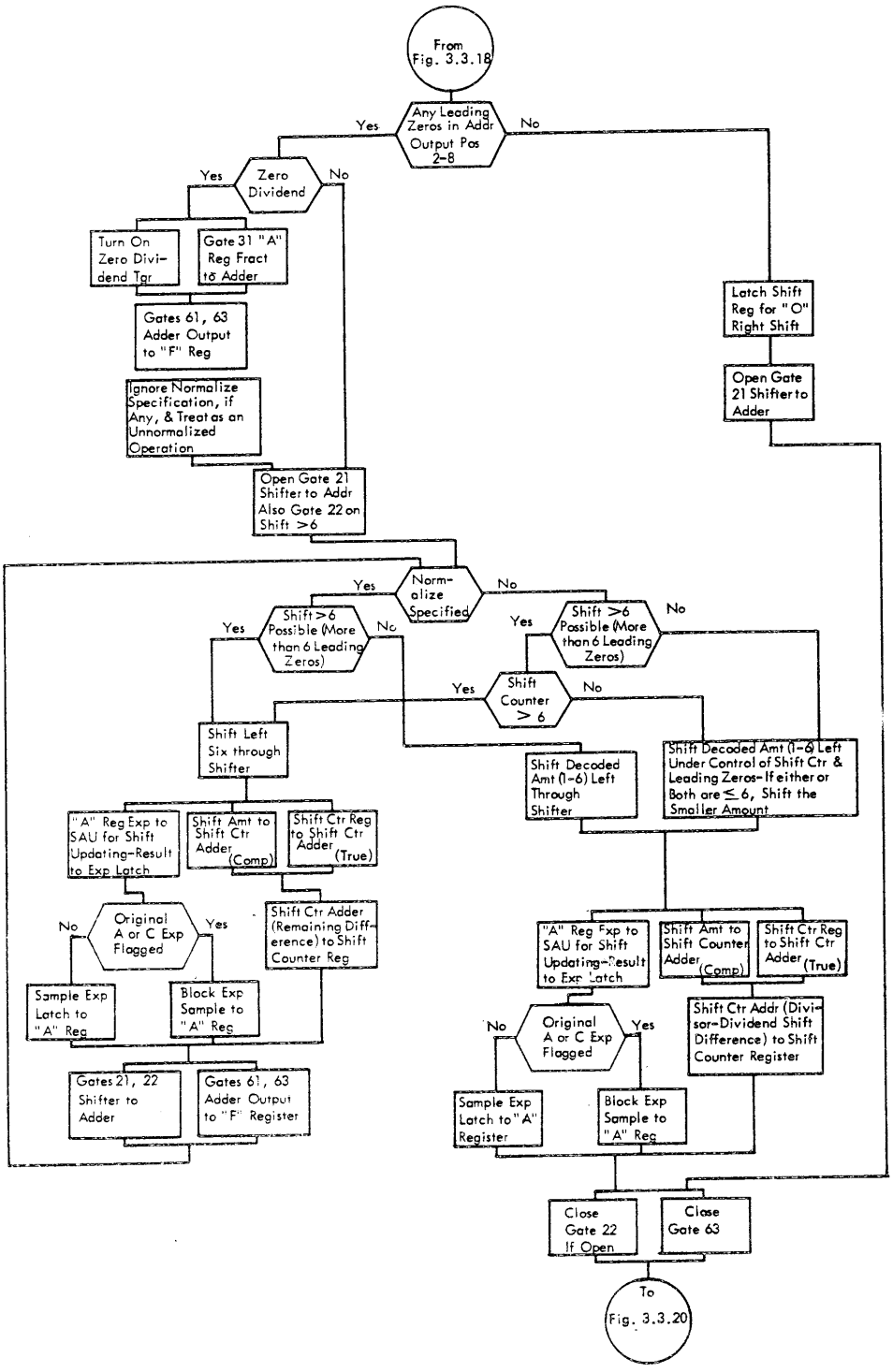


FIGURE 3.3.19. FLOATING-POINT DIVIDE (/), DIVIDEND PRENORMALIZATION

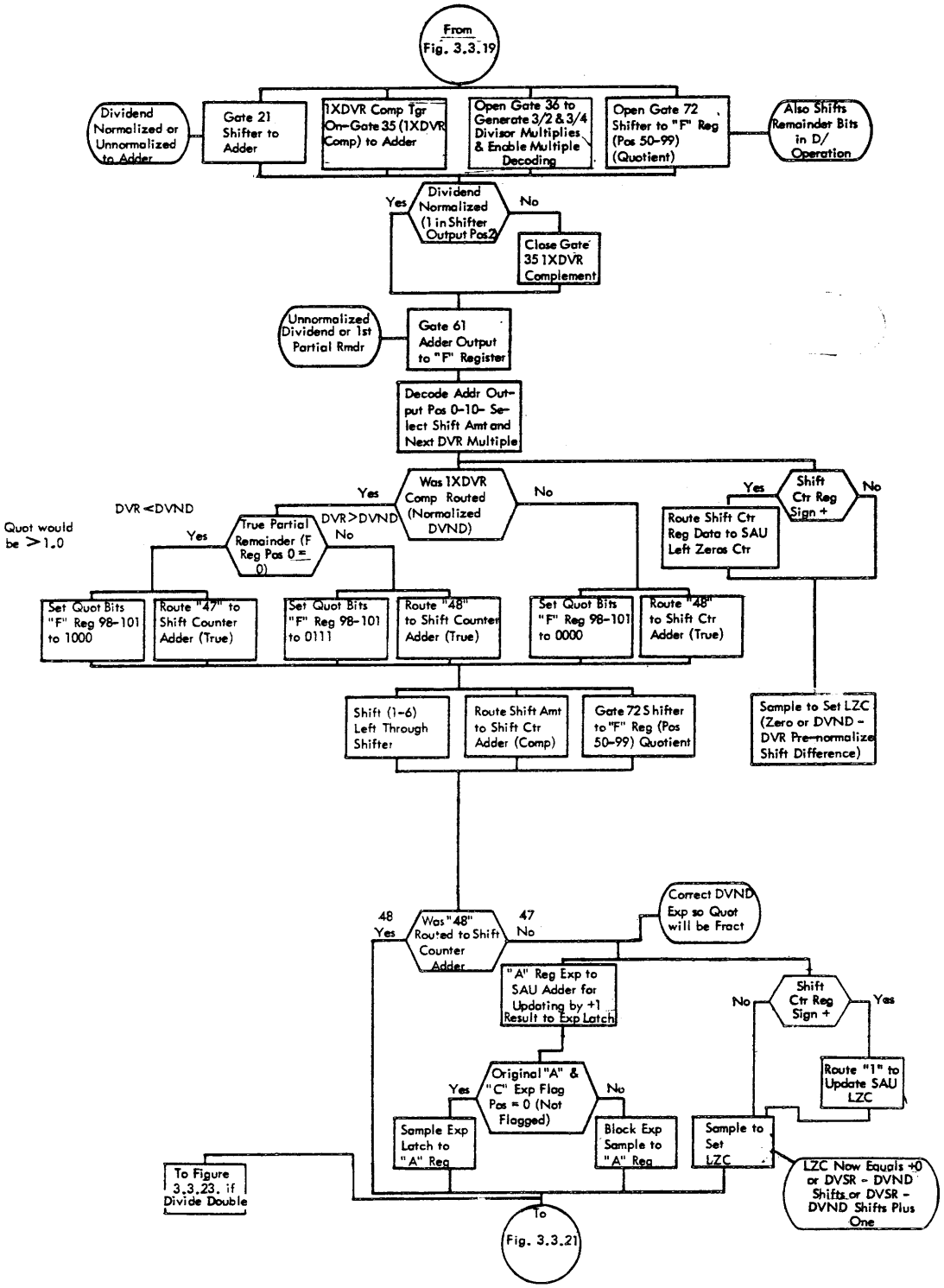


FIGURE 3.3.20. FLOATING-POINT DIVIDE (/), TRIAL REDUCTION CYCLE

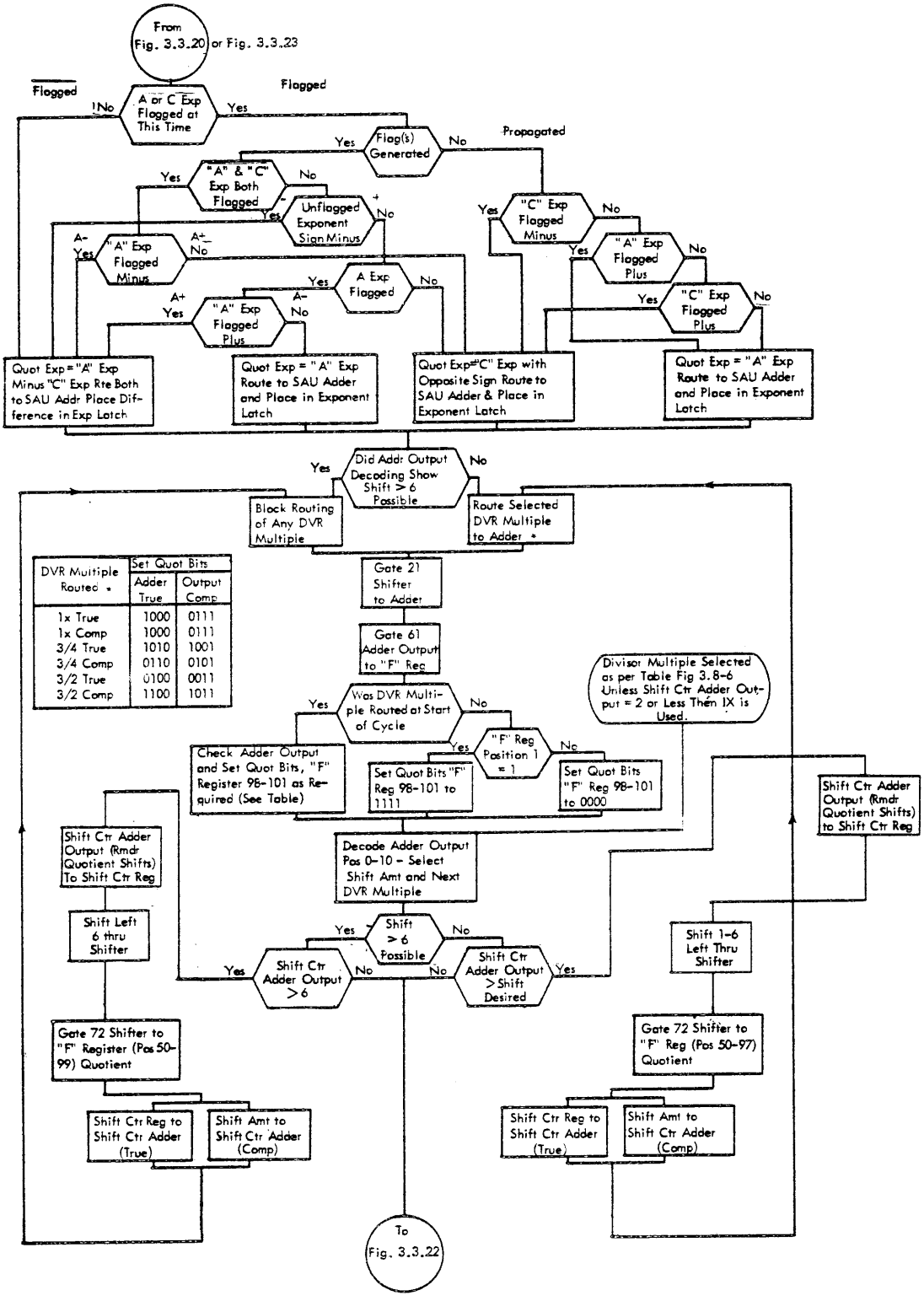


FIGURE 3.3.21. FLOATING-POINT DIVIDE (/), QUOTIENT EXPONENT DETERMINATION AND NORMAL REDUCTION CYCLES

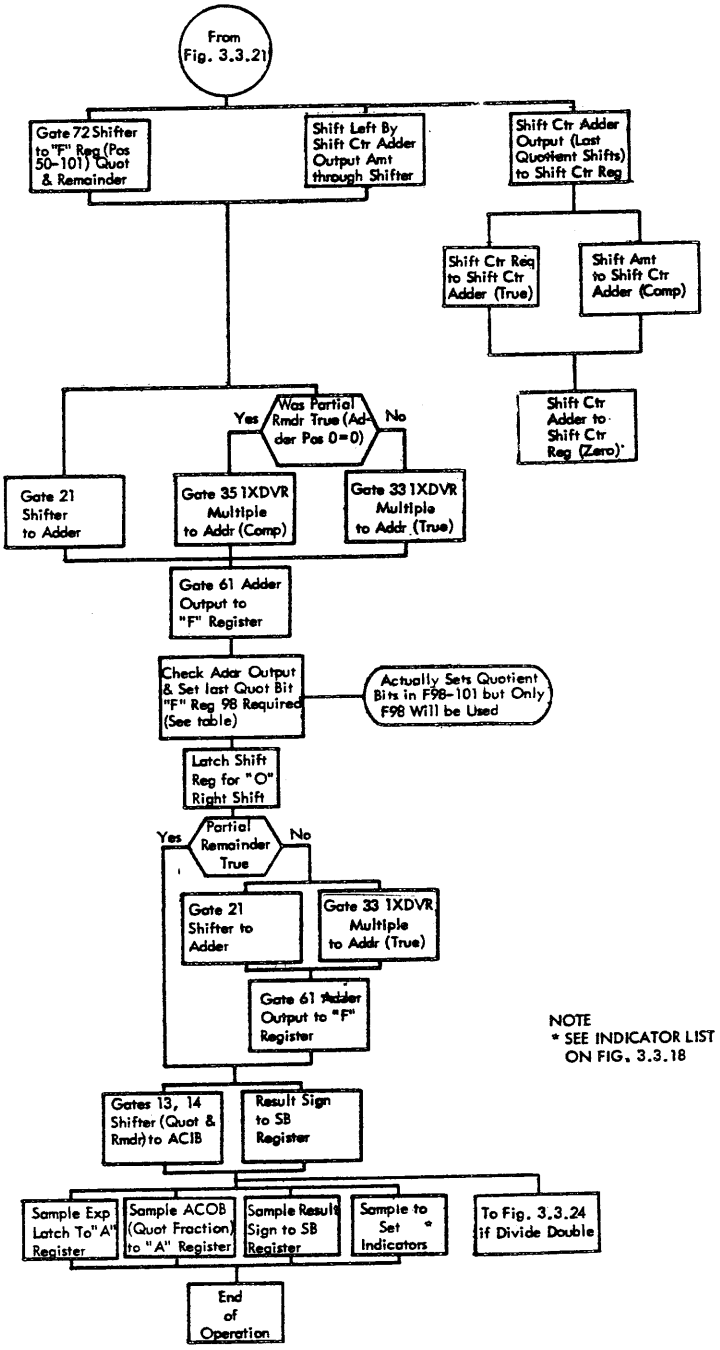


FIGURE 3.3.22. FLOATING-POINT DIVIDE (/), FINAL REDUCTION CYCLE

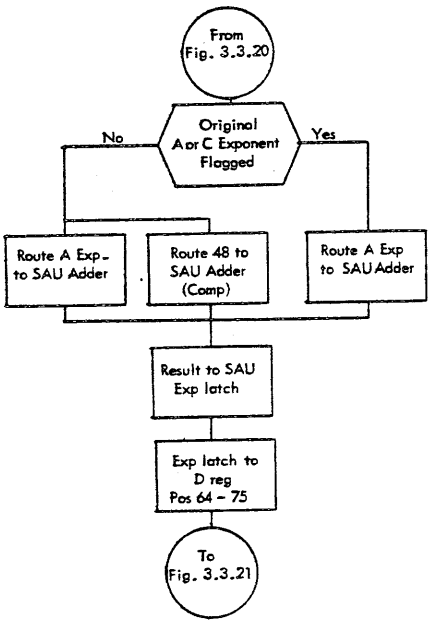


FIGURE 3.3.23. DIVIDE DOUBLE, DETERMINATION OF INTERMEDIATE REMAINDER EXPONENT

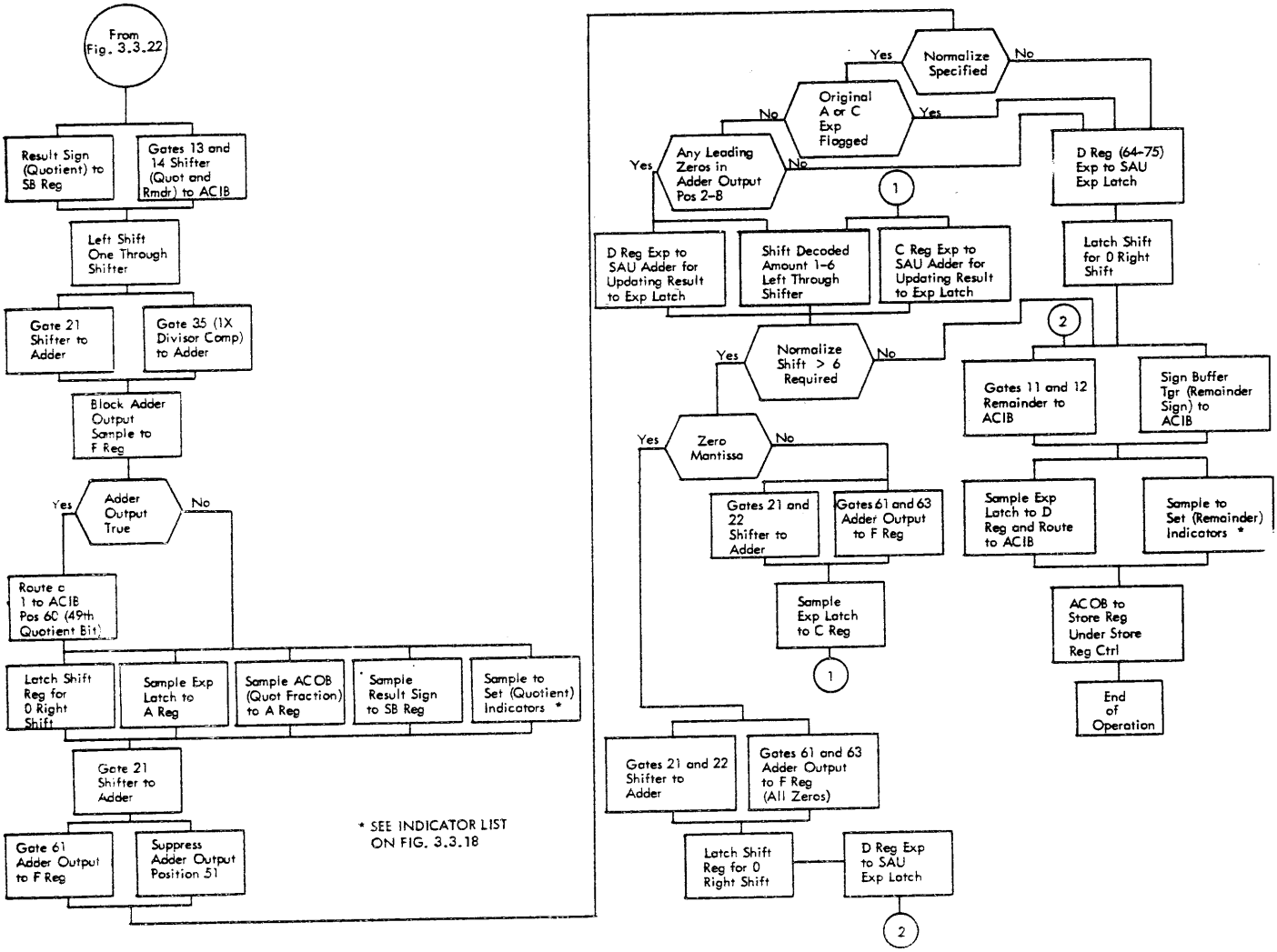


FIGURE 3.3.24. DIVIDE DOUBLE, DEVELOPMENT OF 49TH QUOTIENT BIT AND REMAINDER NORMALIZATION

TABLE 3.3.1. TRIGGERS AND ALD LOCATIONS FOR PAU

Sequencing Circuit	Trigger	Systems Page
Ring Triggers	T_0	61.02.50.1
	T_1	61.02.51.1
	T_2	61.02.52.1
	T_3	61.02.53.1
	T_4	61.02.54.1
	T_B	61.02.65.1
	T_C	61.02.57.1
	M_C	61.03.45.1
	MR1	61.03.51.1
	MR2	61.03.52.1
	MR3	61.03.53.1
	D_3	61.03.75.1
		61.03.76.1
	D_4	61.03.77.1
General Purpose Control Triggers	First Cycle Trigger	61.01.50.1
	Exponent Parity Handling	61.01.55.1
	Wait Trigger	61.01.56.1
	Interrupt End Operation	61.01.57.1
	Exponent and Indicator Latch	61.01.78.1
	Propagated Exponent Flag	61.02.36.1
	Phase Sample Tests Complete	61.02.70.1
	Not Phase Sample Tests Complete	61.02.71.1
	Interrupt Trigger	61.02.73
	Exponent Sample	61.02.78.1
	End Operation	61.02.99.1
	Test 1 Complete	61.04.20.1
	Test 2 Complete	61.04.20.1
	Test 3 Complete	61.04.20.1
	Test 4 Complete	61.04.20.1
	Master Test Complete	61.04.21.1

TABLE 3.3.1. TRIGGERS AND ALD LOCATIONS FOR PAU (cont'd)

Sequencing Circuit	Trigger	Systems Page
Exponent Control Triggers	Exponent Parity Handling	61.01.55.1
	Exponent and Indicator Latch	61.01.78.1
	Propagated Exponent Flag	61.02.36.1
	Exponent Routing Control (TP6)	61.02.76.1
	Bit Address = 64	61.02.82.1
	Write Exponent A	61.02.93.1
	Write Exponent C	61.02.94.1
	Write Exponent D	61.02.95.1
Special Purpose Triggers (not Multiply or Divide)	Pre-shift and Add	61.02.60.1
	Normalize Exponent	61.02.63.1
	Normalize Mantissa	61.02.64.1
	TX	61.02.65.1
	Signal SSQ to VFL	61.02.66.1
	Perform Augment	61.02.67.1
	Mantissa Routing Control	61.02.75.1
Multiply Control Triggers	Multiply	61.03.54.1
	Shift Right Twelve	61.03.55.1
	One X Multiplicand	61.03.56.1
	Gate S & T to PAU Adder (41, 42, 46)	61.03.57.1
	Cumulative Multiply	61.03.58.1
	Cumulative Multiply Exponent Adjust	61.03.59.1
	Cumulative Multiply Pre-Shift Exponent	61.03.60.1
	Lookahead Continue (Mpy & Add)	61.04.25.1
	Lookahead Reject (Mpy & Add)	61.04.25.1
Divide Control Triggers	Divide Normalize Exponent	61.03.63.1
	Divisor	61.03.64.1
	Dividend	61.03.65.1
	Dividend	61.03.66.1
	One X Complement	61.03.67.1
	Second Divide Cycle	61.03.69.1
	Divide Counter	61.03.70.1
	Final Divide	61.03.71.1
	Zero Dividend	61.03.72.1
	Interchange Reciprocal Divide	61.03.73.1

TABLE 3.3.1. TRIGGERS AND ALD LOCATIONS FOR PAU (cont'd)

Sequencing Circuit	Trigger	Systems Page
SAU Control Triggers (Floating Point Control)	SAU Divide Control	61.03.68.1
	VFL Divisor	61.03.80.1
Data Storage Control Triggers	Partial Field or Perform Aug. Remembered	61.01.79.1
	Overflow	61.02.68.1
	True/Complement	61.02.68.1
	Sign Buffer	61.02.69.1
	Shift > 96	61.02.77.1
	Shift > 48	61.02.77.1
	Shift Remembered A	61.03.02.1
	Shift Remembered B	61.03.02.1
Gate Control Triggers	Gate 21 (High Order True Shifter to Adder)	61.80.56.1
	Gate 22 (Low Order True Shifter to Adder)	61.80.57.1
	Gate 23 (Complement Shifter to Adder)	61.80.58.1
	Gate 61-63 (Adder to F Register)	61.81.66.1

TABLE 3.3.2. CONTROL LOGIC AREAS AND ALD LOCATIONS

Logic Area	Systems Page
Execute Register	61.01.06.1-
	61.01.10.1
Operation Decoding	61.01.13.1-
	61.01.21.1
Start Control	61.01.53.1-
	61.01.57.1
Sign Mixing	61.01.65.1-
	61.01.70.1
Indicators Result Setting	61.01.71.1-
	61.01.79.1
Zero Fraction Test	61.01.90.1
Exponent Flag Logic	61.02.30.1-
	61.02.38.1
Ring Triggers (General)	61.02.50.1-
	61.02.57.1
Add Type and Normalization Control Triggers	61.02.60.1- 61.02.68.1
Sampling and Latching Conditions	61.02.74.1-
	61.02.82.1
Exponent Routing Through WI Switch Matrix	61.02.93.1 -
	61.02.95.1
Noisy Mode Control	61.03.01.1
Arithmetic Checker Signals	61.03.02.1
Shift Control (A, B, C)	61.03.10.1
Multiply Logic	61.03.30.1-
	61.03.60.1
Divide Logic	61.03.63.1-
	61.03.80.1

TABLE 3.3.2. CONTROL LOGIC AREAS AND ALD LOCATIONS (cont'd)

Logic Area	Systems Page
Clock Powering (Frame 25)	61.04.01.1- 61.04.05.1
-N Reset Powering (Frame 25)	61.04.11.1- 61.04.15.1
Interrupt Logic	61.04.20.1- 61.04.26.1
F Register SCR, Counter Register Latch and Sample	61.71.80.1- 61.71.83.1
Frame 26 Gate Control and Powering	61.80.10.1- 61.80.95.1
Frame 27 Gate Control and Powering	61.81.01.1- 61.81.67.1
SAU Gating in Store Root and Converts	61.85.01.1
Frame 26 Clock Gating and Powering (F Register)	61.90.11.1- 61.90.20.1
Frame 27 Clock Gating and Powering	61.91.21.1

TABLE 3.3.3. FLOATING POINT INDICATORS

Indicator			
Bit	Code	Name	Indication
22	LC	Lost Carry	Set to 1 when a fraction overflow bit occurs during unnormalized addition. Set to 1 during unnormalized store; rounded if accumulator positions 12-60 equal 1. Set to 1 for shift fraction when a 1 bit is shifted left of accumulator position 12. Set to 1 if the low order bit of a 49-bit remainder during divide double is a 1.
23	PF	Partial Field	Set to 1 for unnormalized division when the magnitude of the dividend fraction is equal or greater than the magnitude of the divisor.
24	ZD	Zero Divisor	Set to 1 in division if the divisor fraction is 0.
25	IR	Imaginary Root	Set to 1 during Store Square Root when the accumulator sign is negative and the absolute modifier bit is 0.
26	LS	Lost Significance	Set to 1 for Add, Add Magnitude, Add to Memory, Add Magnitude to Memory, Add Double, Add Magnitude Double, and Add to Fraction if the result is zero except: 1. If both operands have zero fractions prior to addition. 2. If zero fraction is a forced zero. 3. If result exponent has a propagated flag.

TABLE 3.3.3. FLOATING POINT INDICATORS (cont'd)

Indicator			Indication
Bit	Code	Name	
27	(>PSH)	Preparatory Shift Greater than 48	Set to 1 for Add, Add to Memory, Add Magnitude, Add Magnitude to Memory, Add Double, Add Magnitude Double, Compare, Compare Magnitude, Compare for Range, and Compare Magnitude for Range if the exponent difference is greater than 48, except when the result exponent has a propagated flag.
28	(XPFP)	Exponent Flag Propagated	Set to 1 if the result exponent of a floating point operation has a propagated flag of 1.
29	XPO	Exponent Overflow	Set to 1 if the result exponent of a floating point operation has a generated flag of 1 and a sign of 0.
30	XPH	Exponent Range High	Set to 1 if the result exponent of a floating point operation has a flag of 0, a high point order magnitude bit of 1, and a sign of 0.
31	XPL	Exponent Range Low	Set to 1 if the result exponent of a floating point operation has a flag of 0, a high order magnitude bit of 0, a 1 in position 2, 3, or 4, and a sign of 0.
32	XPU	Exponent Underflow	Set to 1 if the result of a floating point operation has a generated flag of 1 and a sign of 1.
33	ZM	Zero Multiply	Set to 1 if the final result of a floating point multiply operation is an order of magnitude 0 with the exponent net in the XFO range.

TABLE 3.3.3. FLOATING POINT INDICATORS (cont'd)

Indicator			Indication
Bit	Code	Name	
34	RU	Remainder Underflow	Set to 1 for divide double if the remainder exponent has a generated flag of 1 and a sign of 1.
35 36 37	TF UF VF	Data Flags*	Set in accordance with the C register (storage) data flags bits at the end of each operation; not affected by Store, Store Rounded, Store Low Order, and Store Square Root.
55	MOP	To Memory Operations*	Set to 1 for all floating-point-to-memory operations. Set to 0 for all other floating point operations.
56	RLZ	Result Less than Zero*	Set to 1 if the fraction result of the floating point operation was non-zero negative (except compares). Set to 0 for any other case (except compares).
57	RZ	Result Zero*	Set to 1 if the fraction result of the floating point operation was 0 (except compares). Set to 0 for any other case (except compares).
58	RGZ	Result Greater than Zero*	Set to 1 if the fraction result of the floating point operation was non-zero positive (except compares). Set to 0 for any other case (except compares).
59	RN	Result Negative *	Set to 1 if the fraction result of a floating point operation is negative whether 0 or not (except compares). Set to 0 for any other case (except compares).

TABLE 3.3.3. FLOATING POINT INDICATORS (cont'd)

Indicator			Indication
Bit	Code	Name	
60	AL	Accumulator Low*	Set to 1 if the result of the floating point compare just executed was that the accumulator contents were less than the storage operand. Set to 0 by compare whose result was not low. Cannot be set by Compare Range instructions.
61	AE	Accumulator Equal*	Set to 1 if the result of the floating point compare just executed was that the accumulator contents were equal (within range on range instructions) to the storage operand. Set to 0 for other cases. Set in range instructions only if AH is already on.
62	AH	Accumulator High*	Set to 1 if the result of the floating point compare just executed was that the accumulator contents were greater than the storage operand. Set to 0 by any compare whose range is not high.

*Temporary indicators

The numbering of the various control gates in PAU was developed in the early design stages of PAU and, as modifications were made, some of the numbering was dropped in the ALD's. Some of the gates are now identified in the ALD's by a brief description of their function instead of by number. The number reference, however, is still highly useful.

TABLE 3.3.4. PAU DATA FLOW CONTROL GATES

Gate	Function	ALD Page
1	Gates AB register positions 12-59 to F register positions 2-49.	61.80.11
2	Gates AB register positions 60-107 to F register positions 50-97.	61.80.11
3	Gates C register positions 12-59 to F register positions 2-49.	61.80.12
11	Gates shifter positions 2-49 to ACIB positions 12-59 (second level).	61.80.70
12	Gates shifter positions 50-97 to ACIB positions 60-63 and 0-43, respectively (first level).	61.80.70
13	Gates shifter positions 2-49 to ACIB positions 60-63 and 0-43, respectively (first level) (called crossover gate).	61.80.71
14	Gates shifter positions 51-98 to ACIB positions 12-59 (second level) (called crossover gate).	61.80.71
17	Gates shifter positions 98-101 to spill residue generator.	61.80.95
21-PAU	Gates shifter positions 0-51 to main adder positions 0-51 (true).	61.80.56
21-VFL	Gates shifter positions 0-49 to main adder positions 0-49 (true).	61.80.60
22	Gates shifter positions 52-99 to main adder positions 52-99 (true).	61.80.57
23	Gates shifter positions 0-97 to main adder positions 0-97 (complement).	61.80.58
25	Gates shifter positions 2-48 to main adder positions 51-97 (complement); also sets main adder inputs 98 and 99A and 50B to 1. Used in Store Square Root.	61.80.90
31	Gates AB register positions 12-59 to main adder positions 2-49 (true).	61.81.20

TABLE 3.3.4. PAU DATA FLOW CONTROL GATES (cont'd)

Gate	Function	ALD Page
32	Gates AB register positions 60-107 to main adder positions 50-97 (true).	61.81.20
33	Gates C register positions 12-59 to main adder positions 2-49 (true).	61.81.21
34	Gates D register positions 12-59 to main adder positions 2-49 (true).	61.81.31.1
35	Gates C register positions 12-59 to main adder positions 2-49 (complement).	65.04.92
36	Gates C register positions 12-59 to main adder positions 54-100 and 55-102 (true). Multiply and divide multiple generation.	61.81.04
37	Gates D register to multiple generation circuits.	61.81.31.1
41 and 42	Gates S and T register positions 2-61 to main adder positions 2-61 (multiply).	61.03.57
43	Gates S register positions 50-61 to F register positions 1-12; activated by gate 47 (multiply).	68.12.01
44	Gates T register positions 50-61 to F register positions 62-73; activated by gate 47 (multiply).	68.12.01
46	Gates F register positions 1-36 to main adder positions 62-97 (multiply).	61.81.02
47	Gates F register positions 1-37 and 62-85 to F register positions 13-49 and 74-97, respectively. Shift right 12 gate (multiply).	61.03.55
51	Gates main adder positions 53-102 to main adder positions 1-50 (true) (divide 3/2 multiple).	65.04.63
52	Gates main adder positions 53-102 to main adder positions 1-50 (complement) (divide 3/2 multiple).	65.04.63
53	Gates main adder positions 53-102 to main adder positions 2-51 (true) (divide 3/4 multiple).	65.04.62
54	Gates main adder positions 53-102 to main adder positions 2-51 (complement) (divide 3/4 multiple).	65.04.62
61	Gates main adder positions 0-51 to F register positions 0-51.	61.81.67

TABLE 3.3.4. PAU DATA FLOW CONTROL GATES (cont'd)

Gate	Function	ALD Page
62	Suppresses positions 50 and 51 of gate 61 or 63.	61.81.67
63	Gates main adder positions 49-99 to F register positions 49-99.	61.81.67
71	Gates shifter positions 0-49 to F register positions 0-49 (preshift gate).	61.80.80
72	Gates shifter positions 50-97 to F register positions 50-97 (preshift gate).	61.80.80
73	Suppresses bits 98 and 99 of gate 72. Used in divide. It is actually a NQ Divide line and is not labeled 73.	61.80.80
81	Effectively gates F register positions 2-97 offset to main adder positions 2-96 as double inputs and F register positions 98-101 to special adder input positions 95-98. For example, F97 goes to adder 96 and 94, F96 goes to adder 95 and 93, etc. (VFL dec - bin convert).	61.80.30
82	Gates adjust decoder output to main adder positions 3, 7, 11---- 87, 91, 95 (VFL bin - dec convert).	61.80.55
91	Gates SAU-AB switch matrix positions 1-8 to F register positions 2-9 (VFL).	61.80.40
92	Gates SAU-CD switch matrix positions 1-8 to F register positions 2-9 (VFL).	61.80.40
93	Gates SAU-CD switch matrix 1-8 to F register positions 50-57 (VFL multiply).	61.80.40
94	Gates SAU-AB switch matrix positions 1-4 to F register positions 98-101 (VFL).	61.80.50
95	Gates SAU-CD switch matrix positions 1-4 to F register positions 98-101 (VFL).	61.80.50
97	Gates F register positions 90-97 to SAU-CD second level true/complement positions 1-8 (VFL).	61.80.50

Note: Gates 81 through 97 are serial arithmetic gates activated by SAU to control VFL operations that utilize PAU circuits. No 90-series gates are labeled as such in the ALD's.

DESCRIPTION

This category contains a list of all 7101 CE console indicators and a copy of the CPU Scan Card formats. These two items fully identify each CE console indicator and cross-reference each console indicator location with its associated CPU Scan Card punch location, for machine type 7101, Serial No. 30,004 and higher.

The console indicators are listed in table 3.4.1 in sequential console co-ordinate notation. To shorten the length of the table, only the first and last indicators of any register, counter, etc., are identified. The intervening indicators are associated with similarly positioned bits of the register or counter and with similarly positioned punch positions on the CPU Scan Card.

The indicator locations noted in table 3.4.1 and in figures 3.4.1 through 3.4.4 do not include the common CPU frame and panel (frame 31, panel A) designations.

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
1A031 THROUGH 1A040	47.01.01.1	ACIB PARITY ERROR FOR POSITIONS 00-07, 08-11, 12-15, 16-23, 24-31, 32-39, 40-47, 48-55, 56-59 AND 60-63	4	12	11-8
1A043	48.02.01.1	ADD TYPE CHECK	4	11	12
1A044	48.02.01.1	COMPARE TYPE CHECK	4	11	11
1A045	48.02.01.1	LOAD OR STORE TYPE CHECK	4	11	0
1A046	48.02.01.1	MULTIPLY TYPE CHECK	4	11	1
1A047	48.02.01.1	DIVIDE TYPE CHECK	4	11	2
1A048	48.02.01.1	STORE ROOT CHECK	4	11	3
1A049	48.03.01.1	DOUBLE PRECISION CHECK	4	11	4
1A050	48.03.01.1	TO MEMORY TYPE CHECK	4	11	5
1A051	48.03.01.1	SERIAL ARITHMETIC UNIT OP CHK	4	11	6
1A052	48.03.01.1	UNNORMALIZED MODE	4	11	7
1A053	48.02.01.1	STORE MULTIPLIER TYPE CHK	4	11	8
1A054	48.02.01.1	LOAD MULTIPLIER TYPE CHK	4	11	9
1A055	48.02.01.1	EXTERNAL STORE INDICATOR	4	12	12
1A058	47.04.01.1	RESIDUE ERROR HAS OCCURRED	4	12	9
1A059	47.04.01.1	PARITY ERROR HAS OCCURRED	4	13	12
1A066	48.04.42.1	DATA AT FIRST LEVEL LATCH BEING HELD	4	4	6
1A067	48.04.42.1	DATA AT FIRST SECOND LATCH BEING HELD	4	4	7
1A068	48.04.45.1	EXPONENT BEING HELD ON A-BUS	4	4	8
1A069	48.04.45.1	GENERATE RESIDUE BEING HELD	4	4	9
1A070	48.04.41.1	DATA BEING GATED OUT OF A	4	5	12
1A071	48.04.41.1	DATA BEING GATED OUT OF B	4	5	11
1A072	48.04.41.1	DATA BEING PASSED FROM FIRST TO SECOND LEVEL	4	5	0
1A073	48.04.11.1	DATA FROM CD BEING LATCHED ON BUS	4	5	1
1A074	48.04.43.1	DOUBLE PRECISION TRANSFER NO CHECK	4	5	2
1A075	48.04.43.1	BINARY MULTIPLY CUMULATIVE OPERATION	4	5	3
1A077	48.04.44.1	BUS RESIDUE SENT TO INITIAL RESIDUE REGISTER	4	5	4
1A078	48.04.44.1	ENABLE FULL WORD PARITY ERROR	4	5	5
1B001	56.21.21.1	COMPLEMENT BYTE FROM AB	3	63	6
1B002	56.21.11.1	CUT OFF BYTE FROM CD	3	63	7
1B003	56.21.31.1	CLOSE CD TRUE-COMP TO BYTE SIZE	3	63	8
1B004	56.21.32.1	PARTIAL BYTE TRIGGER	3	63	9
1B005	56.21.21.1	COMPLEMENT BYTE FROM CD	3	64	12
1B006	56.21.21.1	CUTOFF BYTE FROM CD	3	64	11
1B007	56.51.02.1	BINARY END OF A 1 TRIGGER	3	64	0
1B008	56.15.01.1	LIKE SIGNS TRIGGER	3	64	1
1B009	56.23.03.1	MAIN VFL CARRY TRIGGER	3	64	2
1B011	56.52.01.1	AB LESS THAN CD	3	64	4
1B012	56.52.01.1	AB GREATER THAN OR EQUAL TO CD	3	64	5
1B013	56.52.01.1	AB GREATER THAN CD	3	64	6
1B022 THROUGH 1B027	56.12.10.1	DIVIDE TYPE CYCLE 1 TO 6	3	65	3-8
1B031 THROUGH 1B040	41.03.01.1 THROUGH 41.03.06.1	ACIB PARITY FOR POSITIONS 00-07, 08-11, 12-15, 16-23, 24-31, 32-39, 40-47, 48-55, 56-59, and 60-63	4	1	12-7
1B043	42.01.08.1	GENERATED RESIDUE FIRST LEVEL 0-43 (2)	4	1	8
1B044	42.01.08.1	GENERATED RESIDUE FIRST LEVEL 0-43 (1)	4	1	9
1B045	42.02.08.1	GENERATED RESIDUE SECOND LEVEL 12-59 (2)	4	2	12
1B046	42.02.08.1	GENERATED RESIDUE SECOND LEVEL 12-59 (1)	4	2	11
1B047	45.02.02.1	PREDICTED RESIDUE EQUALS 2	4	2	0
1B048	45.02.02.1	PREDICTED RESIDUE EQUALS 1	4	2	1
1B049	45.02.02.1	DIVISOR RESIDUE EQUALS 2	4	2	2
1B050	45.02.02.1	DIVISOR RESIDUE EQUALS 1	4	2	3
1B051	45.02.03.1	SPILL RESIDUE EQUALS 2	4	2	4
1B052	45.02.03.1	SPILL RESIDUE EQUALS 1	4	2	5
1B053	48.04.21.1	PARITY ON AB 44-47 108-111 EQUALS ONE	4	2	6
1B054	48.03.01.1	DIVIDE OVERFLOW	4	2	7
1B055	48.03.01.1	NOT NOISY MODE	4	2	8
1B056	48.03.01.1	NORMALIZATION SHIFT WAS EVEN	4	2	9
1B057	48.03.01.1	SUM SIGN IS NEGATIVE	4	3	12
1B058	48.03.01.1	LOST CARRY	4	3	11

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
1B059	48.03.01.1	RESULT EQUALS ZERO	4	3	0
1B060	48.03.01.1	SPILL SIGN IS POSITIVE	4	3	1
1B066	48.04.11.1	CHECK CYCLE TIME 1	4	3	4
1B067	48.04.11.1	CHECK CYCLE TIME 2	4	3	5
1B068	48.04.11.1	CHECK CYCLE TIME 3	4	3	6
1B070	48.04.21.1	UPDATING TIME 1	4	3	8
1B071	48.04.21.1	UPDATING TIME 2	4	3	9
1B075	48.04.31.1	ERROR INTERLOCK TIME 1	4	4	1
1B076	48.04.31.1	ERROR INTERLOCK TIME 2	4	4	2
1B078	48.04.31.1	CHECK COMPLETE	4	4	4
1B087	53.51.12.1	PRE LATCH 2, BITS 01-16 TO CONTROL	3	58	4-9
THROUGH 1B102	THROUGH 53.51.15.1 53.51.01.1 THROUGH 53.51.09.1 AND 53.51.16.1		3	59	12-7
1C033	55.10.01.1	WBC EXECUTION REGISTER POS 00	3	36	11
1C034	55.10.01.1	BOB EXECUTION REGISTER POS 01	3	36	0
1C035	55.10.01.1	1B EXECUTION REGISTER POS 02	3	36	1
1C036	55.10.01.1	SAU EXECUTION REGISTER POS 03-24	3	36	2-9
THROUGH 1C057	THROUGH 55.10.07.1		3	36	12-9
1C058	55.10.07.1	INV BIT EXECUTION REGISTER POS 25	3	38	12-11
1C059	55.10.07.1	ZERO BIT EXECUTION REGISTER POS 26	3	38	0
1C060	55.10.07.1	BR IF ON EXECUTION REGISTER POS 27	3	38	1
1C061	55.10.08.1	UNS EXECUTION REGISTER POS 28	3	38	2
1C062	55.10.08.1	INV EXECUTION REGISTER POS 29	3	38	3
1C063	55.10.08.1	DEC EXECUTION REGISTER POS 30	3	38	4
1C064	55.10.08.1	OP A EXECUTION REGISTER POS 31	3	38	5
1C065	55.10.09.1	OP B EXECUTION REGISTER POS 32	3	38	6
1C066	55.10.09.1	OP C EXECUTION REGISTER POS 33	3	38	7
1C067	55.10.09.1	OP D EXECUTION REGISTER POS 34	3	38	8
1C068	55.10.09.1	OP E EXECUTION REGISTER POS 35	3	38	9
1C069	55.10.10.1	IRPT EXECUTION REGISTER POS 36	3	39	12
1C080	59.06.04.1	SAU RESIDUE ERROR TRIGGER	3	39	11
1C081	59.06.04.1	SAU LOGICAL UNIT COMPARISON ERROR TRIGGER	3	61	5
1C082	59.06.04.1	SAU AB READOUT PARITY ERROR TRIGGER	3	61	6
1C083	59.06.04.1	SAU CD READOUT PARITY ERROR TRIGGER	3	61	7
1C084	59.06.04.1	SAU SWITCH MATRIX IN PARITY ERROR TRIGGER	3	61	8
1C087	53.01.12.1	PRE LATCH 1, BITS 01-16 TO CONTROL	3	61	9
THROUGH 1C102	THROUGH 53.01.15.1 53.06.01.1 THROUGH 53.06.11.1 AND 53.06.16.1		3	57	0-9
1D001	56.16.00.1	HOUSEKEEPING	2	68	2
1D002	56.11.00.1	ROUND SET UP	2	68	3
1D003	56.11.00.1	ROUND CYCLE	2	68	4
1D004	56.14.10.1	TEST BIT	3	59	8
1D006	56.11.10.1	SET UP FOR RECOMPLEMENT	3	60	12
1D007	56.11.10.1	RECOMPLEMENT	3	60	11
1D008	56.11.10.1	ZERO AB	3	60	0
1D010	56.14.00.1	SET UP FOR STORE SQUARE ROOT	3	62	0
1D011	56.14.00.1	STORE SQUARE ROOT SEQ TRIG	3	62	1
1D012	56.14.00.1	PAU DO STORE SQUARE ROOT	3	62	2

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
1D014	56.51.30.1	ZERO DIVIDE TRIGGER	3	62	4
1D015	56.51.20.1	PARTIAL FIELD ADD TRIGGER	3	62	5
1D016	56.51.02.1	PARTIAL FIELD CONNECT TRIGGER	3	62	6
1D017	56.15.05.1	NON ZERO RESULT TRIGGER	3	62	7
1D019	56.12.00.1	MULTIPLY TYPE CYCLES 1, 2, & 3	3	62	9
THROUGH 1D021			3	63	12-11
1D023	56.12.05.1	CUMULATIVE MULTIPLY TYPE CYCLES 1, 2, 3, 4, & 5	3	63	1-5
THROUGH 1D027					
1D031	51.70.01.1	D REGISTER POS 00-07 TO INDICATORS D064 - D071 RESPECTIVELY	2	61	12-5
THROUGH 1D038	51.70.02.1				
1D039	59.51.20.1	PARITY FOR D REGISTER POS 00-07	2	66	2
1D040	51.70.03.1	D REGISTER POS 08-11 TO INDICATORS D072- D075 RESPECTIVELY	2	61	6-9
THROUGH 1D043					
1D044	59.51.20.1	PARITY FOR D REGISTER POS 08-11	2	66	3
1D045	51.70.04.1	D REGISTER POS 12-15 TO INDICATORS D076 - D079 RESPECTIVELY	2	62	12-1
THROUGH 1D048					
1D049	59.51.20.1	PARITY FOR D REGISTER POS 12-15	2	66	4
1D050	51.70.05.1	D REGISTER POS 16-23 TO INDICATORS D080 - D087 RESPECTIVELY	2	62	2-9
THROUGH 1D057	AND 51.70.06.1				
1D058	59.51.20.1	PARITY FOR D REGISTER POS 16-23	2	66	.5
1D059	51.70.07.1	D REGISTER POS 24-31 TO INDICATORS D088 - D095 RESPECTIVELY	2	63	12-5
THROUGH 1D066	AND 51.70.08.1				
1D067	59.51.21.1	PARITY FOR D REGISTER POS 24-31	2	66	6
1D068	51.70.09.1	D REGISTER 32-39 TO INDICATORS D096 - D103 RESPECTIVELY	2	63	6-9
THROUGH 1D075			2	64	12-1
1D076	59.51.21.1	PARITY FOR D REGISTER POS 32-39	2	66	7
1D077	51.70.11.1	D REGISTER POS 40-47 TO INDICATORS D104 - D 111 RESPECTIVELY	2	64	2-9
THROUGH 1D084	AND 51.70.12.1				
1D085	59.51.21.1	PARITY FOR D REGISTER POS 40-47	2	66	8
1D086	51.70.13.1	D REGISTER POS 48-55 TO INDICATORS D112 - D119 RESPECTIVELY	2	65	12-5
THROUGH 1D093	AND 51.70.14.1				
1D094	59.51.21.1	PARITY FOR D REGISTER POS 48-55	2	66	9
1D095	51.70.15.1	D REGISTER POS 56-59 TO INDICATORS D120 - D123 RESPECTIVELY	2	65	6-9
THROUGH 1D098					
1D099	59.51.22.1	PARITY FOR D REGISTER POS 56-59	2	67	12
1D100	51.70.16.1	D REGISTER POS 60-63 TO INDICATORS D124 - D127 RESPECTIVELY	2	66	12-1
THROUGH 1D103					
1D104	59.51.22.1	PARITY FOR D REGISTER POS 60-63	2	67	11
1E031	51.60.01.1	C REGISTER POS 00-07	2	51	12-5
THROUGH 1E038	AND 51.60.02.1				
1E039	59.51.10.1	PARITY FOR C REGISTER POS 00-07	2	56	2
1E040	51.60.03.1	C REGISTER POS 08-11	2	51	6-9
THROUGH 1E043					
1E044	59.51.10.1	PARITY FOR C REGISTER POS 08-11	2	56	3
1E045	51.60.04.1	C REGISTER POS 12-15	2	52	12-1
THROUGH 1E048					

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATOR	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
1E049	59.51.10.1	PARITY FOR C REGISTER POS 12-15	2	56	4
1E050	51.60.05.1	C REGISTER POS 16-23	2	52	2-9
THROUGH	AND				
1E057	51.60.06.1				
1E058	59.51.10.1	PARITY FOR C REGISTER POS 16-23	2	56	5
1E059	51.60.07.1	C REGISTER POS 24-31	2	53	12-5
THROUGH	AND				
1E066	51.60.08.1				
1E067	59.51.11.1	PARITY FOR C REGISTER POS 24-31	2	56	6
1E068	51.60.09.1	C REGISTER POS 32-39	2	53	6-9
THROUGH	AND				
1E075	51.60.10.1		2	54	12-1
1E076	59.51.11.1	PARITY FOR C REGISTER POS 32-39	2	56	7
1E077	51.60.11.1	C REGISTER POS 40-47	2	54	2-9
THROUGH	AND				
1E084	51.60.12.1				
1E085	59.51.11.1	PARITY FOR C REGISTER POS 40-47	2	56	8
1E086	51.60.13.1	C REGISTER POS 48-55	2	55	12-5
THROUGH	AND				
1E093	51.60.14.1				
1E094	59.51.11.1	PARITY FOR C REGISTER POS 48-55	2	56	9
1E095	51.60.15.1	C REGISTER POS 56-59	2	55	6-9
THROUGH					
1E098					
1E099	59.51.12.1	PARITY FOR C REGISTER POS 56-59	2	57	12
1E100	51.60.16.1	C REGISTER POS 60-63	2	56	12-1
THROUGH					
1E103					
1E104	59.51.12.1	PARITY FOR C REGISTER POS 60-63	2	57	11
1F001	56.16.00.1	VFL OPERATION	2	59	1
1F002	56.11.00.1	HANDLE SIGN BYTE	2	59	2
1F003	56.11.06.1	PIPELINE 1	2	59	3
1F004	56.11.06.1	PIPELINE 2	2	59	4
1F005	54.38.03.1	END OF C 1	2	59	5
1F006	54.38.03 1	END OF C 2	2	59	6
1F007	54.38.01.1	RFL CARRY TRIGGER	2	59	7
1F008	54.18.01.1	END OF A 2	2	59	8
1F009	54.19.04.1	END OF HIGH ORDER MARK 2	2	59	9
1F010	56.11.06.1	SET INDICATORS AND RESET	2	60	12
1F012	56.14.00.1	RESET ONLY	2	60	0
1F014	56.13.10.1	SET UP FOR AB TO F HIGH	2	67	0
1F015	56.13.10.1	TRANSFER AB TO F HIGH ORDER FIRST	2	67	1
1F016	56.13.10.1	SET UP FOR CD TO F HIGH	2	67	2
1F017	56.13.10.1	TRANSFER CD TO F HIGH ORDER FIRST	2	67	3
1F018	56.13.00.1	SET UP FOR CD TO F LOW	2	67	4
1F019	56.13.00.1	TRANSFER CD TO F LOW ORDER FIRST	2	67	5
1F020	56.13.05.1	SET UP FOR F TO CD	2	67	6
1F021	56.13.05.1	SIGN OF C TO D POS 127	2	67	7
1F022	56.13.05.1	TRANSFER F TO CD BYTE BY BYTE	2	67	8
1F023	56.13.15.1	SET UP FOR F TO AB AT OFFSET	2	67	9
1F024	56.13.15.1	TRANSFER F TO AB STARTING AT OFFSET	2	68	12
1F025	56.13.20.1	PARALLEL XFR F TO AB FIRST CYCLE	2	68	11
1F026	56.13.20.1	PARALLEL XFR F TO AB SECOND CYCLE	2	68	0
1F027	56.13.20.1	PARALLEL XFR F TO CD POS 12-59	2	68	1
1F045	54.60.06.1	SIGN OF CD REGISTER POS 00(S), 01(T), 02(U), AND 03(V)	2	57	0-3
THROUGH					
1F048					
1F055	54.26.01.1	READ OUT BIT ADDRESS CD POS 64, 32, 16, 8, 4, 2, & 1	2	57	4-9
THROUGH					
1F061				58	12

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
1F064	54.26.02.1	WRITE IN BIT ADDRESS CD POS 64, 32, 16, 8, 4, 2, & 1	2	58	11-5
THROUGH					
1F070					
1F073	54.36.02.1	RESIDUAL FIELD LENGTH REGISTER POS 64, 32, 16, 8, 4, 2 & 1	2	49	7-9
THROUGH				50	12-1
1F079					
1F093	45.01.02.1	RESIDUE 2 - VFL MD	4	13	11
1F094	45.01.02.1	RESIDUE 1 - VFL MD	4	13	0
1F095	45.01.02.1	RESIDUE OF C REGISTER BITS 12-59 EQUALS 2	2	58	6
1F096	45.01.02.1	RESIDUE OF C REGISTER BITS 12-59 EQUALS 1	2	58	7
1F097	45.01.02.1	RESIDUE OF CUM MCD BITS 12-59 EQUALS 2	2	58	8
1F098	45.01.02.1	RESIDUE OF CUM MCD BITS 12-59 EQUALS 1	2	58	9
1F101	59.56.03.1	CD RESIDUE REGISTER POS 2	2	59	12
1F102	59.56.03.1	CD RESIDUE REGISTER POS 1	2	59	11
1F103	59.56.03.1	CD RESIDUE REGISTER POS 0	2	59	0
1G031	51.30.01.1	B REGISTER POS 00-07 TO INDICATORS B064-B071	3	51	12-5
THROUGH	AND	RESPECTIVELY			
1G038	51.30.02.1				
1G039	59.01.50.1	PARITY FOR B REGISTER POS 00-07	3	56	2
1G040	51.30.03.1	B REGISTER POS 08-11 TO INDICATORS B072-B075	3	51	6-9
THROUGH		RESPECTIVELY			
1G043					
1G044	59.01.20.1	PARITY FOR B REGISTER POS 08-11	3	56	3
1G045	51.30.04.1	B REGISTER POS 12-15 TO INDICATORS B076-B079	3	52	12-1
THROUGH		RESPECTIVELY			
1G048					
1G049	59.01.20.1	PARITY FOR B REGISTER POS 12-15	3	56	4
1G050	51.30.05.1	B REGISTER POS 16-23 TO INDICATORS B080-B087	3	52	2-9
THROUGH	AND	RESPECTIVELY			
1G057	51.30.06.1				
1G058	59.01.20.1	PARITY FOR B REGISTER POS 16-23	3	56	5
1G059	51.30.07.1	B REGISTER POS 24-31 TO INDICATORS B088-B095	3	53	12-5
THROUGH	AND	RESPECTIVELY			
1G066	51.30.08.1				
1G067	59.01.21.1	PARITY FOR B REGISTER POS 24-31	3	56	6
1G068	51.30.09.1	B REGISTER POS 32-39 TO INDICATORS B096-B103	3	53	6-9
THROUGH	AND	RESPECTIVELY			
1G075	51.30.10.1		3	54	12-1
1G076	59.01.21.1	PARITY FOR B REGISTER POS 32-39	3	56	7
1G077	51.30.11.1	B REGISTER POS 40-47 TO INDICATORS B 104-B111	3	54	2-9
THROUGH	AND	RESPECTIVELY			
1G084	51.30.12.1				
1G085	59.01.21.1	PARITY FOR B REGISTER POS 40-47	3	56	8
1G086	51.30.13.1	B REGISTER POS 48-55 TO INDICATORS B112-B119	3	55	12-5
THROUGH	AND	RESPECTIVELY			
1G093	51.30.14.1				
1G094	59.01.21.1	PARITY FOR B REGISTER POS 48-55	3	56	9
1G095	51.30.15.1	B REGISTER POS 56-59 TO INDICATORS B120-B123	3	55	6-9
THROUGH		RESPECTIVELY			
1G098					
1G099	59.01.22.1	PARITY FOR B REGISTER POS 56-59	3	57	12
1G100	51.30.16.1	B REGISTER POS 60-63 TO INDICATORS B124-B127	3	56	12-1
THROUGH		RESPECTIVELY			
1G103					
1G104	59.01.22.1	PARITY FOR B REGISTER POS 60-63	3	57	11
1H023	61.02.75.1	MANTISSA ROUTING CONTROL	4	35	4
1H025	65.03.39.1	COUNTER EQUAL ZERO	3	62	12
1H027	65.03.39.1	COUNT TO ZERO	3	62	11
1H031	51.20.01.1	A REGISTER POS 00-07	3	41	12-5
THROUGH	AND				
1H038	51.20.02.1				
1H039	59.01.10.1	PARITY FOR A REGISTER POS 00-07	3	46	2

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
1H040 THROUGH 1H043	51.20.03.1	A REGISTER POS 08-11	3	41	6-9
1H044	59.01.10.1	PARITY FOR A REGISTER POS 08-11	3	46	3
1H045 THROUGH 1H048	51.20.04.1	A REGISTER POS 12-15	3	42	12-1
1H049	59.01.10.1	PARITY FOR A REGISTER POS 12-15	3	46	4
1H050 THROUGH 1H057	51.20.05.1 AND 51.20.06.1	A REGISTER POS 16-23	3	42	2-9
1H058	59.01.10.1	PARITY FOR A REGISTER POS 16-23	3	46	5
1H059 THROUGH 1H066	51.20.07.1 AND 51.20.08.1	A REGISTER POS 24-31	3	43	12-5
1H067	59.01.11.1	PARITY FOR A REGISTER POS 24-31	3	46	6
1H068 THROUGH 1H075	51.02.09.1 AND 51.20.10.1	A REGISTER POS 32-39	3	43	6-9
			3	44	12-1
1H076	59.01.11.1	PARITY FOR A REGISTER POS 32-39	3	46	7
1H077 THROUGH 1H084	51.20.11.1 AND 51.20.12.1	A REGISTER POS 40-47	3	44	2-9
1H085	59.01.11.1	PARITY FOR A REGISTER POS 40-47	3	46	8
1H086 THROUGH 1H093	51.20.13.1 AND 51.20.14.1	A REGISTER POS 48-55		45	12-5
1H094	59.01.11.1	PARITY FOR A REGISTER POS 48-55	3	46	9
1H095 THROUGH 1H098	51.20.15.1	A REGISTER POS 56-59	3	45	6-9
1H099	59.01.12.1	PARITY FOR A REGISTER POS 56-59	3	47	12
1H100 THROUGH 1H103	51.20.16.1	A REGISTER POS 60-63	3	46	12-1
1H104	59.01.12.1	PARITY FOR A REGISTER POS 60-63	3	47	11
1J045 THROUGH 1J048	54.60.03.1	SIGN OF AB REGISTER POS 00, 01, 02, 03	3	47	0-3
1J049 THROUGH 1J052	54.60.04.1	SIGN OF AB REGISTER POS 04(S), 05(T), 06(U), AND 07(V)	3	47	4-7
1J055 THROUGH 1J061	54.16.01.1	READ OUT BIT ADDRESS AB POS 64, 32, 16, 08, 04, 02 & 01	3	47	8-9
			3	48	12-2
1J064 THROUGH 1J070	54.16.02.1	WRITE IN BIT ADDRESS AB POS 64, 32, 16, 08, 04, 02 & 01	3	48	3-9
1J073 THROUGH 1J079	54.45.01.1	LEFT ZEROS COUNT REGISTER POS 01-07 TO INDICATORS 64, 32, 16, 08, 04, 02 & 01	3	49	7-9
			3	50	12-1
1J082 THROUGH 1J088	54.45.01.1	ALL ONES COUNT REGISTER POS 01-07 TO INDICATORS 64, 32, 16, 08, 04, 02, AND 01.	3	61	12-4
1J093	45.01.01.1	RESIDUE OF AB REGISTER POS 12-59 EQUALS 2	3	49	12
1J094	45.01.01.1	RESIDUE OF AB REGISTER POS 12-59 EQUALS 1	3	49	11
1J095	45.01.01.1	RESIDUE OF AB REGISTER POS 60-63 EQUALS 2	3	49	0
1J096	45.01.01.1	RESIDUE OF AB REGISTER POS 60-63 EQUALS 1	3	49	1
1J097	45.01.01.1	RESIDUE OF AB REGISTER POS 64-107 EQUALS 2	3	49	2
1J098	45.01.01.1	RESIDUE OF AB REGISTER POS 64-107 EQUALS 1	3	49	3
1J101	59.06.03.1	AB RESIDUE REGISTER POS 2	3	49	4
1J102	59.06.03.1	AB RESIDUE REGISTER POS 1	3	49	5
1J103	59.06.03.1	AB RESIDUE REGISTER POS 0	3	49	6
1K016	38.22.16.1	NEXT SEL (Last PRG)	2	60	1

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATOR	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
1K017	38.22.16.1	E BOX NEXT STORE 1	3	69	00
1K018	38.22.16.1	E BOX NEXT STORE 2	3	69	08
1K019	38.22.16.1	I BOX NEXT STORE 1	3	39	7
1K020	38.22.16.1	I BOX NEXT STORE 2	3	39	9
1K021	59.91.02.1	E BOX STORE	3	40	12
1K022	59.91.01.1	STORE REG NOT BUSY	3	64	3
1K023	59.91.01.1	STORE TIME 1	3	64	7
1K024	59.91.01.1	STORE REGISTER MEMORY REQUEST	3	64	8
1K025	59.91.02.1	WORD BOUNDARY CROSSOVER STORE	3	64	9
1K026	59.91.02.1	I BOX STORE	3	65	12
1K027	59.91.03.1	STORE C REG EXTERNAL	3	65	11
1K028	59.91.03.1	STORE D REG EXTERNAL	3	65	00
1K029	59.91.03.1	STORE C TIME TGR	3	65	1
1K030	59.91.02.1	ZERO DIVISOR	3	65	2
1K033	59.90.01.1	STORE REGISTER POSITIONS	4	41	12-9
THROUGH	THROUGH	0-55	4	42	12-9
1K088	59.90.14.1		4	43	12-9
			4	44	12-9
			4	45	12-5
1K089	59.90.15.1	STORE REGISTER POSITIONS 56-63	4	51	12-5
THROUGH	THROUGH				
1K096	59.90.16.1				
1K097	59.90.17.1	STORE REGISTER ECC BITS C0, C1, C2, C4, C8, C16,	4	51	6-9
THROUGH	THROUGH	C32, AND CT	4	52	12-1
1K104	59.90.18.1				
1L001	65.04.62.1	.75 TRUE DIVISOR MULTIPLE	3	66	8
1L002	65.04.62.1	.75 COMPLEMENT DIVISOR MULTIPLE	3	66	9
1L003	65.04.63.1	1.5 TRUE DIVISOR MULTIPLE	3	67	12
1L004	65.04.63.1	1.5 COMPLEMENT DIVISOR MULTIPLE	3	67	11
1L005	65.04.92.1	1 TIMES TRUE DIVISOR MULTIPLE	3	67	0
1L006	65.04.92.1	1 TIMES COMPLEMENT DIVISOR MULTIPLE	3	67	1
1L007	61.03.63.1	DIVIDE NORM-EXPONENT	3	67	2
1L008	61.03.64.1	DIVISOR STATUS TRIGGER	3	67	3
1L009	61.03.65.1	DIVIDEND STATUS TRIGGER	3	67	4
1L010	61.03.66.1	DIVIDE STATUS TRIGGER	3	67	5
1L011	61.03.67.1	ONE TIMES COMPLEMENT STATUS	3	67	6
1L012	61.03.69.1	SECOND DIVIDE CYCLE	3	67	7
1L013	61.03.70.1	DIVIDE COUNTER	3	67	8
1L014	61.03.71.1	FINAL DIVIDE	3	67	9
1L015	61.03.72.1	ZERO DIVIDEND	3	68	12
1L016	61.03.73.1	INTERCHANGE DIVIDE	3	68	11
1L017	61.03.75.1	DIVIDE RING D3CA	3	68	0
1L018	61.03.76.1	DIVIDE RING D3CB	3	68	1
1L019	61.03.77.1	DIVIDE RING D4	3	68	2
1L020	61.03.45.1	MULTIPLY RING MC	3	68	3
1L021	61.03.51.1	MULTIPLY RING 1	3	68	4
1L022	61.03.52.1	MULTIPLY RING 2	3	68	5
1L023	61.03.53.1	MULTIPLY RING 3	3	68	6
1L024	61.03.54.1	MULTIPLY STATUS	3	68	7
1L025	61.03.56.1	ONE TIMES MULTIPLICAND	3	68	8
1L026	61.03.55.1	SHIFT RIGHT 12	3	68	9
1L027	61.03.57.1	GATE S AND T REGISTER TO PAU ADDER	3	69	12
1L028	61.03.58.1	CUMULATIVE MULTIPLY	3	69	11
1L030	61.03.60.1	CUMULATIVE MULTIPLY PRESHIFT EXPONENT	3	69	1
1L031	61.81.66.1	GATE 61-63 TRIGGER	3	69	2
1L032	61.80.56.1	HIGH ORDER SHIFTER TRUE TO ADDRESS 0-49	3	69	3
1L033	61.80.57.1	LOW ORDER SHIFTER TRUE TO ADDRESS 50-97	3	69	4
1L034	61.80.58.1	COMPLEMENT SHIFTER TO ADDER	3	69	5
1L035	62.29.05.1	F REGISTER FRACTION IS ZERO	3	69	6
1L036	61.02.60.1	PRESHIFT & ADD	3	69	7
1L038	61.02.76.1	EXPONENT ROUTING CONTROL	3	69	9
1L039	61.02.78.1	EXPONENT SAMPLE	3	70	12
1L040	61.02.63.1	NORM EXPONENT	3	70	11
1L041	61.02.64.1	NORM MANTISSA	3	70	0
1L042	61.02.67.1	PERFORM AUGMENT	3	70	1
1L045	65.04.91.1	INCREMENTS EXPONENTS C, 4, 2, AND 1	3	9	4-7
THROUGH					
1L048					
1L051	65.03.30.1	SHIFT COUNTER POS S, 64, 32, 16, 8, 4, 2, AND 1		19	6-9
THROUGH	65.03.17.1			20	12-1
1L058	65.03.16.1				
1L061	65.05.01.1	LEFT SHIFT 6, 5, 4, 3, 2, AND 1 INDICATORS		26	11-4
THROUGH	THROUGH				
1L066	65.05.06.1				
1L067	65.05.07.1	ZERO SHIFT INDICATOR		26	5
1L068	65.05.08.1	RIGHT SHIFT 1, 2, 3, 4, AND 8 INDICATORS		26	6-9
THROUGH	AND				
1L072	65.05.12.1			27	12
1L075	61.01.07.1	EXECUTE REGISTER POS 18	3	27	11
1L076	61.01.08.1	EXECUTE REGISTER POS 19	3	27	0

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
1L077	61.01.08.1	EXECUTE REGISTER POS 20	3	27	1
1L078	61.01.08.1	EXECUTE REGISTER POS 21-25	3	27	2-6
THROUGH	THROUGH				
1L082	61.01.10.1				
1L085	66.30.17.1	COMPLEMENT GROUP 4	3	27	7
1L086	66.20.01.1	8, 6, 4, OR 2 TIMES MPCND - GROUP 4	3	27	8-9
THROUGH			3	28	12-11
1L089					
1L090	66.30.19.1	COMPLEMENT GROUP 3	3	28	0
1L091	66.20.02.1	8, 6, 4, OR 2 TIMES MPCND - GROUP 3	3	28	1-4
THROUGH					
1L094					
1L095	66.30.21.1	COMPLEMENT GROUP 2	3	28	5
1L096	66.20.03.1	8, 6, 4, OR 2 TIMES MPCND - GROUP 2	3	28	6-9
THROUGH					
1L099					
1L100	66.30.23.1	COMPLEMENT GROUP 1	3	29	12
1L101	66.20.04.1	8, 6, 4, OR 2 TIMES MPCND - GROUP 1	3	29	11-2
THROUGH					
1L104					
1M001	61.02.93.1	WRITE EXPONENT INTO A	3	9	8
1M002	61.02.93.1	WRITE EXPONENT INTO B	3	9	9
1M003	61.02.94.1	WRITE EXPONENT INTO C	3	10	12
1M004	61.02.95.1	WRITE EXPONENT INTO D	3	10	11
1M005	61.02.36.1	PROPAGATE FLAG	3	10	0
1M006	61.02.65.1	TX	3	10	1
1M007	61.02.66.1	SSQ SIGNAL TO VFL	3	29	3
1M008	61.03.80.1	VFL DIVISOR	3	29	4
1M009	61.02.71.1	NOT PHASE SAMPLE TEST COMPLETE	3	29	5
1M010	61.02.73.1	INTERRUPT	3	29	6
1M011	61.02.68.1	OVERFLOW	3	29	7
1M012	61.02.68.1	COMPLEMENT RESULT	3	29	8
1M013	61.02.82.1	BIT ADDRESS CD 64 IS ON	3	29	9
1M014	61.02.77.1	SHIFT EQUAL OR GREATER THAN 96	3	30	12
1M015	61.02.77.1	SHIFT GREATER THAN 48	3	30	11
1M016	61.01.55.1	EXPONENT PARITY	3	30	0
1M017	61.01.79.1	AUGMENT ON PARTIAL FIELD	3	30	1
1M018	61.02.69.1	BUFFER SIGN	3	39	0
1M019	61.03.02.1	SHIFT REMEMBERED A	3	39	1
1M020	61.03.02.1	SHIFT REMEMBERED B	3	39	2
1M021	65.04.95.1	QUOTIENT CONTROL	3	39	3
1M022	61.04.20.1	TEST COMPLETE-EXECUTE TEST	3	39	4
1M023	61.04.20.1	TEST COMPLETE-LOOK AHEAD TEST	3	39	5
1M024	61.04.20.1	TEST COMPLETE-BUS TEST	3	39	6
1M026	61.04.21.1	MASTER TEST COMPLETE	3	39	8
1M029	61.01.55.1	FP EXTERNAL STORE	3	40	11
1M030	61.01.50.1	FIRST CYCLE TRIGGER	3	40	0
1M031	61.01.56.1	FLOATING POINT WAIT	3	40	1
1M032	61.01.57.1	INTERRUPT END OPERATION	3	65	9
1M033	61.02.99.1	END OPERATION	3	66	12
1M034	61.01.78.1	INDICATOR LATCH	3	66	11
1M035	61.01.78.1	INDICATOR EXPONENT LATCH	3	66	0
1M036	61.02.50.1	T0,T1,T2,T3,T4,TB, AND TC RING TRIGGERS	3	66	1-7
THROUGH	THROUGH				
1M042	61.02.57.1				
1M044	68.10.03.1	CARRY REGISTER POS 01-61	3	31	12-9
THROUGH	THROUGH		3	32	12-9
1M104	68.10.61.1		3	33	12-9
			3	34	12-9
			3	35	12-9
			3	36	12

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATOR	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
1N044	68.10.01.1	SUM REGISTER POS 01-61	3	21	12-9
			3	22	12-9
THROUGH	THROUGH		3	23	12-9
1N104	68.10.61.1		3	24	12-9
			3	25	12-9
			3	26	12
1P001	64.51.05.1	ADDER OUTPUT POS P	3	11	12
1P002	61.02.68.1	ADDER OUTPUT POSITION 00	3	11	11
1P003	64.56.03.1	ADDER OUTPUT POSITION 01	3	11	0
1P004	64.56.03.1	ADDER OUTPUT POSITION 02	3	11	1
1P005	65.04.25.1	ADDER OUTPUT POS 03-06	3	11	2-5
THROUGH	65.04.24.1		3		
1P008	65.04.23.1		3		
1P009	64.56.02.1	ADDER OUTPUT POS 07-18	3	11	6-9
THROUGH	AND		3	12	12-5
1P020	64.56.01.1		3		
1P021	64.46.03.1	ADDER OUTPUT POS 19-38	3	12	6-9
THROUGH	64.46.02.1		3	13	12-9
1P040	64.46.01.1		3	14	12-1
1P041	64.36.04.1	ADDER OUTPUT POS 39-58	3	14	2-9
THROUGH	THROUGH		3	15	12-9
1P060	64.36.01.1		3		
1P061	64.26.04.1	ADDER OUTPUT POS 59-78	3	16	12-5
THROUGH	THROUGH		3	17	12-5
1P080	64.26.01.1		3		
1P081	64.16.05.1	ADDER OUTPUT POS 79-98	3	17	6-9
THROUGH	THROUGH		3	18	12-9
1P100	64.16.01.1		3	19	12-1
1P101	64.66.01.1	ADDER OUTPUT POS 99-102	3	19	2-5
THROUGH			3		
1P104			3		
1Q002	62.20.01.1	F REGISTER POS 00-101	3	1	12-9
THROUGH	THROUGH		3	2	12-9
1Q103	62.20.99.1		3	3	12-9
			3	4	12-9
			3	5	12-9
			3	6	12-9
			3	7	12-9
			3	8	12-9
			3	9	12-3
2A005	11.03.02.1	INITIAL RESET TGR	4	45	11
2A008	11.04.01.1	1 CLOCK PULSE	4	45	2
2A009	11.04.01.1	2 CLOCK PULSES	4	45	3
2A010	11.04.01.1	3 CLOCK PULSES	4	45	4
2A011	11.04.01.1	START SYNC A TGR	4	45	5
2A012	11.04.01.1	START SYNC B TGR	4	64	4
2A013	11.04.02.1	STOP SYNC A TGR	4	64	5
2A014	11.04.02.1	STOP SYNC B TGR	4	64	6
2A016	11.04.02.1	AXXB MODE CLOCK CONTROLS	4	64	8
2A017	11.03.01.1	ALLOW MEM BUS CLOCK CTL TGR	4	64	9
2A018	11.03.01.1	INHIBIT DELAYED A-B CLOCK CTL TGR	4	65	12
2A019	11.03.01.1	INHIBIT ABAB CLOCK CTL TGR	4	65	11
2A020	11.03.01.1	B NEXT CLOCK CTL TGR	4	65	0
2A029	23.11.01.1	X REGISTER POS 00-17	1	1	12-9
THROUGH	THROUGH		1	2	12-3
2A046	23.11.09.1				
2A047	23.11.10.1	X REGISTER PARITY 00-17	1	6	2
2A048	23.11.10.1	X REGISTER POS 18-23	1	2	4-9
THROUGH	THROUGH				
2A053	23.11.13.1				

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATOR	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
2A054	23.11.13.1	X REGISTER PARITY 18-23	1	6	3
2A055	23.11.14.1	X REGISTER POS 24-27	1	3	12-1
THROUGH	AND				
2A058	23.11.15.1				
2A059	23.11.16.1	X REGISTER PARITY 24-27	1	6	4
2A060	23.11.17.1	X REGISTER POS 28-31	1	3	2-5
THROUGH	AND				
2A063	23.11.18.1				
2A064	23.11.18.1	X REGISTER PARITY 28-31	1	6	5
2A065	23.11.01.1	X REGISTER POS 32-49	1	3	6-9
THROUGH	THROUGH		1	4	12-9
2A082	23.11.09.1		1	5	12-11
2A083	23.11.10.1	X REGISTER PARITY 32-49	1	6	6
2A084	23.11.19.1	X REGISTER PARITY 46-49	1	6	7
2A085	23.11.10.1	X REGISTER POS 50-55	1	5	0-5
THROUGH	THROUGH				
2A090	23.11.13.1				
2A091	23.11.13.1	X REGISTER PARITY 50-55	1	6	8
2A092	23.11.14.1	X REGISTER POS 56-59	1	5	6-9
THROUGH	AND				
2A095	23.11.15.1				
2A096	23.11.16.1	X REGISTER PARITY 56-59	1	6	9
2A097	23.11.16.1	X REGISTER POS 60-63	1	6	12-1
THROUGH	THROUGH				
2A100	23.11.18.1				
2A101	23.11.18.1	X REGISTER PARITY 60-63	1	7	12
2B001	13.05.01.1	MEMORY A 0 BUSY TGR	4	42	5
2B002	13.05.02.1	MEMORY A 1 BUSY TGR	4	42	6
2B005	13.05.01.1	MEMORY B 0 BUSY TGR	4	42	9
2B006	13.05.01.1	MEMORY B 1 BUSY TGR	4	43	12
2B007	13.05.02.1	MEMORY B 2 BUSY TGR	4	43	11
2B008	13.05.02.1	MEMORY B 3 BUSY TGR	4	43	0
2B028	25.01.01.1	Z REGISTER POS 00-17	1	31	12-9
THROUGH	THROUGH		1	32	12-3
2B045	25.01.05.1				
2B046	25.01.05.1	Z REGISTER PARITY 00-17	1	36	2
2B047	25.01.05.1	Z REGISTER POS 18	1	32	4
2B048	25.01.04.1	Z REGISTER PARITY 12-18	1	36	3
2B049	25.01.05.1	Z REGISTER POS 19-23		32	5-9
THROUGH	AND				
2B053	25.01.06.1				
2B054	25.01.07.1	Z REGISTER PARITY 19-23	1	36	4
2B055	25.01.07.1	Z REGISTER POS 24-27	1	33	12-1
THROUGH					
2B058					
2B059	25.01.09.1	Z REGISTER PARITY 24-27	1	36	5
2B060	25.01.07.1	Z REGISTER POS 28-31	1	33	2-5
THROUGH	AND				
2B063	25.01.08.1				
2B064	25.01.08.1	Z REGISTER PARITY 28-31	1	36	6
2B065	25.01.08.1	Z REGISTER POS 32-40	1	33	6-9
THROUGH	THROUGH		1	34	12-2
2B073	25.01.10.1				
2B074	25.01.10.1	Z REGISTER PARITY 35-40	1	36	7
2B075	25.01.11.1	Z REGISTER POS 41-49	1	34	3-9
THROUGH	AND		1	35	12-11
2B083	25.01.12.1				
2B084	25.01.12.1	Z REGISTER PARITY 32-49	1	36	8
2B085	25.01.13.1	Z REGISTER POS 50-55	1	35	0-5
THROUGH	AND				
2B090	25.01.14.1				

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
2B091	25.01.14.1	Z REGISTER PARITY 50-55	1	36	9
2B092	25.01.14.1	Z REGISTER POS 56-59	1	35	6-9
THROUGH	AND				
2B095	25.01.15.1				
2B096	25.01.15.1	Z REGISTER PARITY 56-59	1	37	12
2B097	25.01.15.1	Z REGISTER POS 60-63	1	36	12-1
THROUGH					
2B100					
2B101	25.01.15.1	Z REGISTER PARITY 60-63	1	37	11
2B102	25.01.16.1	PROGRESSIVE INDEXING REGISTER POS 00-02	1	37	0-2
THROUGH					
2B104					
2C001	12.09.01.1	BX MEMORY REQUEST TGR	1	59	9
2C002	12.09.01.1	HX MEMORY REQUEST TGR	1	60	12
2C003	12.09.01.1	LA STORE MEMORY REQUEST TGR	1	60	11
2C004	12.09.01.1	I FETCH MEMORY REQUEST TGR	1	60	0
2C009	16.04.01.1	BOUNDARY REGISTER COMPARE ERR	4	55	4
2C011	17.08.01.1	RETURN ADDRESS PARITY ERR	1	62	0
2C014	14.02.01.1	BX STORE ADDRESS ERR	1	54	7
2C015	14.02.01.1	HX STORE ADDRESS ERR	1	54	8
2C016	14.02.01.1	LA STORE ADDRESS ERR	1	54	9
2C018	15.01.03.1	GATE 1 TGR	1	55	12
2C019	15.01.03.1	GATE NEXT TGR	1	55	11
2C020	15.01.03.1	GATE 2 TGR	1	55	0
2C021	15.01.03.1	STAR BUSY TGR	1	55	1
2C028	21.05.01.1	INSTRUCTION COUNTER ADDER OUTPUT POS 00-16	1	42	7-9
THROUGH	AND		1	43	12-9
2C044	21.05.02.1		1	44	12-11
2C045	21.04.08.1	INSTR COUNTER ADDER OUTPUT PARITY 00-16	1	44	0
2C053	31.01.58.1	U/L BOUNDARY REGISTER CONTROL BIT 57	4	62	7
2C054	31.01.59.1	U/L BOUNDARY REGISTER ERROR INJECT BIT 58	4	62	8
2C055	31.02.09.1	U/L BOUNDARY REGISTER PARITY ON BIT 57	4	62	9
2C057	31.01.33.1	LOWER BOUNDARY REGISTER POS 32-39	4	61	12-6
THROUGH	THROUGH				
2C064	31.01.40.1				
2C065	31.03.06.1	LOWER BOUNDARY REGISTER PARITY 32-39	4	62	4
2C066	31.01.41.1	LOWER BOUNDARY REGISTER POS 40-47	4	61	6-9
THROUGH	THROUGH		4	62	12-1
2C073	31.01.48.1		4	62	5
2C074	31.02.07.1	LOWER BOUNDARY REGISTER PARITY 40-47	4	62	2
2C075	31.01.49.1	LOWER BOUNDARY REGISTER POS 48	4	62	3
2C076	31.01.50.1	LOWER BOUNDARY REGISTER POS 49	4	62	6
2C077	31.02.08.1	LOWER BOUNDARY REGISTER PARITY 48-49	1	44	1-9
2C085	26.01.01.1	W REGISTER POS 00-17			
THROUGH	THROUGH		1	45	12-6
2C102	26.01.05.1		1	45	7
2C103	26.01.05.1	W REGISTER PARITY 00-17	4	53	9
2D001	15.02.01.1	LOOKAHEAD ADDRESS REGISTER 2	4	54	12-9
THROUGH	THROUGH	POSITIONS 0-18	4	55	12-3
2D019	15.02.05.1		1	41	12-9
2D028	21.01.01.1	INSTRUCTION COUNTER REGISTER POS 00-16			
THROUGH	THROUGH		1	42	12-
2D044	21.01.05.1		1	42	5
2D045	21.01.05.1	INSTRUCTION COUNTER REGISTER PARITY 00-16	1	42	3
2D046	21.01.06.1	INSTRUCTION COUNTER REGISTER POS 17	1	42	4
2D047	21.01.06.1	INSTRUCTION COUNTER REGISTER POS 18	1	42	6
2D048	21.01.06.1	INSTRUCTION COUNTER REGISTER PARITY 17-18	4	34	1
2D054	37.52.15.1	UNIT ADDRESS REGISTER PARITY 12-15	4	34	2
2D055	37.52.23.1	UNIT ADDRESS REGISTER PARITY 16-23	4	63	12-5
2D057	31.01.01.1	UPPER BOUNDARY REGISTER POS 00-07			
THROUGH	THROUGH				
2D064	31.01.08.1		4	64	4
2D065	31.02.01.1	UPPER BOUNDARY REGISTER PARITY 00-07	4	63	6-9
2D066	31.01.09.1	UPPER BOUNDARY REGISTER POS 08-11			
THROUGH	THROUGH				
2D069	31.01.12.1	Serial Numbers 30,003 – 30,005			

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
2D070	31.02.02.1	UPPER BOUNDARY REGISTER PARITY 08-11	4	64	5
2D071	31.01.13.1	UPPER BOUNDARY REGISTER POS 12-15	4	64	12-1
THROUGH	THROUGH				
2D074	31.01.16.1				
2D075	31.02.03.1	UPPER BOUNDARY REGISTER PARITY 12-15	4	64	6
2D076	31.01.17.1	UPPER BOUNDARY REGISTER POS 16	4	64	2
2D077	31.01.18.1	UPPER BOUNDARY REGISTER POS 17	4	64	3
2D078	31.02.04.1	UPPER BOUNDARY REGISTER PARITY 16-17	4	64	7
2D085	27.11.07.1	INDEX ADDER BLOCK 6 ERROR POS 03-00, EAC, 23	1	45	8
2D086	27.11.07.1	INDEX ADDER BLOCK 5 ERROR POS 07-03	1	45	9
2D087	27.11.07.1	INDEX ADDER BLOCK 4 ERROR POS 11-07	1	46	12
2D088	27.11.07.1	INDEX ADDER BLOCK 3 ERROR POS 15-11	1	46	11
2D089	27.11.07.1	INDEX ADDER BLOCK 2 ERROR POS 15-19	1	46	0
2D090	27.11.07.1	INDEX ADDER BLOCK 1 ERROR POS 19-23	1	46	1
2D091	27.11.07.1	INSTRUCTION COUNTER ADDER ERROR	1	46	2
2D092	27.04.03.1	INDEX ADDER BYPASS ERROR	1	46	3
2D093	21.04.07.1	INSTRUCTION COUNTER SUM OR GATING ERROR	1	46	4
2D094	21.04.07.1	INSTRUCTION COUNTER 0-16 CARRY ERROR	1	46	5
2D095	21.04.07.1	INSTRUCTION COUNTER 17-18 ERROR	1	46	6
2D097	24.00.03.1	INDEX ADDRESS CHECK	1	46	8
2D100	26.04.05.1	LOAD GEOMETRIC ADDRESS REGISTER POS 00-03	1	46	9
THROUGH				47	12-0
2D103					
2D104	26.04.05.1	LOAD GEOMETRIC ADDRESS REGISTER PARITY 00-03	1	47	1
2E001	15.02.01.1	LOOKAHEAD ADDRESS REGISTER 1	4	52	2-9
THROUGH	THROUGH	POSITIONS 0-18	4	53	12-8
2D019	15.02.05.1				
2E049	37.52.12.1	UNIT ADDRESS REGISTER POS 12-18	4	33	6-9
THROUGH	THROUGH				
2E055	37.52.18.1		4	34	12-0
2F001	34.03.51.1	GENERATED PARITY (NOT INPUT PARITY) POS 00-07,	1	65	9
THROUGH		08-11, 12-15, 16-23, 24-31, 32-39, 40-47, 48-55, 56-59,	1	66	12-6
2F010	34.03.52.1	AND 60-63.	1	66	7-9
2F011	34.03.52.1	GENERATED PARITY (NOT INPUT PARITY) POS 00-17,	1	67	12-0
THROUGH		18-23, 24-27, 28-31, 32-49, AND 50-55.			
2F016					
2F018	34.03.41.1	GENERATED ECC (NOT INPUT ECC) POS C0, C1, C2, C4,	4	15	12-5
THROUGH	THROUGH	C8, C16, C32 AND CT			
2F025	34.03.44.1				
2F028	15.02.01.1	STORAGE ADDRESS REGISTER	1	68	7-9
THROUGH	THROUGH	POSITIONS 0-18	1	69	12-9
2F046	15.02.05.1		1	70	12-1
2F049	37.22.20.1	MASK REGISTER PARITY 20-23	4	33	2
2F050	37.22.24.1	MASK REGISTER PARITY 24-31	4	33	2
2F051	37.22.32.1	MASK REGISTER PARITY 32-39	4	33	4
2F052	37.22.40.1	MASK REGISTER PARITY 40-47	4	33	5
2F053	37.22.20.1	MASK REGISTER POS 20-47	4	31	12-9
THROUGH	37.22.24.1		4	32	12-9
2F080	37.22.32.1		4	33	12-1
	37.22.40.1				
2F083	32.01.01.1	INSTRUCTION COUNTER BUFFER POS 00-16	2	68	5-9
THROUGH	THROUGH			69	12-9
2F099	32.01.17.1				
2F100	32.01.20.1	INSTRUCTION COUNTER BUFF PARITY POS 00-16	2	70	0

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATOR	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
2F101	32.01.18.1	INSTRUCTION COUNTER BUFFER POS 17	2	70	12
2F102	32.01.19.1	INSTRUCTION COUNTER BUFFER POS 18	2	70	11
2F103	32.01.21.1	INSTRUCTION COUNTER BUFF PARITY POS 17-18	2	70	1
2G001	34.01.51.1	I CHECKER IN-BUS POS 64-73	4	24	6-9
THROUGH	THROUGH			25	12-3
2G010	34.01.53.1				
2G012	34.07.53.1	I CHECKER GENERATED RESIDUE EQUALS 2	4	25	4
2G013	34.07.53.1	I CHECKER GENERATED RESIDUE EQUALS 1	4	25	5
2G015	34.08.51.1	I CHECKER PERMANENT ECC ERROR TRIGGER	4	34	6
2G016	34.08.51.1	I CHECKER TEMPORARY ECC ERROR TRIGGER	4	34	7
2G017	34.08.51.1	I CHECKER PERMANENT LA PARITY ERROR TRIGGER	4	34	8
2G018	34.08.51.1	I CHECKER PERMANENT I PARITY ERROR TRIGGER	4	34	9
2G019	34.08.51.1	I CHECKER UNCORRECTABLE ECC ERROR TRIGGER	4	35	12
2G021	34.08.21.1	I CHECKER CHECK ECC TRIGGER	4	35	11
2G022	34.08.21.1	I CHECKER CHECK LA PARITY TRIGGER	4	35	0
2G023	34.08.21.1	I CHECKER CHECK I PARITY TRIGGER	4	35	1
2G024	34.08.31.1	I CHECKER GENERATE PARITY TRIGGER	4	35	2
2G033	37.12.00.1	IND REG POS 00-MK MACHINE CHECK	4	13	2
2G034	37.12.00.1	IND REG POS 01-IK INSTRUCTION CHECK	4	13	3
2G035	37.12.02.1	IND REG POS 02-IJ INSTRUCTION REJECT	4	13	4
2G036	37.12.02.1	IND REG POS 03-EK EXCHANGE CNTRL CHK	4	13	5
2G037	37.12.04.1	IND REG POS 04-TS TIME SIGNAL	4	13	6
2G038	37.12.04.1	IND REG POS 05-CPUS CPU SIGNAL	4	13	7
2G039	37.12.06.1	IND REG POS 06-EKJ EXCHANGE CHECK REJECT	4	13	8
2G040	37.12.06.1	IND REG POS 07-UNRJ UNIT NOT READY REJECT	4	13	9
2G041	37.12.08.1	IND REG POS 08-CBJ CHANNEL BUSY REJECT	4	14	12
2G042	37.12.08.1	IND REG POS 09-EPGK EXCHANGE PROGRAM CHECK	4	14	11
2G043	37.12.10.1	IND REG POS 10-UK UNIT CHECK	4	14	0
2G044	37.12.10.1	IND REG POS 11-EE END EXCEPTION	4	14	1
2G045	37.12.12.1	IND REG POS 12-EOP END OF OPERATION	4	14	2
2G046	37.12.12.1	IND REG POS 13-CS CHANNEL SIGNAL	4	14	3
2G047	37.12.14.1	IND REG POS 14 RESERVED	4	14	4
2G048	37.12.15.1	IND REG POS 15-OP OPERATION CODE INVALID	4	14	5
2G049	37.12.15.1	IND REG POS 16-AD ADDRESS INVALID	4	14	6
2G050	37.12.17.1	IND REG POS 17-USA UNENDED SEQ OF ADDRESSES	4	14	7
2G051	37.12.17.1	IND REG POS 18-EXE EXECUTE EXCEPTION	4	14	8
2G052	37.12.19.1	IND REG POS 19-DS DATA STORE	4	14	9
2G053	37.12.19.1	IND REG POS 20-DF DATA FETCH	4	21	12
2G054	37.12.21.1	IND REG POS 21-IF INSTRUCTION FETCH	4	21	11
2G055	37.12.21.1	IND REG POS 22-LC LOST CARRY	4	21	0
2G056	37.12.23.1	IND REG POS 23-PF PARTIAL FIELD	4	21	1
2G057	37.12.23.1	IND REG POS 24-ZD ZERO DIVISOR	4	21	2
2G058	37.12.25.1	IND REG POS 25-IR IMAGINARY ROOT	4	21	3
2G059	37.12.25.1	IND REG POS 26-LS LOST SIGNIFICANCE	4	21	4
2G060	37.12.27.1	IND REG POS 27-PSH PREP SHIFT MORE THAN 48	4	21	5
2G061	37.12.27.1	EXPONENT FLAG	4	21	6
2G062	37.12.27.1	EXPONENT OVERFLOW	4	21	7
2G063	37.12.30.1	EXPONENT HIGH	4	21	8
2G064	37.12.30.1	EXPONENT LOW	4	21	9
2G065	37.12.30.1	EXPONENT UNDERFLOW	4	22	12
2G066	37.12.30.1	ZERO MULTIPLY	4	22	11
2G067	37.12.34.1	IND REG POS 34-RU REMAINDER UNDERFLOW	4	22	0
2G068	37.12.34.1	IND REG POS 35-TF DATA FLAG T	4	22	1
2G069	37.12.36.1	IND REG POS 36-UF DATA FLAG U	4	22	2
2G070	37.12.36.1	IND REG POS 37-VF DATA FLAG V	4	22	3
2G071	37.12.38.1	IND REG POS 38-XF INDEX FLAG	4	22	4
2G072	37.12.38.1	IND REG POS 39-BTR BINARY TRANSIT	4	22	5
2G073	37.12.40.1	IND REG POS 40-DTR DECIMAL TRANSIT	4	22	6
2G074	37.12.40.1	IND REG POS 41-PG0 PROGRAM INDICATOR 0	4	22	7
2G075	37.12.40.1	IND REG POS 42-PG1 PROGRAM INDICATOR 1	4	22	8

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
2G076	37.12.40.1	IND REG POS 43-PG2 PROGRAM INDICATOR 2	4	22	9
2G077	37.12.44.1	IND REG POS 44-PG3 PROGRAM INDICATOR 3	4	23	12
2G078	37.12.44.1	IND REG POS 45-PG4 PROGRAM INDICATOR 4	4	23	11
2G079	37.12.44.1	IND REG POS 46-PG5 PROGRAM INDICATOR 5	4	23	0
2G080	37.12.44.1	IND REG POS 47-PG6 PROGRAM INDICATOR 6	4	23	1
2G081	37.12.48.1	IND REG POS 48-XCZ INDEX COUNT ZERO	4	23	2
2G082	37.12.48.1	IND REG POS 49-XVLZ INDEX VALUE LESS THAN 0	4	23	3
2G083	37.12.48.1	IND REG POS 50-XVZ INDEX VALUE ZERO	4	23	4
2G084	37.12.51.1	IND REG POS 51-XVGZ INDEX VALUE MORE THAN 0	4	23	5
2G085	37.12.51.1	IND REG POS 52-XL INDEX LOW	4	23	6
2G086	37.12.53.1	IND REG POS 53-XE INDEX EQUAL	4	23	7
2G087	37.12.53.1	IND REG POS 54-XH INDEX HIGH	4	23	8
2G088	37.12.55.1	IND REG POS 55-MOP TO MEMORY OPERATION	4	23	9
2G089	37.12.55.1	IND REG POS 56-RLZ RESULT LESS THAN ZERO	4	24	12
2G090	37.12.57.1	IND REG POS 57-RZ RESULT ZERO	4	24	11
2G091	37.12.57.1	IND REG POS 58-RGZ RESULT MORE THAN ZERO	4	24	0
2G092	37.12.59.1	IND REG POS 59-RN RESULT NEGATIVE	4	24	1
2G093	37.12.59.1	IND REG POS 60-AL ACCUMULATOR LOW	4	24	2
2G094	37.12.61.1	IND REG POS 61-AE ACCUMULATOR EQUAL	4	24	3
2G095	37.12.62.1	IND REG POS 62-AH ACCUMULATOR HIGH	4	24	4
2G096	37.12.62.1	IND REG POS 63-NM NOISY MODE	4	24	5
2H029	31.01.01.1	LA LEVEL 4 OPERAND FIELD POS 00-75	2	31	12-9
THROUGH	THROUGH		2	32	12-9
2H104	31.01.64.1		2	33	12-9
	31.02.01.1		2	34	12-9
	THROUGH		2	35	12-9
	31.02.10.1		2	36	12-9
	31.29.01.1		2	37	12-1
	AND				
	31.29.02.1				
2J009	38.23.05.1	SAU START TRIGGER	1	67	1
2J010	38.23.04.1	SAU GO TRIGGER	1	67	2
2J011	38.23.04.1	SAU INSTRUCTION REJECT TRIGGER	1	67	3
2J012	38.34.02.1	SAU ENABLED MEMORY TRIGGER	1	67	4
2J013	38.35.06.1	EXECUTION UNIT IND TEST E TGR TO PAU	1	67	5
2J014	38.39.05.1	INSTRUCTION UNIT HOUSECLEAN REQUEST TRIGGER	1	67	6
2J017	38.24.01.1	EXECUTION UNIT FIRST CYCLE MEMORY TRIGGER	1	67	9
2J018	38.24.03.1	SAU WAIT FOR MCND TGR SAU MPYC	1	68	12
2J019	38.24.02.1	EXECUTION UNIT LAST CYCLE STORE TRIGGER	1	68	11
2J021	38.39.04.1	EXECUTION UNITS IDLE TRIGGER	1	68	1
2J022	38.24.03.1	BR TEST RESULT IX TGR - BR UNSUCC - NOPD	1	68	2
2J023	38.24.03.1	BR TEST RESULT X1 TGR - BR SUCC	1	68	3
2J024	38.25.03.1	EXCHANGE UNIT REACTION STORAGE TRIGGER	1	68	4
2J025	38.25.03.1	EXCHANGE RESPONSE BUFFER TRIGGER	1	68	5
2J026	38.25.03.1	EXCHANGE RESPONSE TRIGGER	1	68	6
2J032	38.01.05.1	IAUC COUNTER POS 4 TRIGGER	2	38	11
2J033	38.11.05.1	OCC COUNTER POS 4 TRIGGER	2	38	0
2J034	38.21.02.1	TBC COUNTER POS 4 TRIGGER	2	38	1
2J035	38.31.02.1	ABC COUNTER POS 4 TRIGGER	2	38	2
2J036	38.51.02.1	SCC COUNTER POS 4 TRIGGER	2	38	3
2J037	36.16.02.1	FROM BIT 1 - LEVEL 4	2	38	4
2J038	36.13.03.1	FROM BIT 2 - LEVEL 4	4	34	6
2J040	36.09.03.1	LA LEVEL 4 OP CODE FIELD POS 00-09	2	43	7-9
THROUGH	THROUGH		2	44	12-5
2J049	36.09.12.1				

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
2J050	36.09.13.1	PAR ON OP CODE POS 1-4 FOR PS J ADDR ONLY	2	44	5
2J053	36.08.02.1	DISCONNECT TAG BIT LEVEL 4	2	37	3
2J054	36.07.06.1	NOOP TAG BIT LEVEL 4	2	37	4
2J055	36.06.01.1	WORD BOUNDARY CROSSOVER TAG BIT LEVEL 4	2	37	5
2J056	36.05.01.1	LOOKAHEAD OPERATION CODE TAG BIT LEVEL 4	2	37	6
2J057	36.04.01.1	INSTRUCTION COUNTER VALID TAB BIT LEVEL 4	2	37	7
2J058	36.03.02.1	INTERNAL FETCH TAG BIT LEVEL 4	2	37	8
2J059	36.02.03.1	LEVEL CHECKED TAG BIT LEVEL 4	2	37	9
2J060	36.01.04.1	LEVEL FILLED M TAG BIT LEVEL 4	2	38	12
2J061	36.09.19.1	INDEX STORE TAG - LEVEL 4	2	37	2
2J062	36.09.14.1	EXTERNAL STORE TAG - LEVEL 4	4	4	1
2J063	36.09.15.1	INTERNAL STORE TAG - LEVEL 4	4	4	5
2J066	33.01.01.1	LA LEVEL 4 CONDITIONAL MACH CHK INDICATOR	2	48	3
2J067	33.01.19.1	LA LEVEL 4 INSTRUCTION REJECT INDICATOR	2	48	4
2J068	33.01.04.1	LA LEVEL 4 OPERATION CODE INVALID INDICATOR	2	48	5
2J069	33.01.05.1	LA LEVEL 4 ADDRESS INVALID INDICATOR	2	48	6
2J070	33.01.03.1	LA LEVEL 4 DATA STORE INDICATOR	2	48	7
2J071	33.01.02.1	LA LEVEL 4 DATA FETCH INDICATOR	2	48	8
2J072	33.01.06.1	LA LEVEL 4 INSTRUCTION FETCH INDICATOR	2	48	9
2J073	33.01.07.1	LA LEVEL 4 INDEX FLAG INDICATOR	2	49	12
2J074	33.01.08.1	LA LEVEL 4 INDEX COUNT ZERO INDICATOR	2	49	11
2J075	33.01.09.1	LA LEVEL 4 INDEX VALUE BELOW ZERO INDICATOR	2	49	0
2J076	33.01.10.1	LA LEVEL 4 INDEX VALUE ZERO INDICATOR	2	49	1
2J077	33.01.11.1	LA LEVEL 4 INDEX VALUE ABOVE ZERO INDICATOR	2	49	2
2J078	33.01.12.1	LA LEVEL 4 INDEX LOW INDICATOR	2	49	3
2J079	33.01.13.1	LA LEVEL 4 INDEX EQUAL INDICATOR	2	49	4
2J080	33.01.14.1	LA LEVEL 4 INDEX HIGH INDICATOR	2	49	5
2J083	32.01.01.1	LA LEVEL 4 IC FIELD POS 00-16	2	38	5-9
THROUGH	THROUGH		2	39	12-9
2J099	32.01.17.1				
2J100	32.01.20.1	LA LEVEL 4 IC FIELD PARITY FOR BITS 00-16	2	40	0
2J101	32.01.18.1	LA LEVEL 4 IC FIELD POS 17	2	40	12
2J102	32.01.19.1	LA LEVEL 4 IC FIELD POS 18	2	40	11
2J103	32.01.21.1	LA LEVEL 4 IC FIELD PARITY FOR BITS 17-18	2	40	1
2K029	31.01.01.1	LA LEVEL 3 OPERAND FIELD POS 00-75	2	21	12-9
THROUGH	THROUGH		2	22	12-9
2K104	31.01.64.1		2	23	12-9
	31.02.01.1		2	24	12-9
	THROUGH		2	25	12-9
	31.02.10.1		2	26	12-9
	31.29.01.1		2	27	12-1
	AND				
	31.29.02.1				
2L001	38.51.03.1	SCC ADVANCE ENABLES SEQUENCE TRIGGER	1	64	3
2L002	38.52.07.1	SCC LATE DECODE ENABLE TRIGGER	1	64	4
2L006	38.62.02.1	GATE OUT LAMIB TRIGGER	1	64	9
2L007	38.53.04.1	STORE DATA TIMER E TRIGGER	1	65	12
2L008	38.53.04.1	STORE DATA TIMER M TRIGGER	1	65	11
2L013	35.06.01.1	LA TO INST UNIT TIMER E TGR - LA-I E TGR-	1	65	0
2L014	35.06.02.1	LA TO I INDEX XFER M TGR - LA-I XS/F M TGR-	1	65	1
2L015	35.06.02.1	LA TO NO INDEX XFER M TGR - LA-I M-NX TGR-	1	65	2
2L016	35.33.01.1	CLEAR INDEX TIMER E TRIGGER	1	65	3
2L017	35.33.01.1	CLEAR INDEX TIMER M TRIGGER	1	65	4
2L018	35.33.01.1	WRITE INDEX TIMER E TRIGGER	1	65	5
2L019	35.33.01.1	WRITE INDEX TIMER M TRIGGER	1	65	6
2L025	38.53.01.1	LAAR 1 BUSY TGR	1	65	7
2L026	38.53.01.1	LAAR 2 BUSY TGR	1	65	8
2L032	38.01.04.1	IAUC COUNTER POS 3 TRIGGER	2	28	11
2L033	38.11.04.1	OCC COUNTER POS 3 TRIGGER	2	28	0
2L034	38.21.02.1	TBC COUNTER POS 3 TRIGGER	2	28	1
2L035	38.31.02.1	ABC COUNTER POS 3 TRIGGER	2	28	2

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
2L036	38.51.02.1	SCC COUNTER POS 3 TRIGGER	2	28	3
2L037	36.16.02.1	FROM BIT 1 - LEVEL 3	2	28	4
2L038	36.13.03.1	FROM BIT 2 - LEVEL 3	4	34	5
2L040	36.09.03.1	LA LEVEL 3 OP CODE FIELD POS 00-09	2	42	8-9
THROUGH	THROUGH		2	43	12-5
2L049	36.09.12.1				
2L050	36.09.13.1	PAR ON OP CODE POS 1-4 FOR PS J ADDR ONLY	2	43	6
2L053	36.08.02.1	DISCONNECT TAG BIT LEVEL 3	2	27	3
2L054	36.07.05.1	NOOP TAG BIT LEVEL 3	2	27	4
2L055	36.06.01.1	WORD BOUNDARY CROSSOVER TAG BIT LEVEL 3	2	27	5
2L056	36.05.01.1	LOOKAHEAD OPERATION CODE TAG BIT LEVEL 3	2	27	6
2L057	36.04.01.1	INSTRUCTION COUNTER VALID TAG BIT LEVEL 3	2	27	7
2L058	36.03.02.1	INTERNAL FETCH TAG BIT LEVEL 3	2	27	8
2L059	36.02.03.1	LEVEL CHECKED TAG BIT LEVEL 3	2	27	9
2L060	36.01.03.1	LEVEL FILLED M TAG BIT LEVEL 3	2	28	12
2L061	38.09.19.1	INDEX STORE TAG - LEVEL 3	2	27	2
2L062	36.09.14.1	EXTERNAL STORE TAG - LEVEL 3	4	4	0
2L063	36.09.15.1	INTERNAL STORE TAG - LEVEL 3	4	4	4
2L066	33.01.01.1	LA LEVEL 3 CONDITIONAL MACH CHK INDICATOR	2	47	0
2L067	33.01.18.1	LA LEVEL 3 INSTRUCTION REJECT INDICATOR	2	47	1
2L068	33.01.04.1	LA LEVEL 3 OPERATION CODE INVALID INDICATOR	2	47	2
2L069	33.01.05.1	LA LEVEL 3 ADDRESS INVALID INDICATOR	2	47	3
2L070	33.01.03.1	LA LEVEL 3 DATA STORE INDICATOR	2	47	4
2L071	33.01.02.1	LA LEVEL 3 DATA FETCH INDICATOR	2	47	5
2L072	33.01.06.1	LA LEVEL 3 INSTRUCTION FETCH INDICATOR	2	47	6
2L073	33.01.07.1	LA LEVEL 3 INDEX FLAG INDICATOR	2	47	7
2L074	33.01.08.1	LA LEVEL 3 INDEX COUNT ZERO INDICATOR	2	47	8
2L075	33.01.09.1	LA LEVEL 3 INDEX VALUE BELOW ZERO INDICATOR	2	47	9
2L076	33.01.10.1	LA LEVEL 3 INDEX VALUE ZERO INDICATOR	2	48	12
2L077	33.01.11.1	LA LEVEL 3 INDEX VALUE ABOVE ZERO INDICATOR	2	48	11
2L078	33.01.12.1	LA LEVEL 3 INDEX LOW INDICATOR	2	48	0
2L079	33.01.13.1	LA LEVEL 3 INDEX EQUAL INDICATOR	2	48	1
2L080	33.01.14.1	LA LEVEL 3 INDEX HIGH INDICATOR	2	48	2
2L083	32.01.01.1	LA LEVEL 3 IC FIELD POS 00-16	2	28	5-9
THROUGH	THROUGH		2	29	12-9
2L099	32.01.17.1				
2L100	32.01.20.1	LA LEVEL 3 IC FIELD PARITY FOR BITS 00-16	2	30	0
2L101	32.01.18.1	LA LEVEL 3 IC FIELD POSITION 17	2	30	12
2L102	32.01.19.1	LA LEVEL 3 IC FIELD POSITION 18	2	30	11
2L103	32.01.21.1	LA LEVEL 3 IC FIELD PARITY FOR BITS 17-18	2	30	1
2M029	31.01.01.1	LA LEVEL 2 OPERAND FIELDS POS 00-75	2	11	12-9
THROUGH	THROUGH		2	12	12-9
2M104	31.01.64.1		2	13	12-9
	31.02.01.1		2	14	12-9
	THROUGH		2	15	12-9
	31.02.10.1		2	16	12-9
	31.29.01.1		2	17	12-1
	AND				
	31.29.02.1				
2N001	38.31.03.1	ABC ADVANCE ENABLES SEQUENCE TRIGGER	1	62	1
2N002	38.38.01.1	TRANSFER INDICATOR TIMER E TRIGGER	1	62	2
2N003	38.38.02.1	TRANSFER INDICATOR TIMER M TRIGGER	1	62	3
2N004	38.33.01.1	ARITHMETIC BUS TIMER EE TRIGGER	1	62	4
2N005	38.33.02.1	ARITHMETIC BUS TIMER E TRIGGER	1	62	5
2N006	38.33.03.1	ARITHMETIC BUS TIMER M TRIGGER	1	62	6
2N007	35.26.01.1	INDICATOR REGISTER TIMER E TRIGGER	1	62	7
2N008	35.26.01.1	INDICATOR REGISTER TIMER M TRIGGER	1	62	8
2N009	38.39.02.1	HOUSECLEAN TIMER E TRIGGER	1	62	9
2N010	38.39.02.1	HOUSECLEAN TIMER M TRIGGER	1	63	12
2N011	38.39.01.1	LA HOUSECLEAN OVER TIMER E TRIGGER	1	63	11
2N012	38.39.01.1	LA HOUSECLEAN OVER TIMER M TRIGGER	1	63	0
2N014	38.35.04.1	ALLOW MAR FOR NEXT INSTRUCTION TRIGGER	1	63	2
2N015	38.35.04.1	MODIFY ADDRESSABLE REGISTER MODE TRIGGER	1	63	3
2N016	38.34.01.1	NOOP MODE TRIGGER	1	63	4

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
2N017	38.39.04.1	LA HOUSECLEAN MODE TRIGGER	1	63	5
2N018	38.35.05.1	INTERRUPT NEXT INSTRUCTION TRIGGER	1	63	6
2N019	38.39.05.1	LA DISABLE INTERRUPT LINE TRIGGER	1	63	7
2N020	38.23.04.1	SAU INSTRUCTION INTERRUPT BUFFER TRIGGER	1	63	8
2N021	38.38.03.1	LA INDICATOR TEST TIMER E TRIGGER	1	63	9
2N022	38.35.01.1	LA NORMAL INDICATOR TEST TIMER M TRIGGER	1	64	12
2N023	38.35.01.1	EXECUTION UNIT INDICATOR TEST M TRIGGER	1	64	11
2N024	38.35.01.1	ARITHMETIC CHECKER INDICATOR TEST TRIGGER	1	64	0
2N026	38.35.03.1	LA NOOP INDICATOR TEST TIMER M TRIGGER	1	64	2
2N032	38.01.03.1	IAUC COUNTER POSITION 2 TRIGGER	2	18	11
2N033	38.11.03.1	OCC COUNTER POSITION 2 TRIGGER	2	18	0
2N034	38.21.01.1	TBC COUNTER POSITION 2 TRIGGER	2	18	1
2N035	38.31.01.1	ABC COUNTER POSITION 2 TRIGGER	2	18	2
2N036	38.51.01.1	SCC COUNTER POSITION 2 TRIGGER	2	18	3
2N037	36.16.02.1	FROM BIT 1 - LEVEL 2	2	18	4
2N038	36.13.03.1	FROM BIT 2 - LEVEL 2	4	34	4
2N040	36.09.03.1	LA LEVEL 2 OP CODE FIELD POS 00-09	2	41	9
THROUGH	THROUGH		2	42	12-6
2N049	36.09.12.1				
2N050	36.09.13.1	PAR ON OP CODE POS 1-4 FOR PS J ADDR ONLY	2	42	7
2N053	36.08.01.1	DISCONNECT TAG BIT LEVEL 2	2	17	3
2N054	36.07.04.1	NOOP TAG BIT LEVEL 2	2	17	4
2N055	36.06.01.1	WORD BOUNDARY CROSSOVER TAG BIT LEVEL 2	2	17	5
2N056	36.05.01.1	LOOKAHEAD OPERATION CODE TAG BIT LEVEL 2	2	17	6
2N057	36.04.01.1	INSTRUCTION COUNTER VALID TAG BIT LEVEL 2	2	17	7
2N058	36.03.02.1	INTERNAL FETCH TAG BIT LEVEL 2	2	17	8
2N059	36.02.03.1	LEVEL CHECKED TAG BIT LEVEL 2	2	17	9
2N060	36.01.02.1	LEVEL FILLED M TAG BIT LEVEL 2	2	18	12
2N061	36.09.19.1	INDEX STORE TAG - LEVEL 2	2	17	2
2N062	36.09.14.1	EXTERNAL STORE TAG - LEVEL 2	4	4	11
2N063	36.09.15.1	INTERNAL STORE TAG - LEVEL 2	4	4	3
2N066	33.01.01.1	LA LEVEL 2 CONDITIONAL MACH CHK INDICATOR	2	45	9
2N067	33.01.17.1	LA LEVEL 2 INSTRUCTION REJECT INDICATOR	2	46	12
2N068	33.01.04.1	LA LEVEL 2 OPERATION CODE INVALID INDICATOR	2	46	11
2N069	33.01.05.1	LA LEVEL 2 ADDRESS INVALID INDICATOR	2	46	0
2N070	33.01.03.1	LA LEVEL 2 DATA STORE INDICATOR	2	46	1
2N071	33.01.02.1	LA LEVEL 2 DATA FETCH INDICATOR	2	46	2
2N072	33.01.06.1	LA LEVEL 2 INSTRUCTION FETCH INDICATOR	2	46	3
2N073	33.01.07.1	LA LEVEL 2 INDEX FLAG INDICATOR	2	46	4
2N074	33.01.08.1	LA LEVEL 2 INDEX COUNT ZERO INDICATOR	2	46	5
2N075	33.01.09.1	LA LEVEL 2 INDEX VALUE BELOW ZERO INDICATOR	2	46	6
2N076	33.01.10.1	LA LEVEL 2 INDEX VALUE ZERO INDICATOR	2	46	7
2N077	33.01.11.1	LA LEVEL 2 INDEX VALUE ABOVE ZERO INDICATOR	2	46	8
2N078	33.01.12.1	LA LEVEL 2 INDEX LOW INDICATOR	2	46	9
2N079	33.01.13.1	LA LEVEL 2 INDEX EQUAL INDICATOR	2	47	12
2N080	33.01.14.1	LA LEVEL 2 INDEX HIGH INDICATOR	2	47	11
2N083	32.01.01.1	LA LEVEL 2 IC FIELD POS 00-16	2	18	5-9
THROUGH	THROUGH		2	19	12-9
2N099	32.01.17.1				
2N100	32.01.20.1	LA LEVEL 2 IC FIELD PARITY FOR BITS 00-16	2	20	0
2N101	32.01.18.1	LA LEVEL 2 IC FIELD POS 17	2	20	12
2N102	32.01.19.1	LA LEVEL 2 IC FIELD POS 18	2	20	11
2N103	32.01.21.1	LA LEVEL 2 IC FIELD PARITY FOR BITS 17-18	2	20	1
2P029	31.01.01.1	LA LEVEL 1 OPERAND FIELD POS 00-75	2	1	12-9
THROUGH	THROUGH		2	2	12-9
2P104	31.01.64.1		2	3	12-9
	31.02.01.1		2	4	12-9
	THROUGH		2	5	12-9
	31.02.10.1		2	6	12-9
	31.29.01.1		2	7	12-1
	AND				
	31.29.02.1				
2Q001	38.01.06.1	1AUC ADVANCE ENABLES SEQUENCE TRIGGER	1	59	3
2Q002	38.01.10.1	LOAD PULSE MEMORY TRIGGER	1	59	4

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
2Q004	38.39.03.1	INTERRUPT INHIBITS LOAD TRIGGER	1	59	6
2Q005	38.39.03.1	PSEUDO-INTERRUPT INHIBITS LOAD TRIGGER	1	59	7
2Q006	38.39.03.1	BRANCH RECOVERY INHIBITS LOAD TRIGGER	1	59	8
2Q011	38.11.06.1	OCC ADVANCE ENABLES SEQUENCE TRIGGER	1	50	1
2Q012	35.05.01.1	OPERAND CHECK TIMER E TRIGGER	1	61	12
2Q013	35.05.01.1	OPERAND CHECK TIMER M TRIGGER	1	61	11
2Q014	35.05.02.1	OPERAND CORRECT TIMER E TRIGGER	1	61	0
2Q015	35.05.02.1	OPERAND CORRECT TIMER M TRIGGER	1	61	1
2Q021	38.21.03.1	TBC ADVANCE ENABLES SEQUENCE TRIGGER	1	61	8
2Q023	38.22.15.1	TBC LATE DECODE ENABLE TRIGGER	1	61	9
2Q024	38.25.01.1	TRANSFER BUS TIMER E TRIGGER	1	62	12
2Q025	38.25.02.1	TRANSFER BUS TIMER M TRIGGER	1	62	11
2Q032	38.01.02.1	IAUC COUNTER POSITION 1 TRIGGER	2	8	11
2Q033	38.11.02.1	OCC COUNTER POSITION 1 TRIGGER	2	8	0
2Q034	38.21.01.1	TBC COUNTER POSITION 1 TRIGGER	2	8	1
2Q035	38.31.01.1	ABC COUNTER POSITION 1 TRIGGER	2	8	2
2Q036	38.51.01.1	SCC COUNTER POSITION 1 TRIGGER	2	8	3
2Q037	36.16.02.1	FROM BIT 1 - LEVEL 1	2	8	4
2Q038	36.13.03.1	FROM BIT 2 - LEVEL 1	4	34	3
2Q040	36.09.03.1	LA LEVEL 1 OP CODE FIELD POS 00-09	2	41	12-7
THROUGH	THROUGH				
2Q049	36.09.12.1				
2Q050	36.09.13.1	PAR ON OP CODE POS 1-4 FOR PS J ADDR ONLY	2	41	8
2Q053	36.08.01.1	DISCONNECT TAG BIT LEVEL 1	2	7	3
2Q054	36.07.03.1	NOOP TAG BIT LEVEL 1	2	7	4
2Q055	36.06.01.1	WORD BOUNDARY CROSSOVER TAG BIT LEVEL 1	2	7	5
2Q056	36.05.01.1	LOOKAHEAD OPERATION CODE TAG BIT LEVEL 1	2	7	6
2Q057	36.04.01.1	INSTRUCTION COUNTER VALID TAG BIT LEVEL 1	2	7	7
2Q058	36.03.02.1	INTERNAL FETCH TAG BIT LEVEL 1	2	7	8
2Q059	36.02.03.1	LEVEL CHECKED TAG BIT LEVEL 1	2	7	9
2Q060	36.01.01.1	LEVEL FILLED M TAG BIT LEVEL 1	2	8	12
2Q 061	36.09.19.1	INDEX STORE TAG - LEVEL 1	2	7	2
2Q062	36.09.14.1	EXTERNAL STORE TAG - LEVEL 1	4	4	12
2Q063	36.09.15.1	INTERNAL STORE TAG - LEVEL 1	4	4	2
2Q 066	33.01.01.1	LA LEVEL 1 CONDITIONAL MACH CHK INDICATOR	2	44	6
2Q067	33.01.16.1	LA LEVEL 1 INSTRUCTION REJECT INDICATOR	2	44	7
2Q068	33.01.04.1	LA LEVEL 1 OPERATION CODE INVALID INDICATOR	2	44	8
2Q069	33.01.05.1	LA LEVEL 1 ADDRESS INVALID INDICATOR	2	44	9
2Q070	33.01.03.1	LA LEVEL 1 DATA STORE INDICATOR	2	45	12
2Q071	33.01.02.1	LA LEVEL 1 DATA FETCH INDICATOR	2	45	11
2Q072	33.01.06.1	LA LEVEL 1 INSTRUCTION FETCH INDICATOR	2	45	0
2Q073	33.01.07.1	LA LEVEL 1 INDEX FLAG INDICATOR	2	45	1
2Q074	33.01.08.1	LA LEVEL 1 INDEX COUNT ZERO INDICATOR	2	45	2
2Q075	33.01.09.1	LA LEVEL 1 INDEX VALUE BELOW ZERO INDICATOR	2	45	3
2Q076	33.01.10.1	LA LEVEL 1 INDEX VALUE ZERO INDICATOR	2	45	4
2Q077	33.01.11.1	LA LEVEL 1 INDEX VALUE ABOVE ZERO INDICATOR	2	45	5
2Q078	33.01.12.1	LA LEVEL 1 INDEX LOW INDICATOR	2	45	6
2Q079	33.01.13.1	LA LEVEL 1 INDEX EQUAL INDICATOR	2	45	7
2Q080	33.01.14.1	LA LEVEL 1 INDEX HIGH INDICATOR	2	45	8
2Q083	32.01.01.1	LA LEVEL 1 IC FIELD POS 00-16	2	8	5-9
THROUGH	THROUGH				
2Q099	32.01.17.1		2	9	12-9
2Q100	32.01.20.1	LA LEVEL 1 IC FIELD PARITY FOR BITS 00-16	2	10	0
2Q101	32.01.18.1	LA LEVEL 1 IC FIELD POS 17	2	10	12
2Q102	32.01.19.1	LA LEVEL 1 IC FIELD POS 18	2	10	11
2Q103	32.01.21.1	LA LEVEL 1 IC FIELD PARITY FOR BITS 17-18	2	10	1
3F001	28.10.11.1	FLOATING POINT LOADER FPDD M TGR	1	57	12
3F002	28.13.21.1	FLOATING POINT LEFT LOADER 2 MEMORY TGR	1	57	11
3F003	28.13.31.1	FLOATING POINT LEFT LOADER 3 MEMORY TGR	1	57	0
3F004	28.13.41.1	FLOATING POINT LEFT LOADER 4 MEMORY TGR	1	57	1

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
3F006	28.14.21.1	FLOATING POINT RIGHT LOADER 2 MEMORY TGR	1	57	3
3F007	28.14.31.1	FLOATING POINT RIGHT LOADER 3 MEMORY TGR	1	57	4
3F008	28.14.41.1	FLOATING POINT RIGHT LOADER 4 MEMORY TGR	1	57	5
3F010	28.42.55.1	HALT REQUIRED	1	57	7
3F011	28.42.55.1	PROGRAM HALT	1	57	8
3F012	28.43.11.1	PROGRAM START REO	1	57	9
3F013	28.43.12.1	PROGRAM SINGLE OPERATION	1	58	12
3F014	28.43.18.1	PROGRAM MANUAL OPERATION GO	1	58	11
3F015	28.43.14.1	PROGRAM SINGLE DISPLAY OP	1	58	0
3F016	28.43.15.1	PROGRAM CONSECUTIVE DISPLAY	1	58	1
3F017	28.43.16.1	PROGRAM SINGLE STORE	1	58	2
3F018	28.43.17.1	PROGRAM CONSECUTIVE STORE	1	58	3
3F019	28.43.13.1	PROGRAM ENTER INSTRUCTION OP	1	58	4
3F020	28.43.13.1	PROGRAM ENTER INSTRUCTION MODE	1	58	5
3F021	28.43.21.1	PROGRAM REPEAT INSTRUCTION	1	58	6
3F022	28.60.27.1	INDEX STORAGE READ TEST	1	58	7
3F023	28.60.27.1	INDEX STORAGE WRITE TEST	1	58	8
3F024	28.60.27.1	INDEX STORAGE TEST ADDRESS ADVANCE	1	58	9
3F025	28.60.27.1	INDEX STORAGE TEST ERROR STOP	1	59	12
3F026	28.42.54.1	TIME CLOCK OPERATION TEST	1	59	11
3F028	28.70.84.1	MANUAL DISABLE INTERRUPT ENABLE	1	59	1
3F029	28.42.54.1	MANUAL DISABLE TIME CLOCK	1	59	2
3G001	28.13.12.1	FLOATING POINT LOADER FP DD E TGR	1	55	5
3G002	28.13.21.1	FLOATING POINT LEFT LOADER 2 EXECUTE TGR	1	55	6
3G003	28.13.32.1	FLOATING POINT LEFT LOADER 3 EXECUTE TGR	1	55	7
3G004	28.13.41.1	FLOATING POINT LEFT LOADER 4 EXECUTE TGR	1	55	8
3G006	28.14.21.1	FLOATING POINT RIGHT LOADER 2 EXECUTE TGR	1	56	12
3G007	28.14.32.1	FLOATING POINT RIGHT LOADER 3 EXECUTE TGR	1	56	11
3G008	28.14.41.1	FLOATING POINT RIGHT LOADER 4 EXECUTE TGR	1	56	0
3G009	28.26.50.1	Z RIGHT FLOATING POINT CLASS 1, 2, 3, 4 AND 6	1	56	1-3
THROUGH	AND	INDICATORS	1	54	1
3G013	28.26.51.1		1	56	5
3G015	28.52.02.1	UPDATED INDEX REGISTER N51 INDEX COUNT 0	1	56	6
3G016	28.52.03.1	UPDATED INDEX REGISTER N52 INDEX VALUE LT 0	1	56	7
3G017	28.52.03.1	UPDATED INDEX REGISTER N53 INDEX VALUE 0	1	56	8
3G018	28.52.04.1	UPDATED INDEX REGISTER N54 INDEX VALUE GT 0	1	56	9
3H001	28.11.11.1	VFL LOADER 1 MEMORY TGR	1	53	2
3H002	28.11.21.1	VFL LOADER 2 MEMORY TGR	1	53	3
3H003	28.11.31.1	VFL LOADER 3 MEMORY TGR	1	53	4
3H004	28.11.41.1	VFL LOADER 4 MEMORY TGR	1	53	5
3H005	28.11.53.1	VFL LOADER 5 MEMORY TGR	1	53	6
3H006	28.12.11.1	INDEX OPERAND FETCH 1 MEMORY TGR	1	53	7
3H008	28.22.02.1	FULL WORD TRIGGER	1	53	9
3H009	28.26.52.1	Z LEFT FLOATING POINT CLASS 1	1	54	12
3H010	28.26.53.1	Z LEFT FLOATING POINT CLASS 2	1	54	11
3H011	28.26.53.1	Z LEFT FLOATING POINT CLASS 3	1	54	0
3H012	28.26.53.1	Z LEFT FLOATING POINT CLASS 4	1	54	4
3H013	28.26.53.1	Z LEFT FLOATING POINT CLASS 6	1	54	2
3H015	28.52.02.1	UPDATED INDEX REGISTER N38 INDEX FLAG	1	54	3
3H016	28.52.04.1	UPDATED INDEX REGISTER N48 INDEX LOW	1	54	4
3H017	28.52.05.1	UPDATED INDEX REGISTER N49 INDEX EQUAL	1	54	5
3H018	28.52.05.1	UPDATED INDEX REGISTER N50 INDEX HIGH	1	54	6
3H027	28.42.83.1	RUNNING INDICATOR	1	55	2
3H028	21.02.02.1	INACTIVE INDICATOR	1	55	3
3H029	28.43.21.1	MAINTENANCE MODE INDICATOR	1	55	4
3H033	22.11.01.1	2Y REGISTER POS 32-63	1	23	6-9
THROUGH	THROUGH		1	24	12-9
3H064	22.11.35.1		1	25	12-9
			1	26	12-1
3H065	22.11.19.1	2Y REGISTER PARITY 32-49 OR C08	1	26	6
3H066	22.11.26.1	2Y REGISTER PARITY 50-55 OR C16	1	26	7
3H067	22.11.31.1	2Y REGISTER PARITY 56-59 OR C32	1	26	8
3H068	22.11.36.1	2Y REGISTER PARITY 60-63 OR C T	1	26	9

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
3J001	28.11.11.1	VFL LOADER 1 EXECUTE TGR	1	51	3
3J002	28.11.22.1	VFL LOADER 2 EXECUTE TGR	1	51	4
3J003	28.11.32.1	VFL LOADER 3 EXECUTE TGR	1	51	5
3J004	28.11.42.1	VFL LOADER 4 EXECUTE TGR	1	51	6
3J005	28.11.51.1	VFL LOADER 5 EXECUTE TGR	1	51	7
3J006	28.12.11.1	INDEX OPERAND FETCH 1 EXECUTE TGR	1	51	8
3J008	28.22.02.1	WORD BOUNDARY CROSSOVER TRIGGER	1	52	12
3J009	28.27.32.1	FLOATING POINT Z ALTERNATOR	1	52	11
3J010	28.42.53.1	FLOATING POINT INCOMPLETE WAIT	1	52	0
3J013	28.15.80.1	WORD BOUNDARY CROSSOVER OR DECODE MEM TGR	1	52	1
3J018	27.14.02.1	Z REG RIGHT ADDRESS 8	1	52	2
3J019	27.14.02.1	Z REG LEFT ADDRESS 8	1	52	3
3J021	28.86.44.1	XCL 4 M TGR	1	52	5
3J022	28.86.54.1	XST 4 M TGR	1	52	6
3J023	28.87.14.1	LDX 5 M TGR	1	52	7
3J024	28.88.14.1	LOP 2 M TGR	1	52	8
3J025	28.88.24.1	LOP 3 M TGR	1	52	9
3J026	28.88.34.1	LOP 4 M TGR	1	53	12
3J027	28.88.44.1	LOP 5 M TGR	1	53	11
3J028	28.89.14.1	FINIS 1 RESET 1-EX CONTROLS	1	53	0
3J029	28.89.24.1	FINIS 2 RESET F-EX CONTROLS	1	53	1
3K010	28.26.11.1	PREPARE TO START	1	49	11
3K011	28.27.30.1	CONDITION Z DECODE EXECUTE TGR RST ZL DEC	1	49	0
3K012	28.26.10.1	CONDITION HALF Y	1	49	1
3K013	28.15.80.1	WORD BOUNDARY CROSSOVER OR DECODE EX TGR	1	49	2
3K014	28.42.72.1	I-UNIT RECOVERY REQUIRED	1	49	3
3K015	28.78.14.1	TC HAS STEPPED ONCE DURING LVE & EX & EXIC	1	49	4
3K016	28.70.84.1	INTERRUPT MECHANISM ENABLED	1	49	5
3K017	22.11.37.1	1Y REGISTER MEMORY CHECK	1	49	6
3K018	22.11.37.1	2Y REGISTER MEMORY CHECK	1	49	7
3K019	28.51.11.1	NON IDENTIFIABLE CHECK ERROR	1	49	8
3K020	28.83.14.1	LST 3 M TGR	1	49	9
3K021	28.83.24.1	LDX 3 M TGR	1	50	12
3K023	28.83.44.1	XS STORE 1ST STORE TMT-SWP	1	50	0
3K024	28.84.14.1	INSTRUCTION COUNTER LOAD 1 IC LA	1	50	1
3K025	28.85.14.1	RIGHT ADDRESS MODIFICATION STEP UP OR DOWN	1	51	12
3K026	28.86.14.1	LST 4 M TGR	1	51	11
3K027	28.86.24.1	LDX 6 M TGR	1	51	0
3K028	28.86.34.1	LDX 4 M TGR	1	51	1
3L001	28.42.41.1	Z LEFT INST EXE BLOK INST FETCH TO 1Y	1	39	5
3L002	28.42.41.1	Z RIGHT INST EXE BLOK INST FETCH TO 1Y	1	39	6
3L003	28.42.41.1	Z LEFT INST EXE BLOK INST FETCH TO 2Y	1	39	7
3L004	28.42.41.1	Z RIGHT INST EXE BLOK INST FETCH TO 2Y	1	39	8
3L005	28.42.42.1	Z LEFT INST EXE SUSPEND INST FETCH TO 1Y	1	39	9
3L006	28.42.42.1	Z RIGHT INST EXE SUSPEND INST FETCH TO 1Y	1	40	12
3L007	28.42.43.1	Z LEFT INST EXE SUSPEND INST FETCH TO 1 Y	1	40	11
3L008	28.42.43.1	Z RIGHT INST EXE SUSPEND INST FETCH TO 1Y	1	40	0
3L010	28.26.11.1	I HALF WORD EXECUTION Z RIGHT	1	47	2
3L011	28.27.30.1	CONDITION Z DECODE MEMORY TGR DEC ZL	1	47	3
3L012	28.26.10.1	CONDITION 2Y TO ZL	1	47	4
3L013	28.15.50.1	INDEX FETCH OR DECODE Z LEFT MEMORY TGR	1	47	5
3L014	28.42.54.1	TIME CLOCK OP	1	47	6
3L015	28.42.56.1	EXECUTE WAIT	1	47	7
3L016	28.41.12.1	RESET 2 MEMORY TGR	1	47	8
3L017	28.51.03.1	Z LEFT IDENTIFIABLE CHECK ERROR	1	47	9
3L018	28.51.02.1	Z RIGHT IDENTIFIABLE CHECK ERROR	1	48	12
3L019	28.78.14.1	UNENDED SEQUENCE OF LVE & EX & EXIC	1	48	11
3L020	28.80.54.1	1ST OPERAND FETCH TMT-SWP COMPLETED	1	48	0
3L021	28.81.54.1	1ST OPERAND FETCH TMT-SWP COMPLETED	1	48	1
3L022	28.81.14.1	LEFT ADDRESS MODIFICATION STEP UP OR DOWN	1	48	2
3L023	28.82.14.1	2ND FETCH SWP EXT MEM	1	48	3
3L024	28.82.14.1	2ND FETCH SWP EXT MEMORY	1	48	4

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
3L025	28.82.24.1	XS FETCH 2ND FETCH SWP	1	48	5
3L026	28.82.34.1	2ND FETCH SWP INTERNAL REG	1	48	6
3L027	28.82.44.1	CHECKER CYCLE FOLLOWING XSF5	1	48	7
3M001	28.42.61.1	Z LEFT EMPTY TGR	1	30	11
3M002	28.42.61.1	Z RIGHT EMPTY TGR	1	30	0
3M003	28.42.62.1	Z LEFT EMPTY CONDITION ON ACCEPT	1	30	1
3M004	28.42.62.1	Z RIGHT EMPTY CONDITION ON ACCEPT	1	37	3
3M005	28.42.44.1	SUSPEND INTERLOCK TRIGGER	1	37	4
3M006	28.42.32.1	2Y INST FETCH BOUNDARY ALARM	1	37	5
3M007	28.42.33.1	2Y IDENTIFIABLE CHECK ERROR	1	37	6
3M008	28.42.32.1	2Y ADDRESS INVALID	1	37	7
3M009	28.26.23.1	1 BIT MODIFICATION	1	37	8
3M010	28.26.11.1	1 HALF WORD READY	1	37	9
3M012	28.26.10.1	CONDITION 2Y TO ZR	1	38	11
3M013	28.15.50.1	INDEX FETCH OR DECODE Z LEFT EXECUTE TGR	1	38	0
3M014	28.42.54.1	TIME CLOCK ADVANCE REQUIRED	1	38	1
3M015	28.87.44.1	EXECUTE MODE	1	38	2
3M016	28.41.12.1	RESET 2 EXECUTE TGR	1	38	3
3M017	28.51.04.1	Z LEFT ADDRESS INVALID	1	38	4
3M018	28.51.04.1	Z RIGHT ADDRESS INVALID	1	38	5
3M019	28.51.06.1	Z DATA FETCH OUT OF BOUNDS	1	38	6
3M020	28.79.14.1	TEST BRANCH ADR FOR OUT OF BOUNDS	1	38	7
3M021	28.79.22.1	PROGRAM OPERAND LEVEL LA LOAD	1	38	8
3M022	28.79.32.1	PROGRAM FETCH LEVEL LA LOAD	1	38	9
3M023	28.79.42.1	PROGRAM STORE LEVEL LA LOAD	1	39	12
3M024	28.79.52.1	PROGRAM RECOVERY LEVEL LA LOAD	1	39	11
3M025	28.80.14.1	1ST FETCH TMT-SWP EXT MEMORY	1	39	0
3M026	28.80.14.1	1ST FETCH TMT-SWP EXT MEMORY	1	39	1
3M027	28.80.24.1	XS FETCH 1ST FETCH TMT-SWP	1	39	2
3M028	28.80.34.1	1ST FETCH TMT-SWP INTERNAL REGISTER	1	39	3
3M029	28.80.44.1	CHECKER CYCLE FOLLOWING XSF4	1	39	4
3M033	22.11.01.1	1Y REGISTER POS 32-63	1	13	6-9
THROUGH	THROUGH			THRU	12-9
3M064				16	12-1
3M065	22.11.19.1	1Y REGISTER PARITY 32-49 OR C08	1	16	6
3M066	22.11.26.1	1Y REGISTER PARITY 50-55 OR C16	1	16	7
3M067	22.11.31.1	1Y REGISTER PARITY 56-59 OR C32	1	16	8
3M068	22.11.36.1	1Y REGISTER PARITY 60-63 OR C T	1	16	9
3N001	28.42.11.1	1Y EMPTY TRIGGER	1	27	6
3N002	28.42.11.1	2Y EMPTY TRIGGER	1	27	7
3N003	28.42.21.1	EVEN BRANCH TRIGGER	1	27	8
3N004	28.42.21.1	ODD BRANCH TRIGGER	1	27	9
3N005	28.42.21.1	RECOVERY GATE	1	28	12
3N006	28.42.31.1	1Y INST FETCH BOUNDARY ALARM	1	28	11
3N007	28.42.33.1	1Y IDENTIFIABLE CHECK ERROR	1	28	0
3N008	28.42.31.1	1Y ADDRESS INVALID	1	28	1
3N009	28.26.21.1	Z RIGHT MODIFY REQUIRED	1	28	2
3N010	28.26.62.1	Z RIGHT FLOATING POINT TGR	1	28	3
3N011	28.26.61.1	Z RIGHT I HALF WORD	1	28	4
3N012	28.26.60.1	FULL WORD NOT STRAIGHT	1	28	5
3N013	28.15.60.1	Y RIGHT TO Z RIGHT MEMORY TGR	1	28	6
3N014	28.42.52.1	PROGRESSIVE INDEXING OP	1	28	7
3N016	28.42.82.1	BRANCH RECOVERY OP	1	28	9
3N017	28.51.05.1	Z LEFT INSTRUCTION FETCH	1	29	12
3N018	28.51.05.1	Z RIGHT INSTRUCTION FETCH	1	29	11
3N019	28.51.06.1	Z DATA STORE	1	29	0
3N020	28.75.84.1	BRANCH	1	29	1
3N021	28.75.84.1	BRANCH	1	29	2
3N022	28.76.14.1	BRANCH	1	29	3
3N023	28.77.14.1	LOAD STORE 1 INTO LA	1	29	4

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
3N024	28.78.24.1	GEOMETRIC LOAD FIRST TIME TGR.	1	29	5
3N025	28.77.24.1	INDEX CLEAR 1 M2 DX 1ST STORE	1	29	6
3N026	28.77.34.1	INDEX STORE 1 DX 1ST STORE	1	29	7
3N027	28.77.44.1	LOAD OP CODE TO LA 1 M TGR	1	29	8
3N028	28.78.14.1	ALLOW TIME CLOCK BREAK IN	1	29	9
3N029	28.78.34.1	PX ROUTINE USE YL TGR	1	30	12
3N033	22.11.01.1	2Y REGISTER POS 00-31	1	21	12-9
THROUGH	THROUGH		1	22	12-9
3N064	22.11.35.1		1	23	12-5
3N065	22.11.19.1	2Y REGISTER PARITY 00-17 OR C00	1	26	2
3N066	22.11.26.1	2Y REGISTER PARITY 18-23 OR C01	1	26	3
3N067	22.11.31.1	2Y REGISTER PARITY 24-27 OR C02	1	26	4
3N068	22.11.36.1	2Y REGISTER PARITY 28-31 OR C04	1	26	5
3P001	28.41.23.1	INSTRUCTION COUNTER CLOCK CHECK 1Y	1	18	5
3P002	28.41.23.1	INSTRUCTION COUNTER FETCH OUTSTANDING 1Y	1	18	6
3P003	28.41.33.1	INSTRUCTION COUNTER BLOCK CHECK 2Y	1	18	7
3P004	28.41.33.1	INSTRUCTION COUNTER FETCH OUTSTANDING 2Y	1	18	8
3P006	28.41.50.1	INSTRUCTION WORD CHECK ALTERNATOR	1	19	12
3P007	28.41.23.1	INSTRUCTION COUNTER RETURN TO 1Y	1	19	11
3P008	28.41.33.1	INSTRUCTION COUNTER RETURN TO 2Y	1	19	0
3P009	28.26.23.1	Z LEFT MODIFY REQUIRED	1	19	1
3P010	28.26.62.1	Z LEFT FLOATING POINT TGR	1	19	2
3P011	28.26.61.1	I HALF WORD - Z LEFT	1	19	3
3P012	28.26.60.1	FULL-WORD STRAIGHT	1	19	4
3P013	28.15.61.1	Y RIGHT TO Z RIGHT EXECUTE TGR	1	19	5
3P014	28.42.52.1	PROGRESSIVE INDEXING ROUTINE REQUIRED	1	19	6
3P016	28.87.64.1	INSTRUCTION EXECUTE IN PROGRESS	1	19	8
3P017	28.51.09.1	W SPECIAL ADDRESS 00-15	1	19	9
3P018	28.51.09.1	W INDEX ADDRESS 16-31	1	20	12
3P019	28.51.09.1	W NON EXISTENT ADDRESS	1	20	11
3P020	28.73.14.1	CHECKER CYCLE FOR EXTERNAL DX FETCH	1	20	0
3P021	28.74.14.1	CORRECT CYCLE TIMER FOR ALL ECC CHECKER CY	1	20	1
3P022	28.75.14.1	MISCELLANEOUS DELAY CYCLE	1	27	12
3P023	28.75.24.1	LOAD X VIA CHECKER	1	27	11
3P024	28.75.34.1	COUNT 1 M COUNT W OR X DOWN	1	27	0
3P025	28.75.44.1	LOAD X VIA ADDER.	1	27	1
3P026	28.75.54.1	DX LOGIC CYCLE	1	27	2
3P027	28.75.64.1	IX LOGIC CYCLE	1	27	3
3P028	28.75.74.1	X FIELD TRANSFER TO X OR W	1	27	4
3P029	28.75.74.1	X FIELD TRANSFER TO X OR W	1	27	5
3Q001	28.41.11.1	RESET 1 MEMORY TGR	1	9	4
3Q002	28.41.21.1	INSTRUCTION FETCH TO 1Y MEMORY TGR	1	9	5
3Q003	28.41.31.1	INSTRUCTION FETCH TO 2Y MEMORY TGR 1	1	9	6
3Q004	28.41.31.1	INSTRUCTION FETCH TO 2Y MEMORY TGR 2	1	9	7
3Q005	28.41.41.1	INSTRUCTION COUNTER ADVANCE MEMORY TGR	1	9	8
3Q006	28.41.51.1	INSTRUCTION WORD CHECK 1Y MEMORY TGR	1	9	9
3Q007	28.41.61.1	INSTRUCTION WORD CHECK 2Y MEMORY TGR	1	10	12
3Q008	28.41.71.1	INSTRUCTION CORRECT MEMORY TGR	1	10	11
3Q009	28.15.10.1	Y LEFT TO Z RIGHT MEMORY TGR	1	10	0
3Q010	28.15.30.1	Y RIGHT TO Z LEFT MEMORY TGR	1	10	1
3Q011	28.15.40.1	MODIFIED Z LEFT MEMORY TGR	1	17	12
3Q012	28.15.20.1	MODIFIED Z RIGHT MEMORY TGR	1	17	11
3Q013	28.15.70.1	Y LEFT TO Z LEFT MEMORY TGR	1	17	0
3Q014	28.42.71.1	PREPARE FOR I-UNIT RECOVERY	1	17	1
3Q015	28.42.83.1	INITIAL PROGRAM LOAD	1	17	2
3Q016	28.42.82.1	INTERRUPT OPERATION	1	17	3
3Q017	28.51.07.1	Z RIGHT SPECIAL ADDRESS 00-15	1	17	4
3Q018	28.51.07.1	Z RIGHT INDEX ADDRESS 16-31	1	17	5
3Q019	28.51.07.1	Z RIGHT NON EXISTENT ADDRESS	1	17	6
3Q020	28.71.14.1	INDEX STORAGE FETCH 3 DX J FETCH	1	17	7
3Q021	28.71.24.1	CHECKER CYCLE WITH XSF3	1	17	8
3Q022	28.71.34.1	COUNT ZERO REFILL M	1	17	9

TABLE 3.4.1. 7101 CE CONSOLE INDICATORS (cont'd)

INDICATOR LOCATION	TRIGGER LOCATION (ALD PAGE)	DESCRIPTIVE TITLE	SCAN CARD NO.	CARD COL.	CARD ROW (T TO B)
3Q023	28.71.40.1	PROGRAM BRANCH OK	1	18	12
3Q024	28.72.24.1	BLOCK CHECK 1Y M	1	18	11
3Q025	28.72.34.1	BLOCK CHECK 2Y M	1	18	0
3Q026	28.72.44.1	RETURNED TO 1Y DX	1	18	1
3Q027	28.72.54.1	RETURNED TO 2Y DX	1	18	2
3Q028	28.72.64.1	RETURNED TO Y	1	18	3
3R001	28.41.11.1	RESET 1 EXECUTE TRIGGER	1	7	11
3R002	28.41.21.1	INSTRUCTION FETCH TO 1Y EXECUTE TGR	1	7	0
3R003	28.41.31.1	INSTRUCTION FETCH TO 2Y EXECUTE TGR	1	7	1
3R004	28.41.41.1	INSTRUCTION COUNTER ADVANCE EXEC TGR 1	1	7	2
3R005	28.41.41.1	INSTRUCTION COUNTER ADVANCE EXEC TGR 2	1	7	3
3R006	28.41.51.1	INSTRUCTION WORD CHECK 1Y EXECUTE TGR	1	7	4
3R007	28.41.61.1	INSTRUCTION WORD CHECK 2Y EXECUTE TGR	1	7	5
3R008	28.41.71.1	INSTRUCTION CORRECT EXECUTE TGR	1	7	6
3R009	28.15.11.1	Y LEFT TO Z RIGHT EXECUTE TGR	1	7	7
3R010	28.15.30.1	Y RIGHT TO Z LEFT EXECUTE TGR	1	7	8
3R011	28.15.40.1	MODIFIED Z LEFT EXECUTE TGR	1	7	9
3R012	28.15.20.1	MODIFIED Z RIGHT EXECUTE TGR	1	8	12
3R013	28.15.70.1	Y LEFT TO Z LEFT EXECUTE TGR	1	8	11
3R014	28.42.51.1	STORE WAIT LA TO 16-31 OR 11&12	1	8	0
3R015	28.42.84.1	INITIAL PROGRAM LOAD FROM EXCHANGE	1	8	1
3R016	28.42.81.1	LOOKAHEAD RECOVERY MODE	1	8	2
3R017	28.51.08.1	Z LEFT SPECIAL ADDRESS 00-15	1	8	3
3R018	28.51.08.1	Z LEFT INDEX ADDRESS 16-31	1	8	4
3R019	28.51.08.1	Z LEFT NON EXISTENT ADDRESSS	1	8	5
3R020	28.70.14.1	BRANCH DEC 3 M	1	8	6
3R021	28.70.24.1	BRANCH EMF 5 M1	1	8	7
3R022	28.70.24.1	BRANCH EMF 5 M2	1	8	8
3R023	28.70.24.1	BRANCH EMF 5 M3	1	8	9
3R024	28.70.34.1	EXTERNAL MEMORY FETCH 1 M1	1	9	12
3R025	28.70.34.1	EXTERNAL MEMORY FETCH 1 M2	1	9	11
3R026	28.70.44.1	INDEX STORAGE FETCH 1 DX 1ST FETCH	1	9	0
3R027	28.70.54.1	INTERNAL REGISTER FETCH 1 M	1	9	1
3R028	28.70.64.1	CHECKER CYCLE WITH XSF1	1	9	2
3R029	28.70.74.1	EXTERNAL MEMORY FETCH 6 M	1	9	3
3S033	22.11.01.1	1 Y REGISTER POS 00-31	1	11	12-9
THROUGH	THROUGH		1	12	12-9
3S064	22.11.35.1		1	13	12-4
3S065	22.11.19.1	1Y REGISTER PARITY 00-17 OR C00	1	16	2
3S066	22.11.26.1	1Y REGISTER PARITY 18-23 OR C01	1	16	3
3S067	22.11.31.1	1Y REGISTER PARITY 24-27 OR C02	1	16	4
3S068	22.11.36.1	1Y REGISTER PARITY 28-31 OR C04	1	16	5

PRI SMP	SEC SMP	COL	ROW 9	8	7	6	5	4	3	2	1	0	11	12	COL	COMMENTS
1	2 1	1	2A040	2A039	2A038	2A037	2A036	2A035	2A034	2A033	2A032	2A031	2A030	2A029	1	
1	3 2	2	2A053	2A052	2A051	2A050	2A049	2A048	2A046	2A045	2A044	2A043	2A042	2A041	2	X REG
1	5 4	3	2A068	2A067	2A066	2A065	2A063	2A062	2A061	2A060	2A058	2A057	2A056	2A055	3	BITS
1	6 5	4	2A080	2A079	2A078	2A077	2A076	2A075	2A074	2A073	2A072	2A071	2A070	2A069	4	0-63, 8P
1	8 7	5	2A095	2A094	2A093	2A092	2A090	2A089	2A088	2A087	2A086	2A085	2A082	2A081	5	
1	9 8	6	2A096	2A091	2A084	2A083	2A064	2A059	2A054	2A047	2A100	2A099	2A098	2A097	6	
1	11 10	7	3R011	3R010	3R009	3R008	3R007	3R006	3R005	3R004	3R003	3R002	3R001	2A101	7	
1	12 11	8	3R023	3R022	3R021	3R020	3R019	3R018	3R017	3R016	3R015	3R014	3R013	3R012	8	I CONTROLS
1	14 13	9	3Q006	3Q005	3Q004	3Q003	3Q002	3Q001	3R029	3R028	3R027	3R026	3R025	3R024	9	BITS 1-39
1	15 14	10									3Q010	3Q009	3Q008	3Q007	10	
2	2 1	11	3S044	3S043	3S042	3S041	3S040	3S039	3S038	3S037	3S036	3S035	3S034	3S033	11	1Y REG
2	3 2	12	3S056	3S055	3S054	3S053	3S052	3S051	3S050	3S049	3S048	3S047	3S046	3S045	12	BITS 0-63, 8P
2	5 4	13	3M036	3M035	3M034	3M033	3S064	3S063	3S062	3S061	3S060	3S059	3S058	3S057	13	
2	6 5	14	3M048	3M047	3M046	3M045	3M044	3M043	3M042	3M041	3M040	3M039	3M038	3M037	14	
2	8 7	15	3M060	3M059	3M058	3M057	3M056	3M055	3M054	3M053	3M052	3M051	3M050	3M049	15	
2	9 8	16	3M068	3M067	3M066	3M065	3S068	3S067	3S066	3S065	3M064	3M063	3M062	3M061	16	
2	11 10	17	3Q022	3Q021	3Q020	3Q019	3Q018	3Q017	3Q016	3Q015	3Q014	3Q013	3Q012	3Q011	17	I CONTROLS
2	12 11	18		3P004	3P003	3P002	3P001		3Q028	3Q027	3Q026	3Q025	3Q024	3Q023	18	BITS 40-79
2	14 13	19	3P017	3P016		3P014	3P013	3P012	3P011	3P010	3P009	3P008	3P007	3P006	19	
2	15 14	20									3P021	3P020	3P019	3P018	20	
3	2 1	21	3N044	3N043	3N042	3N041	3N040	3N039	3N038	3N037	3N036	3N035	3N034	3N033	21	2Y REG
3	3 2	22	3N056	3N055	3N054	3N053	3N052	3N051	3N050	3N049	3N048	3N047	3N046	3N045	22	BITS 0-63, 8P
3	5 4	23	3H036	3H035	3H034	3H033	3N064	3N063	3N062	3N061	3N060	3N059	3N058	3N057	23	
3	6 5	24	2H048	3H047	3H046	3H045	3H044	3H043	3H042	3H041	3H040	3H039	3H038	3H037	24	
3	8 7	25	3H060	3H059	3H058	3H057	3H056	3H055	3H054	3H053	3H052	3H051	3H050	3H049	25	
3	9 8	26	3H068	3H067	3H066	3H065	3N068	3N067	3N066	3N065	3H064	3H063	3H062	3H061	26	
3	11 10	27	3N004	3N003	3N002	3N001	3P029	3P028	3P027	3P026	3P025	3P024	3P023	3P022	27	I CONTROLS
3	12 11	28	3N016		3N014	3N013	3N012	3N011	3N010	3N009	3N008	3N007	3N006	3N005	28	BITS 80-119
3	14 13	29	3N028	3N027	3N026	3N025	3N024	3N023	3N022	3N021	3N020	3N019	3N018	3N017	29	
3	15 14	30									3M003	3M002	3M001	3N029	30	
4	2 1	31	2B039	2B038	2B037	2B036	2B035	2B034	2B033	2B032	2B031	2B030	2B029	2B028	31	Z REG
4	3 2	32	2B053	2B052	2B051	2B050	2B049	2B047	2B045	2B044	2B043	2B042	2B041	2B040	32	BITS 0-63, 10P
4	5 4	33	2B068	2B067	2B066	2B065	2B063	2B062	2B061	2B060	2B058	2B057	2B056	2B055	33	
4	6 5	34	2B081	2B080	2B079	2B078	2B077	2B076	2B075	2B073	2B072	2B071	2B070	2B069	34	
4	8 7	35	2B095	2B094	2B093	2B092	2B090	2B089	2B088	2B087	2B086	2B085	2B083	2B082	35	
4	9 8	36	2B091	2B084	2B074	2B064	2B059	2B054	2B048	2B046	2B100	2B099	2B098	2B097	36	
4	11 10	37	3M010	3M009	3M008	3M007	3M006	3M005	3M004	2B104	2B103	2B102	2B101	2B096	37	PX 00, 01, 02
4	12 11	38	3M022	3M021	3M020	3M019	3M018	3M017	3M016	3M015	3M014	3M013	3M012		38	I CONTROLS
4	14 13	39	3L005	3L004	3L003	3L002	3L001	3M029	3M028	3M027	3M026	3M025	3M024	3M023	39	BITS 120-153
4	15 14	40										3L008	3L007	3L006	40	
5	2 1	41	2D039	2D038	2D037	2D036	2D035	2D034	2D033	2D032	2D031	2D030	2D029	2D028	41	I C REG
5	3 2	42	2C030	2C029	2C028	2D048	2D047	2D046	2D045	2D044	2D043	2D042	2D041	2D040	42	BITS 0-18, 2P
5	5 4	43	2C042	2C041	2C040	2C039	2C038	2C037	2C036	2C035	2C034	2C033	2C032	2C031	43	ICA REG
5	6 5	44	2C093	2C092	2C091	2C090	2C089	2C088	2C087	2C086	2C085	2C045	2C044	2C043	44	BITS 0-16, 1P
5	8 7	45	2D086	2D085	2C103	2C102	2C101	2C100	2C099	2C098	2C097	2C096	2C095	2C094	45	W REG BITS 0-17, 1P
5	9 8	46	2D100	2D097		2D095	2D094	2D093	2D092	2D091	2D090	2D089	2D088	2D087	46	
5	11 10	47	3L017	3L016	3L015	3L014	3L013	3L012	3L011	3L010	2D104	2D103	2D102	2D101	47	LGA 4, 2, 1, P
5	12 11	48			3L027	3L026	3L025	3L024	3L023	3L022	3L021	3L020	3L019	3L018	48	
5	14 13	49	3K020	3K019	3K018	3K017	3K016	3K015	3K014	3K013	3K012	3K011	3K010		49	I CONTROLS
5	15 14	50									3K024	3K023		3K021	50	
6	2 1	51		3J006	3J005	3J004	3J003	3J002	3J001		3K028	3K027	3K026	3K025	51	155-291
6	3 2	52	3J025	3J024	3J023	3J022	3J021		3J019	3J018	3J013	3J010	3J009	3J008	52	
6	5 4	53	3H008		3H006	3H005	3H004	3H003	3H002	3H001	3J029	3J028	3J027	3J026	53	
6	6 5	54	2C016	2C015	2C014	3H018	3H017	3H016	3H015	3H013	3H012	3H011	3H010	3H009	54	
6	8 7	55		3G004	3G003	3G002	3G001	3H029	3H028	3H027	2C021	2C020	2C019	2C018	55	
6	9 8	56	3G018	3G017	3G016	3G015	3G013	3G012	3G011	3G010	3G009	3J008	3G007	3G006	56	
6	11 10	57	3F012	3F011	3F010		3F008	3F007	3F006		3F004	3F003	3F002	3F001	57	
6	12 11	58	3F024	3F023	3F022	3F021	3F020	3F019	3F018	3F017	3F016	3F015	3F014	3F013	58	
6	14 13	59	2C001	2Q006	2Q005	2Q004		2Q002	2Q001	3F029	3F028		3F026	3F025	59	
6	15 14	60									2Q011	2C004	2C003	2C002	60	
7	2 1	61	2Q023	2Q021	2B008	2B007	2B006	2B005	2B002	2B001	2Q015	2Q014	2Q013	2Q012	61	L A CONTROLS
7	3 2	62	2N009	2N008	2N007	2N006	2N005	2N004	2N003	2N002	2N001	2C011	2Q025	2Q024	62	
7	5 4	63	2N021	2N020	2N019	2N018	2N017	2N016	2N015	2N014		2N012	2N011	2N010	63	
7	6 5	64	2L006	2A010	2A009	2A008	2A005	2L002	2L001	2N026	2N025	2N024	2N023	2N022	64	
7	8 7	65	2F001	2L026	2L025	2L019	2L018	2L017	2L016	2L015	2L014	2L013	2L008	2L007	65	1-104
7	9 8	66	2F013	2F012	2F011	2F010	2F009	2F008	2F007	2F006	2F005	2F004	2F003	2F002	66	
7	11 10	67	2J017			2J014	2J013	2J012	2J011	2J010	2J009	2F016	2F015	2F014	67	
7	12 11	68	2F030	2F029	2F028	2J026	2J025	2J024	2J023	2J022	2J021		2J019	2J018	68	
7	14 13	69	2F042	2F041	2F040	2F039	2F038	2F037	2F036	2F035	2F034	2F033	2F032	2F031	69	STAR
7	15 14	70									2F046	2F045	2F044	2F043	70	
8	2 1	71													71	
8	3 2	72													72	
8	5 4	73													73	
8	6 5	74													74	
8	8 7	75													75	
8	9 8	76													76	
8	11 10	77													77	
8	12 11	78													78	
8	14 13	79													79	
8	15 14	80					CD 1						SIGMA		80	

PRIMARY SCAN
A RING (PA) = 6 STAGES
B RING (PB) = 6 STAGES

SECONDARY SCAN
A RING (SA) = 4 STAGES
B RING (SB) = 4 STAGES

PRIMARY SAMPLE (PRI SMP) = 6(PB-1) + PA
SECONDARY SAMPLE (SEC SMP) = 4(SB-1) + SA

FIGURE 3.4.1. CPU SCAN CARD
IMAGE - CARD 1

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4-25/4-26

M3-04-3

INDICATORS

PRI SMP	SEC SMP	COL	ROW 9	8	7	6	5	4	3	2	1	0	11	12	COL	COMMENTS
9	2 | 1	1	2P040	2P039	2P038	2P037	2P036	2P035	2P034	2P033	2P032	2P031	2P030	2P029	1	L A LEVEL 1
9	3 | 2	2	2P052	2P051	2P050	2P049	2P048	2P047	2P046	2P045	2P044	2P043	2P042	2P041	2	DATA FIELD
9	5 | 4	3	2P064	2P063	2P062	2P061	2P060	2P059	2P058	2P057	2P056	2P055	2P054	2P053	3	BITS 0-13,
9	6 | 5	4	2P076	2P075	2P074	2P073	2P072	2P071	2P070	2P069	2P068	2P067	2P066	2P065	4	10P & 2R
9	8 | 7	5	2P088	2P087	2P086	2P085	2P084	2P083	2P082	2P081	2P080	2P079	2P078	2P077	5	
9	9 | 8	6	2P100	2P099	2P098	2P097	2P096	2P095	2P094	2P093	2P092	2P091	2P090	2P089	6	
9	11 | 10	7	2Q059	2Q058	2Q057	2Q056	2Q055	2Q054	2Q053	2Q061	2P104	2P103	2P102	2P101	7	
9	12 | 11	8	2Q087	2Q086	2Q085	2Q084	2Q083	2Q037	2Q036	2Q035	2Q034	2Q033	2Q032	2Q060	8	
9	14 | 13	9	2Q099	2Q098	2Q097	2Q096	2Q095	2Q094	2Q093	2Q092	2Q091	2Q090	2Q089	2Q088	9	I C
9	15 | 14	10									2Q103	2Q100	2Q102	2Q101	10	FIELD
10	2 | 1	11	2M040	2M039	2M038	2M037	2M036	2M035	2M034	2M033	2M032	2M031	2M030	2M029	11	L A LEVEL 2
10	3 | 2	12	2M052	2M051	2M050	2M049	2M048	2M047	2M046	2M045	2M044	2M043	2M042	2M041	12	DATA FIELD
10	5 | 4	13	2M064	2M063	2M062	2M061	2M060	2M059	2M058	2M057	2M056	2M055	2M054	2M053	13	BITS 0-63,
10	6 | 5	14	2M076	2M075	2M074	2M073	2M072	2M071	2M070	2M069	2M068	2M067	2M066	2M065	14	10P & 2R
10	8 | 7	15	2M088	2M087	2M086	2M085	2M084	2M083	2M082	2M081	2M080	2M079	2M078	2M077	15	
10	9 | 8	16	2M100	2M099	2M098	2M097	2M096	2M095	2M094	2M093	2M092	2M091	2M090	2M089	16	
10	11 | 10	17	2N059	2N058	2N057	2N056	2N055	2N054	2N053	2N061	2M104	2M103	2M102	2M101	17	
10	12 | 11	18	2N087	2N086	2N085	2N084	2N083	2N037	2N036	2N035	2N034	2N033	2N032	2N060	18	
10	14 | 13	19	2N099	2N098	2N097	2N096	2N095	2N094	2N093	2N092	2N091	2N090	2N089	2N088	19	I C
10	15 | 14	20									2N103	2N100	2N102	2N101	20	FIELD
11	2 | 1	21	2K040	2K039	2K038	2K037	2K036	2K035	2K034	2K033	2K032	2K031	2K030	2K029	21	L A LEVEL 3
11	3 | 2	22	2K052	2K051	2K050	2K049	2K048	2K047	2K046	2K045	2K044	2K043	2K042	2K041	22	DATA FIELD
11	5 | 4	23	2K064	2K063	2K062	2K061	2K060	2K059	2K058	2K057	2K056	2K055	2K054	2K053	23	BITS 0-63,
11	6 | 5	24	2K076	2K075	2K074	2K073	2K072	2K071	2K070	2K069	2K068	2K067	2K066	2K065	24	10P & 2R
11	8 | 7	25	2K088	2K087	2K086	2K085	2K084	2K083	2K082	2K081	2K080	2K079	2K078	2K077	25	
11	9 | 8	26	2K100	2K099	2K098	2K097	2K096	2K095	2K094	2K093	2K092	2K091	2K090	2K089	26	
11	11 | 10	27	2L059	2L058	2L057	2L056	2L055	2L054	2L053	2L061	2K104	2K103	2K102	2K101	27	
11	12 | 11	28	2L087	2L086	2L085	2L084	2L083	2L037	2L036	2L035	2L034	2L033	2L032	2L060	28	
11	14 | 13	29	2L099	2L098	2L097	2L096	2L095	2L094	2L093	2L092	2L091	2L090	2L089	2L088	29	IC
11	15 | 14	30									2L103	2L100	2L102	2L101	30	FIELD
12	2 | 1	31	2H040	2H039	2H038	2H037	2H036	2H035	2H034	2H033	2H032	2H031	2H030	2H029	31	L A LEVEL 4
12	3 | 2	32	2H052	2H051	2H050	2H049	2H048	2H047	2H046	2H045	2H044	2H043	2H042	2H041	32	DATA FIELD
12	5 | 4	33	2H064	2H063	2H062	2H061	2H060	2H059	2H058	2H057	2H056	2H055	2H054	2H053	33	BITS 0-63,
12	6 | 5	34	2H076	2H075	2H074	2H073	2H072	2H071	2H070	2H069	2H068	2H067	2H066	2H065	34	10P &2R
12	8 | 7	35	2H088	2H087	2H086	2H085	2H084	2H083	2H082	2H081	2H080	2H079	2H078	2H077	35	
12	9 | 8	36	2H100	2H099	2H098	2H097	2H096	2H095	2H094	2H093	2H092	2H091	2H090	2H089	36	
12	11 | 10	37	2J059	2J058	2J057	2J056	2J055	2J054	2J053	2J061	2H104	2H103	2H102	2H101	37	
12	12 | 11	38	2J087	2J086	2J085	2J084	2J083	2J037	2J036	2J035	2J034	2J033	2J032	2J060	38	
12	14 | 13	39	2J099	2J098	2J097	2J096	2J095	2J094	2J093	2J092	2J091	2J090	2J089	2J088	39	I C
12	15 | 14	40									2J103	2J100	2J102	2J101	40	FIELD
13	2 | 1	41	2N040	2Q050	2Q049	2Q048	2Q047	2Q046	2Q045	2Q044	2Q043	2Q042	2Q041	2Q040	41	LEVEL 1 - 4
13	3 | 2	42	2L041	2L040	2N050	2N049	2N048	2N047	2N046	2N045	2N044	2N043	2N042	2N041	42	OP CODE
13	5 | 4	43	2J042	2J041	2J040	2L050	2L049	2L048	2L047	2L046	2L045	2L044	2L043	2L042	43	
13	6 | 5	44	2Q069	2Q068	2Q067	2Q066	2J050	2J049	2J048	2J047	2J046	2J045	2J044	2J043	44	
13	8 | 7	45	2N066	2Q080	2Q079	2Q078	2Q077	2Q076	2Q075	2Q074	2Q073	2Q072	2Q071	2Q070	45	LEVEL 1 - 4
13	9 | 8	46	2N078	2N077	2N076	2N075	2N074	2N073	2N072	2N071	2N070	2N069	2N068	2N067	46	INDICATOR FIELD
13	11 | 10	47	2L075	2L074	2L073	2L072	2L071	2L070	2L069	2L068	2L067	2L066	2N080	2N079	47	
13	12 | 11	48	2J072	2J071	2J070	2J069	2J068	2J067	2J066	2L080	2L079	2L078	2L077	2L076	48	
13	14 | 13	49	1F075	1F074	1F073		2J080	2J079	2J078	2J077	2J076	2J075	2J074	2J073	49	
13	15 | 14	50									1F079	1F078	1F077	1F076	50	
14	2 | 1	51	1E043	1E042	1E041	1E040	1E038	1E037	1E036	1E035	1E034	1E033	1E032	1E031	51	C REG
14	3 | 2	52	1E057	1E056	1E055	1E054	1E053	1E052	1E051	1E050	1E048	1E047	1E046	1E045	52	BITS 0-63,
14	5 | 4	53	1E071	1E070	1E069	1E068	1E066	1E065	1E064	1E063	1E062	1E061	1E060	1E059	53	10P
14	6 | 5	54	1E084	1E083	1E082	1E081	1E080	1E079	1E078	1E077	1E075	1E074	1E073	1E072	54	
14	8 | 7	55	1E098	1E097	1E096	1E095	1E093	1E092	1E091	1E090	1E089	1E088	1E087	1E086	55	
14	9 | 8	56	1E094	1E085	1E076	1E067	1E058	1E049	1E044	1E039	1E103	1E102	1E101	1E100	56	
14	11 | 10	57	1F060	1F059	1F058	1F057	1F056	1F055	1F048	1F047	1F046	1F045	1E104	1E099	57	
14	12 | 11	58	1F098	1F097	1F096	1F095	1F070	1F069	1F068	1F067	1F066	1F065	1F064	1F061	58	
14	14 | 13	59	1F009	1F008	1F007	1F006	1F005	1F004	1F003	1F002	1F001	1F103	1F102	1F101	59	
14	15 | 14	60										1F012		1F010	60	
15	2 | 1	61	1D043	1D042	1D041	1D040	1D038	1D037	1D036	1D035	1D034	1D033	1D032	1D031	61	
15	3 | 2	62	1D057	1D056	1D055	1D054	1D053	1D052	1D051	1D050	1D048	1D047	1D046	1D045	62	D REG
15	5 | 4	63	1D071	1D070	1D069	1D068	1D066	1D065	1D064	1D063	1D062	1D061	1D060	1D059	63	BITS 0-63,10P
15	6 | 5	64	1D084	1D083	1D082	1D081	1D080	1D079	1D078	1D077	1D075	1D074	1D073	1D072	64	
15	8 | 7	65	1D098	1D097	1D096	1D095	1D093	1D092	1D091	1D090	1D089	1D088	1D087	1D086	65	
15	9 | 8	66	1D094	1D085	1D076	1D067	1D058	1D049	1D044	1D039	1D103	1D102	1D101	1D100	66	
15	11 | 10	67	1F023	1F022	1F021	1F020	1F019	1F018	1F017	1F016	1F015	1F014	1D104	1D099	67	
15	12 | 11	68	2F087	2F086	2F085	2F084	2F083	1D003	1D002	1D001	1F027	1F026	1F025	1F024	68	
15	14 | 13	69	2F099	2F098	2F097	2F096	2F095	2F094	2F093	2F092	2F091	2F090	2F089	2F088	69	I C BUFFER
15	15 | 14	70									2F103	2F100	2F102	2F101	70	REG
16	2 | 1	71													71	
16	3 | 2	72													72	
16	5 | 4	73													73	
16	6 | 5	74													74	
16	8 | 7	75													75	
16	9 | 8	76													76	
16	11 | 10	77													77	
16	12 | 11	78													78	
16	14 | 13	79													79	
16	15 | 14	80				CD. 2							SIGMA		80	

PRIMARY SCAN
A RING (PA) = 4 STAGES
B RING (PB) = 4 STAGES

SECONDARY SCAN
A RING (SA) = 4 STAGES
B RING (SB) = 4 STAGES

PRIMARY SAMPLE (PRI SMP) = 6(PB-1) + PA
SECONDARY SAMPLE (SEC SMP) = 4(SB-1) + SA

FIGURE 3.4.2. CPU SCAN CARD
IMAGE - CARD 2

PRI SMP	SEC SMP	COL	ROW 9	8	7	6	5	4	3	2	1	0	11	12	COL	COMMENTS
17	2 | 1	1	1Q013	1Q012	1Q011	1Q010	1Q009	1Q008	1Q007	1Q006	1Q005	1Q004	1Q003	1Q002	1	
17	3 | 2	2	1Q025	1Q024	1Q023	1Q022	1Q021	1Q020	1Q019	1Q018	1Q017	1Q016	1Q015	1Q014	2	F REG
17	5 | 4	3	1Q037	1Q036	1Q035	1Q034	1Q033	1Q032	1Q031	1Q030	1Q029	1Q028	1Q027	1Q026	3	BITS 0-101
17	6 | 5	4	1Q049	1Q048	1Q047	1Q046	1Q045	1Q044	1Q043	1Q042	1Q041	1Q040	1Q039	1Q038	4	
17	8 | 7	5	1Q061	1Q060	1Q059	1Q058	1Q057	1Q056	1Q055	1Q054	1Q053	1Q052	1Q051	1Q050	5	
17	9 | 8	6	1Q073	1Q072	1Q071	1Q070	1Q069	1Q068	1Q067	1Q066	1Q065	1Q064	1Q063	1Q062	6	
17	11 | 10	7	1Q085	1Q084	1Q083	1Q082	1Q081	1Q080	1Q079	1Q078	1Q077	1Q076	1Q075	1Q074	7	
17	12 | 11	8	1Q097	1Q096	1Q095	1Q094	1Q093	1Q092	1Q091	1Q090	1Q089	1Q088	1Q087	1Q086	8	
17	14 | 13	9	1M002	1M001	1L048	1L049	1L046	1L045	1Q103	1Q102	1Q101	1Q100	1Q099	1Q098	9	
17	15 | 14	10									1M006	1M005	1M004	1M003	10	
18	2 | 1	11	1P012	1P011	1P010	1P009	1P008	1P007	1P006	1P005	1P004	1P003	1P002	1P001	11	
18	3 | 2	12	1P024	1P023	1P022	1P021	1P020	1P019	1P018	1P017	1P016	1P015	1P014	1P013	12	
18	5 | 4	13	1P036	1P035	1P034	1P033	1P032	1P031	1P030	1P029	1P028	1P027	1P026	1P025	13	ADDER
18	6 | 5	14	1P048	1P047	1P046	1P045	1P044	1P043	1P042	1P041	1P040	1P039	1P038	1P037	14	BITS P, 0-102
18	8 | 7	15	1P060	1P059	1P058	1P057	1P056	1P055	1P054	1P053	1P052	1P051	1P050	1P049	15	
18	9 | 8	16	1P072	1P071	1P070	1P069	1P068	1P067	1P066	1P065	1P064	1P063	1P062	1P061	16	
18	11 | 10	17	1P084	1P083	1P082	1P081	1P080	1P079	1P078	1P077	1P076	1P075	1P074	1P073	17	
18	12 | 11	18	1P096	1P095	1P094	1P093	1P092	1P091	1P090	1P089	1P088	1P087	1P086	1P085	18	
18	14 | 13	19	1L054	1L053	1L052	1L051	1P104	1P103	1P102	1P101	1P100	1P099	1P098	1P097	19	
18	15 | 14	20									1L058	1L057	1L056	1L055	20	
19	2 | 1	21	1N055	1N054	1N053	1N052	1N051	1N050	1N049	1N048	1N047	1N046	1N045	1N044	21	SUM REG
19	3 | 2	22	1N067	1N066	1N065	1N064	1N063	1N062	1N061	1N060	1N059	1N058	1N057	1N056	22	BITS 1-61
19	5 | 4	23	1N079	1N078	1N077	1N076	1N075	1N074	1N073	1N072	1N071	1N070	1N069	1N068	23	
19	6 | 5	24	1N091	1N090	1N089	1N088	1N087	1N086	1N085	1N084	1N083	1N082	1N081	1N080	24	
19	8 | 7	25	1N103	1N102	1N101	1N100	1N099	1N098	1N097	1N096	1N095	1N094	1N093	1N092	25	
19	9 | 8	26	1L071	1L070	1L069	1L068	1L067	1L066	1L065	1L064	1L063	1L062	1L061	1N104	26	
19	11 | 10	27	1L087	1L086	1L085	1L082	1L081	1L080	1L079	1L078	1L077	1L076	1L075	1L072	27	
19	12 | 11	28	1L099	1L098	1L097	1L096	1L095	1L094	1L093	1L092	1L091	1L090	1L089	1L088	28	
19	14 | 13	29	1M013	1M012	1M011	1M010	1M009	1M008	1M007	1L104	1L103	1L102	1L101	1L100	29	
19	15 | 14	30									1M017	1M016	1M015	1M014	30	
20	2 | 1	31	1M055	1M054	1M053	1M052	1M051	1M050	1M049	1M048	1M047	1M046	1M045	1M044	31	CARRY REG
20	3 | 2	32	1M067	1M066	1M065	1M064	1M063	1M062	1M061	1M060	1M059	1M058	1M057	1M056	32	BITS 1-61
20	5 | 4	33	1M079	1M078	1M077	1M076	1M075	1M074	1M073	1M072	1M071	1M070	1M069	1M068	33	
20	6 | 5	34	1M091	1M090	1M089	1M088	1M087	1M086	1M085	1M084	1M083	1M082	1M081	1M080	34	
20	8 | 7	35	1M103	1M102	1M101	1M100	1M099	1M098	1M097	1M096	1M095	1M094	1M093	1M092	35	
20	9 | 8	36	1C043	1C042	1C041	1C040	1C039	1C038	1C037	1C036	1C035	1C034	1C033	1M104	36	
20	11 | 10	37	1C055	1C054	1C053	1C052	1C051	1C050	1C049	1C048	1C047	1C046	1C045	1C044	37	SAU EXECUTE
20	12 | 11	38	1C067	1C066	1C065	1C064	1C063	1C062	1C061	1C060	1C059	1C058	1C057	1C056	38	REG
20	14 | 13	39	1K020	1M026	1K019	1M024	1M023	1M022	1M021	1M020	1M019	1M018	1C069	1C068	39	
20	15 | 14	40									1M031	1M030	1M029	1K021	40	
21	2 | 1	41	1H043	1H042	1H041	1H040	1H038	1H037	1H036	1H035	1H034	1H033	1H032	1H031	41	A REG
21	3 | 2	42	1H057	1H056	1H055	1H054	1H053	1H052	1H051	1H050	1H048	1H047	1H046	1H045	42	BITS 0-63,
21	5 | 4	43	1H071	1H070	1H069	1H068	1H066	1H065	1H064	1H063	1H062	1H061	1H060	1H059	43	10P
21	6 | 5	44	1H084	1H083	1H082	1H081	1H080	1H079	1H078	1H077	1H075	1H074	1H073	1H072	44	
21	8 | 7	45	1H098	1H097	1H096	1H095	1H093	1H092	1H091	1H090	1H089	1H088	1H087	1H086	45	
21	9 | 8	46	1H094	1H085	1H076	1H067	1H058	1H049	1H044	1H039	1H103	1H102	1H101	1H100	46	
21	11 | 10	47	1J056	1J055	1J052	1J051	1J050	1J049	1J048	1J047	1J046	1J045	1H104	1H099	47	
21	12 | 11	48	1J070	1J069	1J068	1J067	1J066	1J065	1J064	1J061	1J060	1J059	1J058	1J057	48	
21	14 | 13	49	1J075	1J074	1J073	1J103	1J102	1J101	1J098	1J097	1J096	1J095	1J094	1J093	49	
21	15 | 14	50									1J079	1J078	1J077	1J076	50	
22	2 | 1	51	1G043	1G042	1G041	1G040	1G038	1G037	1G036	1G035	1G034	1G033	1G032	1G031	51	B REG
22	3 | 2	52	1G057	1G056	1G055	1G054	1G053	1G052	1G051	1G050	1G048	1G047	1G046	1G045	52	BITS 0-63,
22	5 | 4	53	1G071	1G070	1G069	1G068	1G066	1G065	1G064	1G063	1G062	1G061	1G060	1G059	53	10P
22	6 | 5	54	1G084	1G083	1G082	1G081	1G080	1G079	1G078	1G077	1G075	1G074	1G073	1G072	54	
22	8 | 7	55	1G098	1G097	1G096	1G095	1G093	1G092	1G091	1G090	1G089	1G088	1G087	1G086	55	
22	9 | 8	56	1G094	1G085	1G076	1G067	1G058	1G049	1G044	1G039	1G103	1G102	1G101	1G100	56	
22	11 | 10	57	1C096	1C095	1C094	1C093	1C092	1C091	1C090	1C089	1C088	1C087	1G104	1G099	57	
22	12 | 11	58	1B092	1B091	1B090	1B089	1B088	1B087	1C102	1C101	1C100	1C099	1C098	1C097	58	PRE LATCH 1
22	14 | 13	59		1D004	1B102	1B101	1B100	1B099	1B098	1B097	1B096	1B095	1B094	1B093	59	PRE LATCH 2
22	15 | 14	60										1D008	1D007	1D006	60	
23	2 | 1	61	1C084	1C083	1C082	1C081	1C080	1J088	1J087	1J086	1J085	1J084	1J083	1J082	61	
23	3 | 2	62	1D019		1D017	1D016	1D015	1D014		1D012	1D011	1D010	1H027	1H025	62	
23	5 | 4	63	1B004	1B003	1B002	1B001	1D027	1D026	1D025	1D024	1D023		1D021	1D020	63	
23	6 | 5	64	1K025	1K024	1K023	1B013	1B012	1B011	1K022	1B009	1B008	1B007	1B006	1B005	64	
23	8 | 7	65	1M032	1B027	1B026	1B025	1B024	1B023	1B022	1K030	1K029	1K028	1K027	1K026	65	
23	9 | 8	66	1L002	1L001	1M042	1M041	1M040	1M039	1M038	1M037	1M036	1M035	1M034	1M033	66	
23	11 | 10	67	1L014	1L013	1L012	1L011	1L010	1L009	1L008	1L007	1L006	1L005	1L004	1L003	67	
23	12 | 11	68	1L026	1L025	1L024	1L023	1L022	1L021	1L020	1L019	1L018	1L017	1L016	1L015	68	
23	14 | 13	69	1L038	1K018	1L036	1L035	1L034	1L033	1L032	1L031	1L030	1K017	1L028	1L027	69	
23	15 | 14	70									1L042	1L041	1L040	1L039	70	
24	2 | 1	71													71	
24	3 | 2	72													72	
24	5 | 4	73													73	
24	6 | 5	74													74	
24	8 | 7	75													75	
24	9 | 8	76													76	
24	11 | 10	77													77	
24	12 | 11	78													78	
24	14 | 13	79													79	
24	15 | 14	80			CD 3								SIGMA		80	

PRIMARY SCAN
A RING (PA) = 4 STAGES
B RING (PB) = 4 STAGES

SECONDARY SCAN
A RING (SA) = 4 STAGES
B RING (SB) = 4 STAGES

PRIMARY SAMPLE (PRI SMP) = 6(PB-1) + PA
SECONDARY SAMPLE (SEC SMP) = 4(SB-1) + SA

FIGURE 3.4.3. CPU SCAN CARD
IMAGE - CARD 3

PRI SMP	SEC SMP	COL	ROW 9	8	7	6	5	4	3	2	1	0	11	12	COL	COMMENTS
25	2 | 1	1	1B044	1B043	1B040	1B039	1B038	1B037	1B036	1B035	1B034	1B033	1B032	1B031	1	
25	3 | 2	2	1B056	1B055	1B054	1B053	1B052	1B051	1B050	1B049	1B048	1B047	1B046	1B045	2	
25	5 | 4	3	1B078	1B076	1B075	1B071	1B070	1B068	1B067	1B066	1B060	1B059	1B058	1B057	3	
25	6 | 5	4	1A069	1A068	1A067	1A066	2J063	2L063	2N063	2Q063	2J062	2L062	2N062	2Q062	4	
25	8 | 7	5					1A078	1A077	1A075	1A074	1A073	1A072	1A071	1A070	5	
25	9 | 8	6													6	
25	11 | 10	7													7	
25	12 | 11	8													8	
25	14 | 13	9													9	
25	15 | 14	10													10	
26	2 | 1	11	1A054	1A053	1A052	1A051	1A050	1A049	1A048	1A047	1A046	1A045	1A044	1A043	11	
26	3 | 2	12	1A058	1A040	1A039	1A038	1A037	1A036	1A035	1A034	1A033	1A032	1A031	1A055	12	
26	5 | 4	13	2G040	2G039	2G038	2G037	2G036	2G035	2G034	2G033		1F094	1F093	1A059	13	
26	6 | 5	14	2G052	2G051	2G050	2G049	2G048	2G047	2G046	2G045	2G044	2G043	2G042	2G041	14	IND REG BITS 0-19
26	8 | 7	15					2F025	2F024	2F023	2F022	2F021	2F020	2F019	2F018	15	
26	9 | 8	16													16	
26	11 | 10	17													17	
26	12 | 11	18													18	
26	14 | 13	19													19	
26	15 | 14	20													20	
27	2 | 1	21	2G064	2G063	2G062	2G061	2G060	2G059	2G058	2G057	2G056	2G055	2G054	2G053	21	IND REG
27	3 | 2	22	2G076	2G075	2G074	2G073	2G072	2G071	2G070	2G069	2G068	2G067	2G066	2G065	22	BITS 20-63
27	5 | 4	23	2G088	2G087	2G086	2G085	2G084	2G083	2G082	2G081	2G080	2G079	2G078	2G077	23	
27	6 | 5	24	2G004	2G003	2G002	2G001	2G096	2G095	2G094	2G093	2G092	2G091	2G090	2G089	24	
27	8 | 7	25					2G013	2G012	2G010	2G009	2G008	2G007	2G006	2G005	25	
27	9 | 8	26													26	
27	11 | 10	27													27	
27	12 | 11	28													28	
27	14 | 13	29													29	
27	15 | 14	30													30	
28	2 | 1	31	2F064	2F063	2F062	2F061	2F060	2F059	2F058	2F057	2F056	2F055	2F054	2F053	31	MASK REG
28	3 | 2	32	2F076	2F075	2F074	2F073	2F072	2F071	2F070	2F069	2F068	2F067	2F066	2F065	32	BITS 20-47,
28	5 | 4	33	2E052	2E051	2E050	2E049	2F052	2F051	2F050	2F049	2F080	2F079	2F078	2F077	33	4P
28	6 | 5	34	2G017	2G016	2G015	2J038	2L038	2N038	2Q038	2D055	2D054	2E055	2E054	2E053	34	
28	8 | 7	35						1H023	2G024	2G023	2G022	2G021	2G019	2G018	35	
28	9 | 8	36													36	
28	11 | 10	37													37	
28	12 | 11	38													38	
28	14 | 13	39													39	
28	15 | 14	40													40	
29	2 | 1	41	1K044	1K043	1K042	1K041	1K040	1K039	1K038	1K037	1K036	1K035	1K034	1K033	41	
29	3 | 2	42	1K056	1K055	1K054	1K053	1K052	1K051	1K050	1K049	1K048	1K047	1K046	1K045	42	STORE REG
29	5 | 4	43	1K068	1K067	1K066	1K065	1K064	1K063	1K062	1K061	1K060	1K059	1K058	1K057	43	0-55
29	6 | 5	44	1K080	1K079	1K078	1K077	1K076	1K075	1K074	1K073	1K072	1K071	1K070	1K069	44	
29	8 | 7	45					1K088	1K087	1K086	1K085	1K084	1K083	1K082	1K081	45	
29	9 | 8	46													46	
29	11 | 10	47													47	
29	12 | 11	48													48	
29	14 | 13	49													49	
29	15 | 14	50													50	
30	2 | 1	51	1K100	1K099	1K098	1K097	1K096	1K095	1K094	1K093	1K092	1K091	1K090	1K089	51	STORE REG 56-63
30	3 | 2	52	2E008	2E007	2E006	2E005	2E004	2E003	2E002	2E001	1K104	1K103	1K102	1K101	52	LAAR 1
30	5 | 4	53	2D001	2E019	2E018	2E017	2E016	2E015	2E014	2E013	2E012	2E011	2E010	2E009	53	
30	6 | 5	54	2D013	2D012	2D011	2D010	2D009	2D008	2D007	2D006	2D005	2D004	2D003	2D002	54	LAAR 2
30	8 | 7	55					2C054	2C009	2D019	2D018	2D017	2D016	2D015	2D014	55	
30	9 | 8	56													56	
30	11 | 10	57													57	
30	12 | 11	58													58	
30	14 | 13	59													59	
30	15 | 14	60													60	
31	2 | 1	61	2C069	2C068	2C067	2C066	2C064	2C063	2C062	2C061	2C060	2C059	2C058	2C057	61	ULB REG
31	3 | 2	62	2C055	2C053	2C052	2C077	2C074	2C065	2C076	2C075	2C073	2C072	2C071	2C070	62	
31	5 | 4	63	2D069	2D068	2D067	2D066	2D064	2D063	2D062	2D061	2D060	2D059	2D058	2D057	63	
31	6 | 5	64	2A012	2A011	2D078	2D075	2D070	2D065	2D077	2D076	2D074	2D073	2D072	2D071	64	
31	8 | 7	65					2A020	2A019	2A018	2A017	2A016		2A014	2A013	65	
31	9 | 8	66													66	
31	11 | 10	67													67	
31	12 | 11	68													68	
31	14 | 13	69													69	
31	15 | 14	70													70	
32	2 | 1	71													71	
32	3 | 2	72													72	
32	5 | 4	73													73	
32	6 | 5	74													74	
32	8 | 7	75													75	
32	9 | 8	76													76	
32	11 | 10	77													77	
32	12 | 11	78													78	
32	14 | 13	79													79	
32	15 | 14	80		CD 4									SIGMA		80	

PRIMARY SCAN
A RING (PA) = 6 STAGES
B RING (PB) = 6 STAGES

SECONDARY SCAN
A RING (SA) = 4 STAGES
B RING (SB) = 4 STAGES

PRIMARY SAMPLE (PRI SMP) = 6 (PB-1) + PA
SECONDARY SAMPLE (SEC SMP) = 4 (SB-1) + SA

FIGURE 3.4.4. CPU SCAN CARD
IMAGE - CARD 4

DESCRIPTION

This category contains a brief functional description of each CPU control switch on the 7101 CE console. These switches are listed under the following headings:

a. 7101 CE Console Level Switches

b. 7101 CE Console Pulse Switches

c. 7101 CE Console Marginal Check Controls

7101 CE CONSOLE LEVEL SWITCHES

The level switches on the 7101 CE console are shown in block diagram form on systems page 73.03.01.1. These switches are listed according to sequential console co-ordinates.

A3B29-A3B60 and A3D29-A3D60 PANEL KEYS – These 64 2-position switches are used as a data source when executing a single-store or a consecutive-store operation, as an instruction source when executing an enter-instruction operation, and as a data source when in the maintenance mode and executing a fetch-type instruction that selects address 4.

The output of the PANEL KEYS (a 0 bit if the switch is in the normal position and a 1 bit if it is in the down position) can be modified by the setting of the 3-position (normal, up, and down) PANEL KEY SET 10 and PANEL KEY SET 01 switches. If both of these switches are in the up position, the output of the PANEL KEYS will be all 0's regardless of the PANEL KEYS setting. If both of these switches are in the down position, the output of the PANEL KEYS will be all 1's regardless of the PANEL KEYS setting. If the PANEL KEY SET 01 switch is in the down position and the PANEL KEY SET 10 switch is in either the normal or up position, the PANEL KEYS data will be OR'ed with a 010101----01 pattern. If the PANEL KEY SET 10 switch is in the down position and the PANEL KEY SET 01 switch is in either the normal or up position, the PANEL KEYS data will be OR'ed with a 101010----10 pattern. If both of these switches are in the normal position, the PANEL KEYS data will not be modified.

A3F31-A3F48, ADDRESS KEYS 0-17 - The contents of these 2-position switches are gated (a 0 bit if the switch is in the normal position and a 1 bit if it is in the down position) into the W register when the DISPLAY or STORE pushbutton is depressed. The W register is then used to

select the storage address from which data will be fetched for display in the X and Y registers or into which data will be stored from the PANEL KEYS.

A3F49 MAINT MODE - When set (down), this switch places the CPU in the maintenance mode to condition the Allow Error Inject (ALLOW ER INJ) level switch and the console pushbutton switches for maintenance operations. In addition, when this switch is set, all references to storage address 4 are interpreted as a fetch of the information from the PANEL KEYS.

A3F50, TIME CLK (DISABLE) - When set (down), this switch inhibits the stepping of the time clock and interval timer.

A3F51 IRPT (DISABLE) - When set (down), this switch inhibits the execution of all interrupts that normally result from the setting of indicator register bits. This switch also inhibits the interrupt that is initated by the Force Enable on Execute instructions.

A3F52-A3F55, LA 1, 2, 3, 4 - When set (down), these switches set the disconnect tag for the associated level of lookahead. When this tag is set, the associated level of lookahead is bypassed for all lookahead loading operations.

A3F56, RPT INST - When set (down), this switch enables the CPU to alternately gate the contents of the PANEL KEYS into the 1Y and 2Y registers. Execution of the repeat-instruction operation, which can be performed only in the maintenance mode, is initiated by depressing the START (Program) pushbutton (A3D24). When depressed, this pushbutton, instead of processing the sequential instructions of the stored program, causes the CPU to continually execute the full- or half-word instructions that were preset into the PANEL KEYS. If a branch instruction was preset into the PANEL KEYS, the instruction or instructions contained in the branch location will be executed before the instruction in the PANEL KEYS is repeated.

A3F57, TC TEST - When set (down), this switch allows the time clock and the interval timer to be stepped normally when the CPU is stopped. This switch is operative only if the TIME CLK switch is in the cleared (normal) position.

A3A58, MULTI OP - When set (down), this switch has the same effect as depressing the SINGLE OP pushbutton (A3B26) at a 10-cps rate. This switch is operative only in the maintenance mode.

A3F59, INH SCAN AND A3F60, ERR STOP - These two 3-position (normal, up, down) switches function together to determine what action will be taken when a CPU error occurs. The effect of the switch settings on CPU operation is noted below:

Condition	INH SCAN	ERR STOP	Effect
1.	Normal	Normal	When an error occurs, the CPU clock is stopped and a scan operation is performed. After the scan operation is completed, the CPU clock is automatically restarted to reinitiate normal CPU operation.
2.	Down	Normal	Scanning is suppressed and the CPU clock is not stopped on error.
3.	Up	Normal	Same as condition 1 except that single ECC errors are ignored.
4.	Normal	Down	Same as condition 1 except that CPU operation is not resumed after the scan.
5.	Down	Down	CPU operation stops on any error; scanning does not occur.
6.	Up	Down	On all errors except single ECC errors, the CPU clock is stopped and a scan operation is performed. CPU operation is not resumed after the scan.
7.	Normal	Up	Same as condition 6.
8.	Down	Up	CPU stops on all errors but single ECC errors; scanning does not occur.
9.	Up	Up	Same as condition 6.

A3F61, READ (INDEX STG TEST) - When set (down), this switch conditions CPU circuits so that a continuous read test can be performed on the selected index storage register or registers. Execution of this test, which can be performed only in the maintenance mode, is initiated by the START XS TEST (A3A16) pushbutton. When depressed, this pushbutton causes the CPU to generate a continuous series of index storage read test cycles.

The index storage register to be tested is selected by the W register which was initially preset from the ADDRESS KEYS upon the execution of a display or store operation. If the Address Advance (ADR ADV) switch is set, the contents of the W register will be increased by 1 at the end of each index storage read test cycle so that consecutive index storage registers can be tested sequentially.

The information read out of the selected index storage register is parity-checked by the I checker. If an error is detected, the error signal will set the index storage error trigger. In addition, if the Error Stop (ERR STOP) switch is set, the error signal will terminate the read test.

A3F62, WRITE (INDEX STG TEST) - When set (down), this switch conditions CPU circuits so that a continuous read, clear, and write test can be performed on the selected index storage register or registers. Execution of this test, which can be performed only in the maintenance mode, is initiated by the START XS TEST (A3A16) pushbutton. When depressed, this pushbutton causes the CPU to generate a continuous series of index storage read, clear, and write test cycles. These test cycles respectively read out the information in the selected storage index and rewrite the original information (read out into the X register) into the selected index storage register. The index storage register to be tested is selected by the W register which was initially preset from the ADDRESS KEYS upon the execution of a display or store operation. If the Address Advance (ADR ADV) switch is set, the contents of the W register will be increased by 1 at the end of each index storage read, clear, and write test cycle sequence so that consecutive index storage registers can be tested sequentially.

The information read out of the selected index storage register is parity-checked by the I checker. If an error is detected, the error signal will set the index storage error trigger. In addition, if the Error Stop (ERR STOP) switch is set, the error signal will terminate the test.

A3F63, ADR ADV (INDEX STG TEST) - When set (down), this switch causes a 1 to be added to the W register at the end of each test sequence when either the index storage read or index storage write test is executed.

A3F64, ERR STOP (INDEX STG TEST) - When set (down), this switch routes the index storage read or index storage write parity error signal to terminate the test. The test can be reinitiated by resetting the index storage error trigger and depressing the START XS TEST (A3A16) pushbutton.

A3F65, PANEL KEY SET 01; and A3F66, PANEL KEY SET 10 - These two 3-position (normal, up, down) switches function together to modify the output of the PANEL KEYS during the execution of single-store, consecutive-store, and enter-instruction operations and during the maintenance mode execution of fetch-type instructions that select address 4. If both of these

switches are in the up position, the output of the PANEL KEYS will be all 0's regardless of the PANEL KEY setting. If both of these switches are in the down position, the output of the PANEL KEYS will be all 1's regardless of the PANEL KEY setting. If the PANEL KEY SET 01 switch is in the down position and the PANEL KEY SET 10 switch is in either the normal or up position, the PANEL KEYS data will be OR'ed with a 010101----01 pattern. If the PANEL KEY SET 10 switch is in the down position and the PANEL KEY SET 01 switch is in either the normal or up position, the PANEL KEYS data will be OR'ed with a 101010---10 pattern. If both of these switches are in the normal position, the PANEL KEYS data will not be modified.

A3F67, SCAN TEST - When set (down), this switch enables the maintenance mode operation of the SCAN TEST RING RESET (A3B14) and SCAN TEST STEP (A3B16) pushbuttons. These pushbuttons are used to control the stepping and resetting of the CPU scanner circuitry during test operations.

A3F68, COMP (PLS MODE) - When set (down), this switch causes a computer reset operation to be automatically performed approximately every millisecond. Following the reset, the CPU clock is automatically restarted, and enter-instruction and program-start operations are initiated.

A3F69, MSTR (PLS MODE) - This switch is used only in conjunction with switch A3F68 (COMP, PLS MODE). When both of these switches are set (down), a master reset operation is automatically performed approximately every millisecond. Following the reset, the CPU clock is automatically restarted, and enter-instruction and program-start operations are initiated.

A3F70, ALLOW ER INJ - When set (down), this switch enables the maintenance mode operation of the ERR INJECT ON (A3B20) and ERR INJECT OFF (A3B22) pushbuttons.

7101 CE CONSOLE PULSE SWITCHES

The pulse switches contained on the 7101 CE Console are shown in block diagram form on systems page 73.04.01.1. These switches are listed according to sequential console co-ordinates.

A3A14, INIT PROG LOAD - This pushbutton, which duplicates the function of the INITIAL PROGRAM LOAD pushbutton on the 7152 console and the INITIAL LOAD pushbutton on the Exchange CE console, is used in conjunction with the CHANNEL SIGNAL pushbuttons on various I/O devices to initially load a program into the system without executing a programmed Read instruction. The program to be loaded must start with a control word that specifies the number of words to be read and the core storage address into which the first program instruction is to be stored. After the program has been stored, the CPU automatically starts the execution of the new program.

When initially setting up the manual controls for an initial program load operation, the operator must first depress the CHANNEL SIGNAL pushbutton on the I/O device that is to be subsequently used for this purpose. Since a tape drive unit will generate a channel signal at the end of a rewind operation, the operator must ensure that such an operation is not in process unless the tape drive unit being rewound is to be used as the program source. After the desired channel signal has been generated, the operator can initiate the initial program load operation by depressing the INITIAL PROGRAM LOAD pushbutton.

When depressed, the INITIAL PROGRAM LOAD pushbutton will cause the following sequence:

a. A program halt operation will be executed to terminate the execution of the stored program.

b. A master reset operation will be executed to reset all of the control and error triggers in the CPU.

c. A start clock operation will be executed to reinitiate the generation of controlled clock pulses.

d. An initial program-load-start pulse will be sent to the Exchange. This pulse will:

   1. Reset the Exchange circuits to terminate all I/O operations.

   2. Reset all control words in the Exchange to zero.

   3. Reset all I/O devices to an initial power-on status.

   4. Set the Exchange circuits so that the channel signal will be interpreted in a special way.

After the INITIAL PROGRAM LOAD pushbutton is depressed, the selected channel signal will cause the following sequence:

a. The Exchange circuits will store a simulated control word into the associated control word location. This control word will contain the following:

   1. Data word address = 4
   2. Chain flag = 1
   3. Multiple flag = 0
   4. Skip flag = 0
   5. Count = 1
   6. Refill address = 4

Note

Data word address 4 refers to a special core storage location which is used only during initial program load operations.

b. The Exchange circuits will execute a simulated read instruction on the selected channel to initiate the loading of the desired program.

c. The first word read from the selected I/O device will be stored in the special core storage location (address 4). Since the simulated control word is then exhausted, its refill address will cause the next control word to be fetched from location 4 which was just loaded with the first word of the desired program. This new control word will specify the address at which the first program instruction is to be stored and the number of program words that are to be stored. After the new control word is stored into the associated control word location, reading will continue as in normal operation.

d. After the read operation is completed, the Exchange circuits will send an initial-start signal to the CPU.

e. Upon receipt of the initial-start signal, the CPU circuits will fetch and execute the instruction contained in the location specified by the data word address field of the control word that was initially stored into address 4. In order to continue the execution of the newly stored program, this instruction, which is the first instruction of the stored program, must be a Branch Disabled instruction to the address of the second instruction. As a result of this requirement, the second instruction of the newly stored program is actually the first instruction of the desired program.

A3A16, START XS TEST - When depressed, this pushbutton initiates a series of index storage read or index storage read, clear, and write test cycles. The type of test cycles that are generated and the type of test control this is exercised is determined by the status of the INDEX STORAGE TEST level switches (A3F61-A3F64). The index storage test can be terminated by a stop-on-error condition or by setting the applicable level switch (A3F61 or A3F62) to the NORMAL position.

A3A18, DISPLAY - When depressed, this pushbutton causes the contents of the X register to be transferred into the 2Y register and the contents of the ADDRESS KEYS selected storage register (except locations 1, 3, and 5 through 12) to be transferred into the X and 1Y registers for display purposes. This pushbutton will also cause the contents of the ADDRESS KEYS to be transferred into the W register to preset this register for consecutive-display (CONS DISPLAY) operations.

A3020, CONS DISPLAY - When depressed, this pushbutton causes:

a. The contents of the X register to be transferred into the 2Y register.

b. The contents of the W register to be increased by 1.

c. The contents of the selected storage register to be transferred into the X and 1Y registers for display purposes. The storage register contents selected for display are addressed by the contents of the modified W register.

A3A22, STORE - When depressed, this pushbutton causes the contents of the PANEL KEYS (modified by the PANEL KEY SET UP switches) to be transferred into the X and 1Y registers. The contents of the X register are subsequently stored into the storage register (except storage register 1) specified by the contents of the ADDRESS KEYS. This pushbutton will also cause the contents of the ADDRESS KEYS to be transferred into the W register to preset this register for consecutive-store (CONS STORE) operations.

A3A24, CONS STORE - When depressed, this pushbutton causes:

a. The contents of the PANEL KEYS (modified by the PANEL KEY SET UP switches) to be transferred into the X and 1Y registers.

b. The contents of the W register to be increased by 1.

c. The contents of the X register to be transferred into the storage register (except storage register 1) specified by the modified contents of the W register.

A3A26, ENTER INST - When depressed, this pushbutton causes the contents of the PANEL KEYS (modified by the PANEL KEY SET UP switches) to be transferred into the 1Y register. If the PROGRAM START or SINGLE OP pushbutton is then depressed, the half-word (1Y 0-31) or full-word (1Y 0-63) instruction in the 1Y register will be executed prior to resuming the normal execution of the program.

A3B14, RING RESET (SCAN TEST) - When depressed, this pushbutton resets the CPU scan rings. This pushbutton is operative only if the SCAN TEST and MAINT MODE switches are set.

A3B16, RING STEP (SCAN TEST) - When depressed, this pushbutton advances the CPU scan rings by one position. This pushbutton is operative only if the SCAN TEST and MAINT MODE switches are set.

A3B18, SCAN - When depressed, this pushbutton initiates a scan operation which produces the same result as an error detected during normal operation. This pushbutton is operative only if the clock is stopped, the MAINT MODE switch is set, and the INHIBIT SCAN switch is clear.

A3B20, ON (ERR INJECT) - When depressed, this pushbutton sets bit 58 of the upper boundary register to inhibit the generation of boundary alarms and to enable bits 0 through 8 of this register to be used to inject errors into the I checker output lines. This pushbutton is operative only if the MAINT MODE and ALLOW ER INJ switches are set.

A3B22, OFF (ERR INJECT) - When depressed, this pushbutton clears bit 58 of the upper boundary register. This pushbutton is operative only if the MAINT MODE and ALLOW ER INJ switches are set.

A3B26, SINGLE OP - When depressed, this pushbutton causes one instruction to be loaded into lookahead from the I unit. The lookahead instruction will then be executed, and a new instruction will be transferred into the I unit if either the 1Y or the 2Y register is empty. This operation is similar to a program start, followed immediately by a program halt.

A3C18, AXXB - When depressed, this pushbutton causes controlled clock pulses to be distributed at one-third of the normal clock frequency. The frequency of free-running clock pulses is not affected by this pushbutton.

A3C20, 1 PULSE - When depressed, this pushbutton permits one controlled clock pulse (either an A or a B pulse, depending upon the status of the clock) to be distributed to the CPU. The clock must be stopped for this control to be operative.

A3C22, 2 PULSE - When depressed, this pushbutton permits two controlled clock pulses (either A and B or B and A, depending upon the status of the clock) to be distributed to the CPU. The clock must be stopped for this control to be operative.

A3C24, 3 PULSE - When depressed, this pushbutton permits three controlled clock pulses (either ABA or BAB, depending upon the status of the clock) to be distributed to the CPU. The clock must be stopped for this control to be operative.

A3D14, MASTER (RESET) - When depressed, this pushbutton resets the indicator register and all control and error triggers within the CPU. This pushbutton will also set the Program Halt Required, Program Halt, and I Recovery Required triggers to prepare the CPU for subsequent manual operations.

A3D16, ERR TGR (RESET) - When depressed, this pushbutton resets all of the error triggers within the CPU.

A3D18, COMPUTER (RESET) - When depressed, this pushbutton resets the indicator register and all of the control triggers within the CPU. This pushbutton will also set the Program Halt Required, Program Halt, and I Recovery Required triggers to prepare the CPU for subsequent manual operations.

A3D20, START (CLOCK) - When depressed, this pushbutton reinitiates the distribution of controlled clock pulses to the CPU. This pushbutton is effective only if the clock had been previously stopped by means of the STOP pushbutton.

A3D22, STOP (CLOCK) - When depressed, this pushbutton terminates the distribution of controlled clock pulses to the CPU after the next SBC pulse. Free-running pulses are not affected by this pushbutton. Control of the clock pulses is assumed by the 1 PULSE, 2 PULSE, or 3 PULSE pushbuttons.

A3D24, START (PROGRAM) - When depressed, this pushbutton causes the I unit to resume loading instructions into the lookahead unit. If the information that was previously loaded into the I unit has been destroyed because of manual operations, this pushbutton will initiate an I unit recovery operation prior to resuming lookahead loading. However, if the information that was previously loaded into the I unit is still valid, lookahead loading will be resumed from the point at which it was previously stopped.

A3D26, HALT (PROGRAM) - When depressed, this pushbutton causes a Program Halt to be set, thereby trigger-suppressing lookahead loading and allowing the instruction unit to fill up and wait for lookahead. Normally, this pushbutton is used to stop the execution of the program to permit manual intervention.

7101 CE CONSOLE MARGINAL CHECK CONTROLS

The marginal check controls contained on the 7101 CE console are shown in block diagram form on systems page 02.04.00.1. These controls are listed according to sequential console co-ordinates.

A3F075, RESET - This momentary contact toggle switch is used to deselect the marginal check selection circuits that were previously set by one of the MARGINAL CHECK SELECTION toggle switches. This switch, which is actuated by setting it to either the UP or DOWN position, is operative only if the CPU is in the maintenance mode and if the +6 MAR and -12 MAR Variacs are in the neutral or 0 position.

A3F076-A3F093, MARGINAL CHECK SELECTION - These 18 momentary contact toggle switches are associated with the 18 frames of the CPU and are used to select the CPU frame or frames which will be subsequently marginal checked. The MARGINAL CHECK SELECTION switches associated with the CPU frame or frames to be tested must be momentarily set to either the UP or DOWN position prior to the application of a marginal check voltage excursion. If the switch is momentarily set to the UP position, the associated CPU frame will be conditioned for a marginal check excursion on its +6v supply line. If the switch is momentarily set to the DOWN position, the associated CPU frame will be conditioned for a marginal check excursion on its -12v supply line. These switches are operative only if the CPU is in the maintenance mode and if the +6 MAR and -12 MAR Variacs are in the neutral or 0 position.

A3J097, FRAME SELECTOR - This 20-position rotary switch, which can be set to select any one of the 19 CPU frames, is used to select a particular CPU frame for voltage-monitoring purposes. The nine output lines of this switch, which represent the various voltage supply lines within the selected CPU frame, are connected as input lines to the METER RANGE SELECTOR switch.

A3N097, METER RANGE SELECTOR - This 10-position rotary switch is used to connect the 7101 CE console marginal check voltmeter to any voltage supply line of the selected CPU frame.

+6 MAR Variac - This Variac is used to apply both positive and negative voltage excursions to the +6v supply line of the selected CPU frames. This Variac is operative only if the CPU is in the maintenance mode.

-12 MAR Variac - This Variac is used to apply both positive and negative voltage excursions to the -12v supply line of the selected CPU frames. This Variac is operative only if the CPU is in the maintenance mode.

MEM DRVS Variac - This Variac is used to apply both positive and negative voltage excursions to the +60v supply line which is permanently connected to the index core storage driver circuits that are contained in CPU frame 14.

DESCRIPTION

This category contains:

a. An analysis of the file number coding scheme used for program identification.

b. A brief description of the applicable CPU maintenance programs.

c. The general procedure to be followed when marginal checking individual frames of the CPU.

FILE NUMBER PROGRAM IDENTIFICATION CODE

All maintenance programs used with the 7030 DPS are identified by a mnemonic code and a file number code. The file number assigned to each program is a 7-character alphanumeric code which signifies the following:

a. 1st character- Specifies the Data Processing System.
Example: The letters J and K are used to designate the 7030 DPS.

b. 2nd character- Specifies the type of program control.
Examples: A designates self-control.
B designates SSIP control.
C designates DCP control.

c. 3rd character- Blank

d. 4th character- Specifies a major area of the system.
Examples: A designates the CPU.
B designates the CSU.
C designates the Tape System.
E designates the Exchange.
F designates the FIX program.
N designates peripheral units.
S designates the systems test.
T designates the Disk System.
U designates a utility program.

e. 5th character- Specifies a detailed area of the system, using letters A through Z.

f. 6th character- Specifies the program number, using numbers 1 through 9.

g. 7th character- Specifies revision level, using letters A through Z.

MAINTENANCE PROGRAM ABSTRACTS

The following list briefly describes the current 7101 CPU maintenance programs. The program listing and the associated detailed writeup for each program are available in the program library.

I-BOX 1: The I-BOX 1 program (File No. JA AX1) is a go/no-go type of reliability program which tests the following I-unit instructions:

a. Unconditional Branch

b. Direct Index Arithmetic except RNX, LVE, and SVA

c. Immediate Index Arithmetic except LVS

d. Index Branching

e. Store Instruction Counter If

If no errors exist, this program will cycle indefinitely. If an error is detected, the program will branch to a specified address and hang up. This program should be run before any other CPU maintenance program.

SENSE SWITCH INTERROGATION PROGRAM (SSIP). This maintenance control program (File No. JA UA1) controls the execution of all CPU maintenance programs except the SMFI-1 program. This program contains eight options which are selected by sense switches (PANEL KEYS) as follows:

PANEL KEYS Position	Option
32 -	Suppress error printout
33 -	Stop on error
34 -	Repeat each test 100 times, and print number of errors
35 -	Repeat current test indefinitely
36 -	Print out section identity
37 -	Repeat block of tests
38 -	Start each test enabled
39 -	Spare

An option is selected when the associated PANEL KEYS switch on the 7101 CE console is placed in the DOWN position. In addition to these options, this program contains four print formats: identity print, single error print, total error count, and indicator printout as a result of an interrupt.

I-BOX 2: The I-BOX 2 program (File No. JB AX2) checks the CPU for proper execution of the Store Zero, Compare Value, and Compare Count instructions and for proper selection of an index storage register. This program, which operates under control of the SSIP program, should normally be executed after the I-BOX 1 program.

I-BOX 3: The I-BOX 3 program (File No. JB AX3) checks the CPU for proper loading and storing of index registers. This program, which operates under control of the SSIP program, should normally be run after the I-BOX 2 program.

I-BOX 4: The I-BOX 4 program (File No. JB AX4) checks the CPU for proper execution of the Transmit and Swap instructions and varied instructions in the direct index, immediate index, index branch, and miscellaneous classes. This program, which operates under control of the SSIP program, should normally be run after the I-BOX 3 program.

I-BOX 5: The I-BOX 5 program (File No. JB AX5) exercises the programming features of the CPU such as the time clock, the interrupt system, and boundary control. This program, which operates under control of the SSIP program, should normally be run after the I-BOX 4 program.

VFL INSTRUCTION (VFL INSTRUCT): The VFL INSTRUCT program (File No. JB AV1) checks the execution of all VFL instructions and the associated SAU control circuits. This program, which operates under control of the SSIP program, should normally be run after the I-BOX 5 program.

FLOATING POINT INSTRUCTION (FLO PNT INST): The FLO PNT INST program (File No. JB AF1) checks the execution of all floating point instructions and associated control circuits. This program, which operates under control of the SSIP program, should normally be executed after the VFL INSTRUCT program.

I-BOX, I-CHKR: The I-BOX, I-CHKR program (File No. JB AC1) checks the reliability of the I checker. This program, which operates under control of the SSIP program, should be used after the I-unit programs are executed or when the I checker is suspected of being faulty.

MEMORY 1: The MEMORY 1 program (File No. KC BA1) uses a number of tests to check the operation of all core storage units. Error injection is used to check the error correction bits and to isolate single bit failures. The program operates under self-control.

SYSTEMS EVALUATION (SEVA): The SEVA program (File No. KA SS1) is an overall test of the central processor unit and all available I/O devices. Random numbers are used in algebraic problems, using VFL and floating point arithmetic. Solutions are obtained and checked for accuracy. Random numbers are also used in information transfers to I/O devices to check these units. The program is completely self-controlled.

GENERAL PROCEDURE FOR MARGINAL CHECKING INDIVIDUAL FRAMES OF CPU

1. Refer to table 3.6.1 to determine which program(s) should be executed to exercise circuits within CPU frame(s) to be checked.

2. Refer to applicable program writeup for specific loading and operating procedures.

3. Load and execute program to ensure reliability of CPU under non-marginal check conditions. If an error is detected, correct system operation before continuing to step 4.

4. Stop program.

5. Set FRAME SELECTION switch for frame to be tested. Set this momentary contact toggle switch to UP position if +6v line is to be varied or to DOWN position if -12v line is to be varied.

6. Set METER RANGE SELECTOR rotary switch to voltage line that is to be varied.

7. Set FRAME SELECTOR rotary switch to frame that is to be voltage-monitored.

8. Start program.

9. Turn knob on applicable Variac to obtain excursion specified in table 3.6.1.

10. Allow program to make several passes with margin applied, and then perform following:

    a. If program runs successfully, either check CPU circuits with an excursion of the opposite polarity as in step 9 or proceed to step 11.

    b. If program does not run satisfactorily, repair system and repeat steps 4 through 10.

11. Stop program, and reset Variac to its 0 position (red light will go out). Deselect CPU frame selection control circuits by setting marginal check RESET switch (momentary contact toggle switch) to either UP or DOWN position.

12. Repeat steps 2 through 10 for other marginal check voltage.

13. Repeat steps 1 through 11 to check circuits within other CPU frames.

TABLE 3.6.1. MARGINAL CHECK FRAME SELECTION CHART

Program Number	CPU Frame Number																	
	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
JA AX1			X	X	X	X	X	X	X	X								
JB AX2	X	X	X	X	X	X	X			X								X
*JB AX3	X	X	X	X	X	X	X											X
JB AX4			X	X	X	X	X	X	X	X								X
JB AX5			X	X	X	X	X	X	X	X								X
JB AV1								X	X	X	X	X	X	X	X	X	X	X
JB AF1								X	X	X	X	X	X	X	X	X	X	X
JB AC1			X	X	X	X	X			X								
KC BA1	X	X																

Notes: X - Specifies that the associated program should run successfully with a ±2v excursion on the +6 or -12v line.

* This program is also used to marginal check the index core storage drivers (located in frame 14) which are permanently associated with the MEM DRIVERS Variac. The index core storage circuits should operate satisfactorily with a ±2% excursion applied to the +60v (nominal) supply voltage that is applied to these drivers.

DESCRIPTION

This category contains a brief discussion of the I unit conditions under which particular bits of the indicator register will be set for CPU 7101, Serial No. 30,004 and higher.

MACHINE CHECK INDICATOR

The machine check (MK) indicator (bit 0 of the indicator register) is set directly from the nonidentifiable check (NIDC) trigger in the I unit. The NIDC trigger can be set under any of the following conditions:

a. A conditional index adder error (refer to table 3.7.1).

b. A conditional uncorrectable error (refer to table 3.7.2).

c. Any error that occurs during the advancing of the instruction counter.

d. A conditional I unit parity error (refer to table 3.7.3).

e. An index storage address check which does not condition the identification check (IDC) trigger in the I unit.

f. A conditional memory check (refer to table 3.7.4).
Note: The conditions for gating the 1Y and 2Y MC triggers to the IDC or NIDC triggers are shown in table 3.7.5.

g. A store address, return address, or boundary register parity error that is detected by the storage bus control circuits.

INSTRUCTION REJECT INDICATOR

The instruction reject (IJ) indicator (bit 2 of the indicator register) is set from the identifiable check (IDC) trigger in lookahead, which in turn is set from the Z right or Z left identifiable check (ZRIDC or ZLIDC) trigger in the I unit. The ZRIDC and ZLIDC triggers can be set under any of the following conditions:

a. A conditional I unit parity error when using ZR or ZL controls (refer to table 3.7.6).

b. A conditional uncorrectable error when using ZR or ZL controls (refer to table 3.7.7).

c. A conditional index adder error when the NIDC trigger is not conditioned (refer to table 3.7.8).

d. The 1Y or 2Y IDC trigger is set and the corresponding Y to Z transfer trigger is also set (refer to table 3.7.9).

e. A lookahead parity error when using ZR or ZL controls.

f. A conditional index storage address check when using ZR or ZL controls (refer to table 3.7.10).

g. A memory check if the NIDC trigger is not conditioned.

OPERATION CODE INVALID INDICATOR

The operation code invalid (OP) indicator (bit 15 of the indicator register) is set if an undefined operation code is detected or if one of four special conditions exists. Invalid operation codes associated with VFL, I/O, and FP instructions are noted in table 3.7.11, and invalid operation codes associated with I unit instructions are noted in table 3.7.12.

The special conditions under which the OP indicator is set are noted below:

a. VFL store instruction specifies immediate addressing.

b. Progressive indexing (PX) is specified and the I-field is zero.

c. The Z register contains the left half word of two full-word instructions.

d. A miscellaneous instruction is decoded while the full-word (FW) trigger is on.

ADDRESS INVALID INDICATOR

The address invalid (AD) indicator (bit 16 of the indicator register) is set from the AD trigger in lookahead, which in turn is set from the Z left or Z right address invalid (ZLAD or ZRAD) trigger in the I unit or the AD trigger in the SAU or PAU unit.

The AD indicator will be set under any of the following conditions:

a. An out-of-bounds address is detected by the storage bus control circuits during the execution of an instruction fetch operation. The above error condition, which includes the free instruction fetch for IRPT OP, IPL OP, EX OP, and EXID OP conditions, will set the appropriate trigger only if the repeat instruction level switch (located on the 7101 CE console) is in the NORMAL position.

b. A data store or data fetch boundary alarm is detected during the execution of VFL, IO, and FP instructions (refer to table 3.7.13).

c. A data store or data fetch boundary alarm is detected during the execution of I unit instructions (refer to table 3.7.14).

UNENDED SEQUENCE OF ADDRESSES INDICATOR

The unended sequence of addresses (USA) indicator (bit 17 of the indicator register) is set directly from the USA trigger in the I unit. The USA trigger is set if more than 1 ms passes during the execution of an EX, EXID, or LVE instruction. The elapsed time is detected by use of a PUSA (prepare for a USA condition) trigger, which is set when a time clock break in pulse occurs during the execution of these instructions and reset at the completion of these instructions. When set, the PUSA trigger will gate the next time clock advance pulse (1 ms later) to set the USA trigger.

EXECUTE EXCEPTION INDICATOR

The execute exception (EXE) indicator (bit 18 of the indicator register) is set by:

a. The LOP3 sequencer if a successful branch condition is detected during EX mode operation.

b. The LOP4 sequencer if a branch disabled (BD) or store instruction counter on branch disabled (SIC-BD) instruction is decoded during EX mode operation.

DATA STORE INDICATOR

The data store (DS) indicator (bit 19 of the indicator register) is set from the DS trigger in lookahead, which in turn is set (except during the execution of a SIC-BI instruction) from the ZDS trigger in the I unit. The ZDS trigger is set on boundary alarms according to the conditions noted in table 3.7.15. This indicator will also be set if a VFL or FP instruction attempts to store data into storage location 2 or 3.

DATA FETCH INDICATOR

The data fetch (DF) indicator (bit 20 of the indicator register) is set from the DF trigger in lookahead, which in turn is set from the ZDF trigger in the I unit. The ZDF trigger is set on boundary alarms according to the conditions noted in table 3.7.16. This indicator will also be set if a VFL or FP instruction attempts to fetch the data from storage location 1, 2, or 3.

INSTRUCTION FETCH INDICATOR

The instruction fetch (IF) indicator (bit 21 of the indicator register) is set from the IF trigger in lookahead, which in turn is set from the Z right or Z left instruction fetch (ZRIF or ZLIF) trigger in the I unit. The ZRIF or ZLIF trigger is set if an out of bounds address is detected by the storage bus control circuits during the execution of an instruction fetch operation. The above error condition,which includes the free instruction fetch for IPL OP, EX OP, and EXID OP conditions, will set the appropriate IF trigger only if the repeat instruction level switch (located on the 7101 CE console) is in the NORMAL position.

If the above operation fetches a branch instruction, the ZRIF or ZLIF trigger will be set only if a boundary alarm is generated, the branch condition is successful, and the branch address is valid. If the above operation fetches a BB or BI instruction, then the appropriate IF trigger will be set directly on a boundary alarm. Under this condition, however, the ZRIF and ZLIF triggers are not gated to the IF trigger in lookahead.

TABLE 3.7.1. INDEX ADDER ERROR CONDITIONS THAT SET NIDC TRIGGER

TMTD + TMTI + SWPD + SWPI	A	A				A					
BRANCH			A								
TIME CLOCK OP				A	A						
IRPT OP + IPL OP							A				
IRPT OP								A			
E-BOX SIC - BI + SIC - CB + SIC - CBR									A	A	
TMTD + SWPD + SDOP + CDOP + SSOP + CSOP + XSWT + XSRT											
RAM1 E	A		A							A	
LAM1 E		A									
CNT1 E											A
CNT1 EM				A							
ADD1 E						A					
ADD1 EM					A			A			
ADD3 E							A				
ADD5 E									A		
IAU ERROR	A	A	A	A	A	A	A	A	A	A	A

Legend: A - AND

Note: The NIDC (nonidentifiable check) trigger is subsequently sampled to set the MK (machine check) indicator (bit 0 of the indicator register).

TABLE 3.7.2. UNCORRECTABLE I UNIT ERROR CONDITIONS THAT SET NIDC TRIGGER

TMTD + TMTI + SWPD + SWPI	A					
RENAME		A				
SWPD + SWPI			A			
E - BOX SIC - BI + SIC - CB - SIC - CBR				A		
LDX3 E	A					
LDX4 E		A	A			
LDX5 E				A		
EMF3 M	A				A	
EMF4 M			A			A
LST3 E					A	
LST4 E						A
UNCORR ERROR	A	A	A	A	A	A

Legend: A - AND

Note: The NIDC (nonidentifiable check) trigger is subsequently sampled to set the MK (machine check) indicator (bit 0 of the indicator register).

TABLE 3.7.3. I UNIT PARITY ERROR CONDITIONS THAT SET NIDC TRIGGER

TMTD + TMTI + SWPD + SWPI	A						A				
SWPD + SWPI		A						A			
RENAME			A								
ANY SIC - BRANCH						A					
CHK4 E	A										
CHK5 E		A									
LST1 E			A								
LST3 E				A							
LST4 E					A						
LOP3 E						A					
LDX3 E							A				
LDX4 E								A			
EMF3 NM				A			A				
EMF4 NM					A			A			
Z-XA						$\overline{A}$					
NO-OP						$\overline{A}$					
BROK						A					
I-BOX PARITY ERROR	A	A	A	A	A	A	A	A			

Legends: A - AND

$\overline{A}$ - NOT AND

Note: The NIDC (nonidentifiable check) trigger is subsequently sampled to set the MK (machine check) indicator (bit 0 of the indicator register).

TABLE 3.7.4. MEMORY CHECK CONDITIONS THAT SET NIDC TRIGGER

TMTD + TMTI + SWPD + SWPI	A					
SWPD + SWPI		A				
RENAME			A			
LDX3 E	A					
LDX4 E		A	A			
LST3 E				A		
LST4 E					A	
MEMORY CHK	A	A	A	A	A	

Legend: A - AND

Note: The NIDC (nonidentifiable check) trigger is subsequently sampled to set the MK (machine check) indicator (bit 0 of the indicator register).

TABLE 3.7.5. 1Y AND 2Y MEMORY CHECK CONDITIONS THAT SET IDC OR NIDC TRIGGERS

EXID + LX + SX + RN + SV + SC + SR + SAD		A							A					
SWPD + SWPI + EXOP + EXID OP										A				
R + RCZ + ICR - I + ICRN - I + ICR + RN + PX + SDOP + CDOP + SSOP + CSOP				A							A			
CHK1 E	A							A						
LDX1 E		A							A					
LDX3 E			A											
LDX4 E				A						A	A			
LDX5 E					A							A		
LDX6 E						A							A	
LST3 E							A							
LST4 E														A
USE 1Y	A	A		A										
USE 2Y								A	A		A			
OA17					A	A						$\overline{A}$	$\overline{A}$	

Legends: A - AND

$\overline{A}$ - NOT AND

Note: The NIDC (nonidentifiable check) trigger is subsequently sampled to set the MK (machine check) indicator (bit 0 of the indicator register). The IDC (identifiable check) trigger in lookahead is subsequently sampled to set the IJ (instruction reject) indicator (bit 2 of the indicator register).

TABLE 3.7.6. I UNIT PARITY ERROR CONDITIONS THAT SET IDC TRIGGER

EXID + LX + SX + RN + SV + SC + SR + SAD	A						
EXOP + EXID OP		A					
EXOP			A				
R + RCZ + ICR-I + ICRN-I + LID + ICR + EXOP + EXID OP + PX				A			
R + RCZ					A		
LG + DX AND NOT RN						A	
LDX1 E	A						
LDX4 E		A					
CHK5 E				A			
CHK6 E					A	A	
EMF4 M		$\overline{A}$					
CHK4 E			A				
MOD ZL E + MOD ZR E							A
PX IN Y							A
FW NOT ST							A
XF + DEC ZL + DEC ZR							A

Legends: A – AND
$\overline{A}$ – NOT AND

Note: The IDC (identifiable check) trigger in lookahead is subsequently sampled to set the IJ (instruction reject) indicator (bit 2 of the indicator register).

TABLE 3.7.7. UNCORRECTABLE I UNIT ERROR CONDITIONS THAT SET IDC TRIGGER

EXID + DX$\overline{RN}$	A					
R + RCZ		A				
EX OP + EXID OP			A			A
R + RCZ + ICR-I + ICRN-I + ICR + PX				A		
SIC-CBR-CB + E-BOX SIC-BI					$\overline{A}$	
CHK1 E	A	A				
LDX3 E			A			
LDX4 E				A		A
LDX5 E					A	
EMF4 M						A

Legends: A – AND
$\overline{A}$ – NOT AND

Note: The IDC (identifiable check) trigger in lookahead is subsequently sampled to set the IJ (instruction reject) indicator (bit 2 of the indicator register).

TABLE 3.7.8. INDEX ADDER ERROR CONDITIONS THAT SET IDC TRIGGER

CNT1 E	A														
RAM1 E		A													
LAM1 E			A												
ADD1 E				A											
ADD2 E					A										
ADD3 E						A									
ADD4 E							A								
ADD5 E								A							
YL-ZR E									A						
YL-ZL E										A					
YR-ZR E											A				
YR-ZL E												A			
MOD ZR E													A		
MOD ZL E														A	
WBC TEST E															A
USE ZR + ZL	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
IAU ERROR	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A

Legend: A – AND

Note: The IDC (identifiable check) trigger in lookahead is subsequently sampled to set the IJ (instruction reject) indicator (bit 2 of the indicator register).

TABLE 3.7.9. 1Y AND 2Y ERROR CONDITIONS THAT SET IDC TRIGGER

1YMC	A			
2YMC			A	
UNCOR ERR		A		A
IWC1 E LTH	A	A		
IWC2 E LTH			A	A
ICOR E		A		A
	SET 1Y IDC		SET 2Y IDC	

Legend: A – AND

Note: The IDC (identifiable check) trigger in lookahead is subsequently sampled to set the IJ (instruction reject) indicator (bit 2 of the indicator register).

TABLE 3.7.10. INDEX STORAGE ADDRESS CHECK CONDITIONS THAT SET IDC TRIGGER

LG	A	O			
KV + KC		O			
DX NOT BLOCKED AND NOT (SX + SR + SV + SC + SAD + RN)		O			
SV + SC + SR + SX + SAD			A		
EX OP				A	
R + RCZ + ICR-I + ICRN-I + LID + EXOP + EXID OP + PX					A
XSF1 E	A	A			
XSF3 E			A		
XSF4 E				A	
XSF5 E					A

Legends: A – AND
O – OR

Note: The IDC (identifiable check) trigger in lookahead is subsequently sampled to set the IJ (instruction reject) indicator (bit 2 of the indicator register).

TABLE 3.7.11. VFL, FP, AND I/O CONDITIONS THAT SET OP TRIGGER

Z51	A	A					
Z52		A					
Z53	A	$\overline{A}$				A	A
Z54		$\overline{A}$		A		A	A
Z55	A	A	A	$\overline{A}$		A	
Z56	$\overline{A}$	$\overline{A}$	A	A		A	A
Z57	$\overline{A}$	$\overline{A}$	A	A			$\overline{A}$
Z58	$\overline{A}$	$\overline{A}$	A	$\overline{A}$			
Z59	$\overline{A}$	$\overline{A}$	A	A	A		
ZFW	A	A		A			
I-FIELD = 0					A		
PX01 + PX02					A		
IMMEDIATE				A			
GT FP IND-LA						A	A
GT VFL IND-LA	A	A	A	A	A		

Legends: A – AND
$\overline{A}$ – NOT AND

Note: The OP (operation code invalid) trigger is subsequently sampled to set the OP indicator (bit 15 of the indicator register).

TABLE 3.7.12. I UNIT CONDITIONS THAT SET OP TRIGGER

ZEDEC 19	A	A	A	A	A		
ZEDEC 20	$\overline{A}$	A	A	$\overline{A}$	A		
ZEDEC 21	A	$\overline{A}$	A	A	A		
ZEDEC 22	A	A	A	$\overline{A}$	$\overline{A}$		A
ZEDEC 23	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$		$\overline{A}$
ZEDEC 24	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	A	$\overline{A}$
ZEDEC 25	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$
ZEDEC 26	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$
ZEDEC 27	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$	$\overline{A}$
FULL WORD					$\overline{A}$	A	A
GI IEI-LA	A	A	A	A	A	A	A

Legends: A – AND
$\overline{A}$ – NOT AND

Note: The OP (operation code invalid) trigger is subsequently sampled to set the OP indicator (bit 15 of the indicator register).

TABLE 3.7.13. VFL, FP, AND I/O CONDITIONS THAT SET AD TRIGGER IN LOOKAHEAD

VFL					A						
VFL CL 2			A								
VFL CL 5					$\overline{A}$						
RD + WR + CCW				A							
FPL CL 2						$\overline{A}$					
FPL CL 3 + 4							A				
FPR CL 2									$\overline{A}$		
FPR CL 3 + 4										A	
ZL EQ1 + WEQ1-WBC			A								
ZR EQ 0-31 + NA				A							
WBC WNA + ZOAL NA					A						
ZL EQ1							A				
ZOAL NA						A					
ZR EQ1										A	
ZOAR NA									A		
IMMEDIATE					$\overline{A}$						
ZLAD*	A							A			
ZRAD*	A	A									A
GT VFL IND TO LA	A		A	A	A						
GT FPL IND TO LA		A				A	A	A			
GT FPR IND TO LA									A	A	A

Legends: A – AND
$\overline{A}$ – NOT AND

Note: The AD (address invalid) trigger is subsequently sampled to set the AD indicator (bit 16 of the indicator register).

*The ZLAD and ZRAD triggers can be set for VFL or FP instructions only if the address of the instruction itself is nonexistent.

TABLE 3.7.14. I UNIT ERROR CONDITIONS THAT SET AD TRIGGER IN LOOKAHEAD

EXID	A																	A
R + RCZ + ICR-I + ICRN-I + ICR + PX + SDOP + CDOP		A																
CB + CBR + SIC CB-CBR			$\bar{A}$						A									
SV + SC + SR + SAD				A														
BB								A										
RN							A						A					
SX											A							
SZ												A						
TMTD + TMTI														O	O			
SWPD + SWPI														O	O			
EMF1 E	A																A	A
EMF3 E															A			
EMF4 E		A																
EMF5 E			A															
EMF6 E					A													
EMF7 E						A												
XSF1 E				A														
XSF3 E											A							
DEC1 E							A			A		A						
DEC4 E								A										
CNT1 E									A					A				
ADD4 E													A					
LAMIE																		A
ZSA	A																	
RF ADR INV		A				A												
BR ADR INV			A				A		A									
SIC ADR INV					A					A								
ZOA = IRH				A														
BB BT ADR INVALID								A										
ZOAL = EEM																		A
BROK									A	A								
ZOA 1-NA											A	A		A				
ZOAL 1 + NA															A			
ZOAL NA																		
ZLNA USE ZL																	A	
ZRNA USE ZR																		A

LEGENDS: A – AND
$\bar{A}$ – NOT AND
O – OR

Note: The AD (address invalid) trigger is subsequently sampled to set the AD indicator (bit 16 of the indicator register).

TABLE 3.7.15. CONDITIONS FOR SETTING ZDS TRIGGER IN I UNIT

EXID + SC + SV + SR + SX + SAD + RN + R + RCZ		A												
RN						A								
SV + SC + SR + SAD							A		A				A	
R + RCZ + SX								A						
SZ										A				
BB											A			
SX														A
EMF 1		A					A	A						
EMF 6	A													
IRF 1									A					
XSF 1													A	
XSF 3														A
DEC 1										A				
DEC 3			A											
DEC 4											A			
LST 3				A								A		
LST 4					A								A	
ADD 4						A								
SIC ADR VALID	A		A											
ZOA = EEM		A												
ZOAR = EEM				A										
ZOAL = EEM					A									
ZLXA			$\overline{A}$											
ZOA = ILH													A	
ZOA = 2							A							
ZOA = 3									A					
ZOA = 1 + 2 + 3								A		A				A
ZOAR = 1 + 2 + 3												A		
ZOAL = 1 + 2 + 3													A	
ZOA = 2 + 3 CHANGE BIT											A			
BOUNDARY ALARM	A	A	A	A	A	A								
INTERRUPT ENABLED	A	A	A	A	A	A	A	A	A	A	A	A	A	A

Legends: A – AND
$\overline{A}$ – NOT AND

Note: The ZDS (Z register data store error) trigger is sampled to set the DS trigger in lookahead. This DS trigger is subsequently sampled to set the DS indicator (bit 19 of the indicator register).

TABLE 3.7.16. CONDITIONS FOR SETTING ZDF TRIGGER IN I UNIT

KV + KC + LG + DX (SX + SV + SC + SR + SAD + RN)	A						A						
TMTD + TMTI + SWPD + SWPI		A						A		A			A	
SWPD + SWPI				A					A		A			A
R - RCZ + ICR-I + ICRN-I + ICR + PX			A											
RN						A								
BB												A		
EMF 1	A						A							
EMF 3		A						A						
EMF 4			A	A					A					
EMF 7					A									
IRF 3										A				
IRF 4											A			
XSF 4													A	
XSF 5														A
DEC 1						A								
DEC 4												A		
ZOA = NOT NA + XA + SA	A													
ZOAL = EEM		A												
ZOAR = EEM				A										
W = EEM			A											
REFILL ADR VALID					A									
ZOA = 1 + 2 + 3							A							
ZOAL = 1 + 2 + 3								A		A			A	
ZOAR = +2 +3									A		A			A
ZL = +2 +3 NO CHANGE ON BIT												A		
BOUNDARY ALARM	A	A	A	A	A	A								
INTERRUPT ENABLED	A	A	A	A	A	A	A	A	A	A	A	A	A	A

Legend: A – AND

Note: The ZDF (Z register data fetch error) trigger is sampled to set the DS trigger in lookahead. This DS trigger is subsequently sampled to set the DF indicator (bit 20 of the indicator register).

EXAMPLE SHOWS TWO NORMALIZATION SEQUENCES. LOAD WITH FLAG IS THE SAME EXCEPT FLAG BITS ROUTED TO SIGN BYTE REGISTER ON LAST SAMPLE.

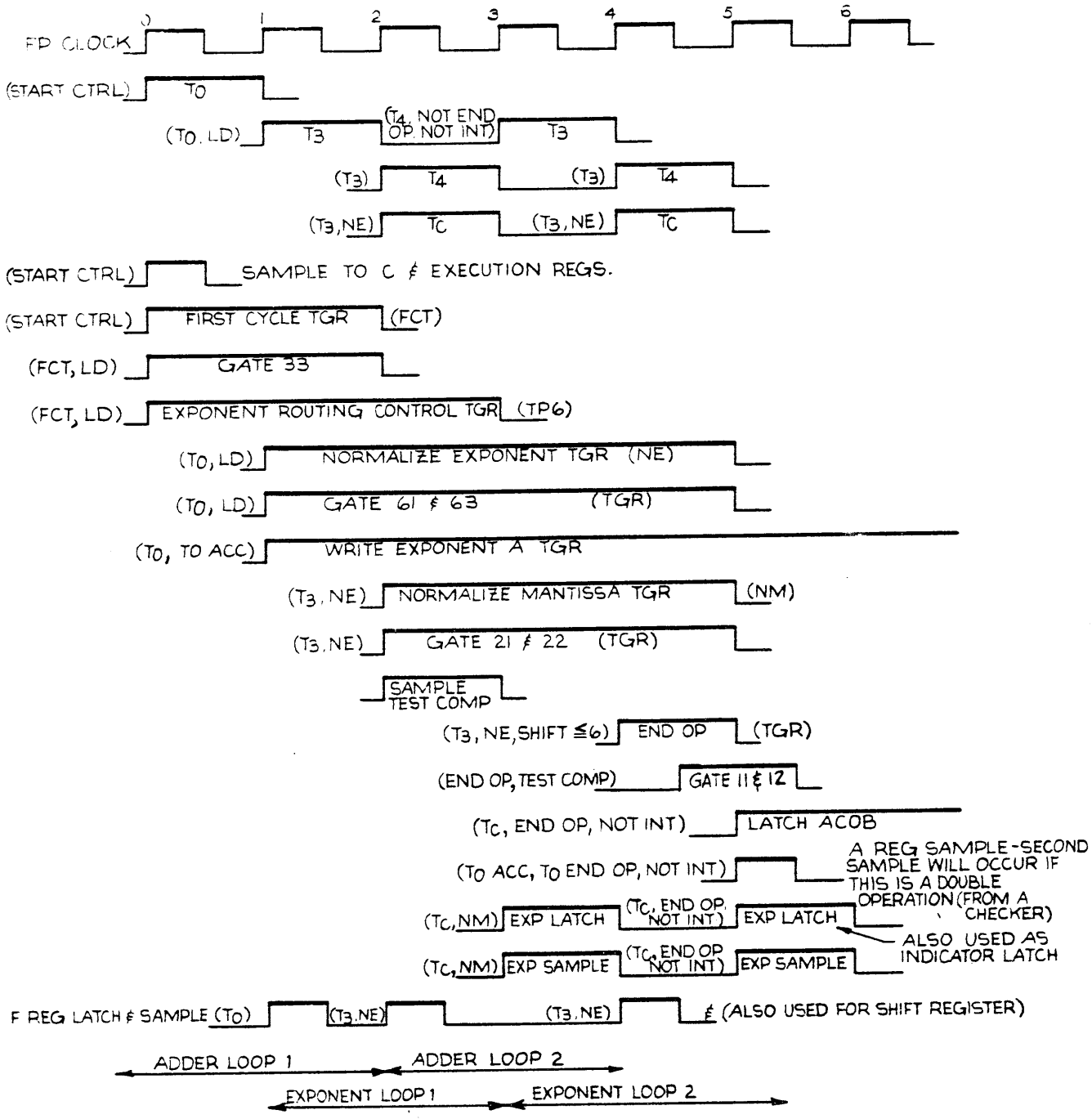


FIGURE 3.8.1. FLOATING-POINT LOAD (TIMING)

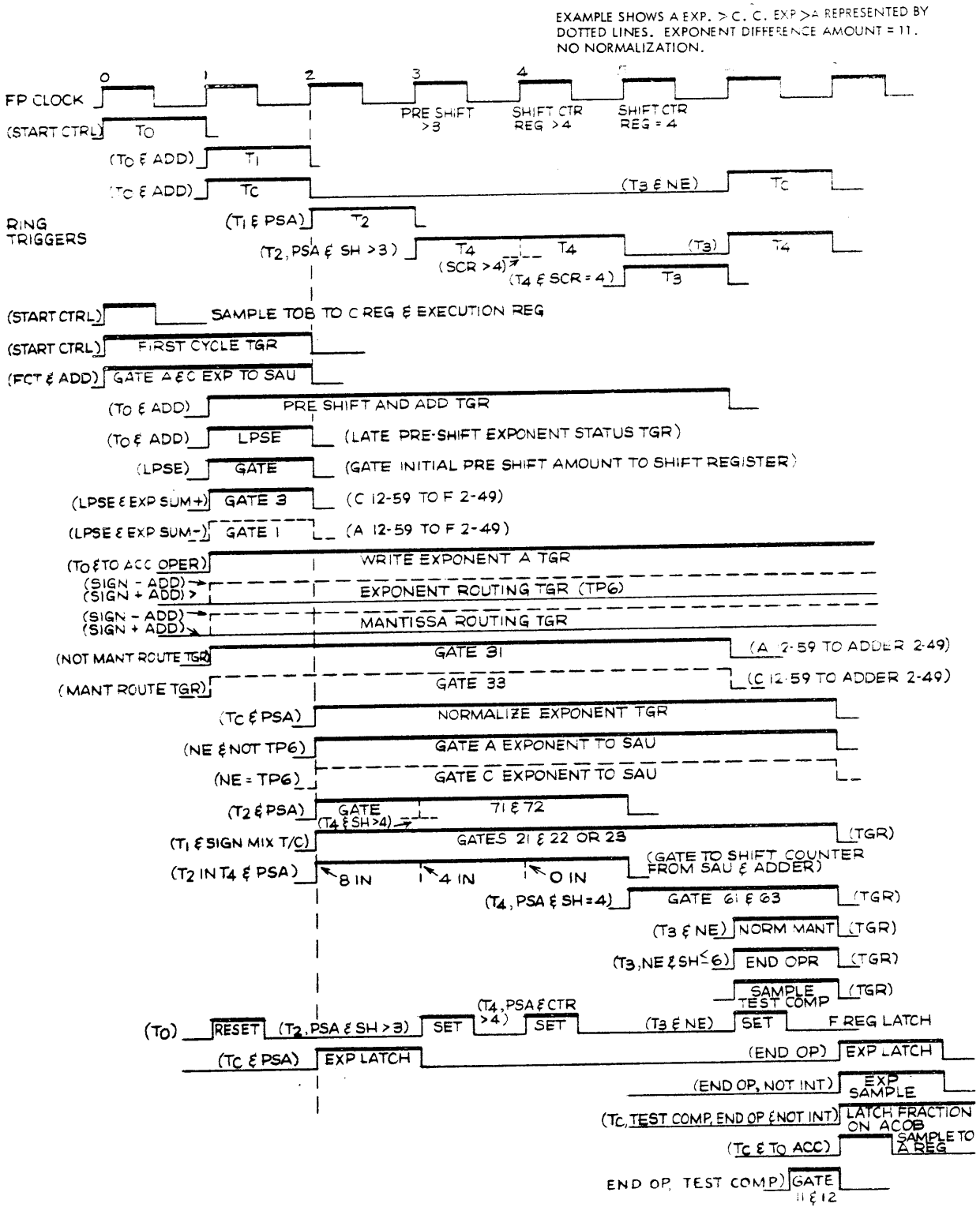


FIGURE 3.8.2. FLOATING-POINT ADD (TIMING)

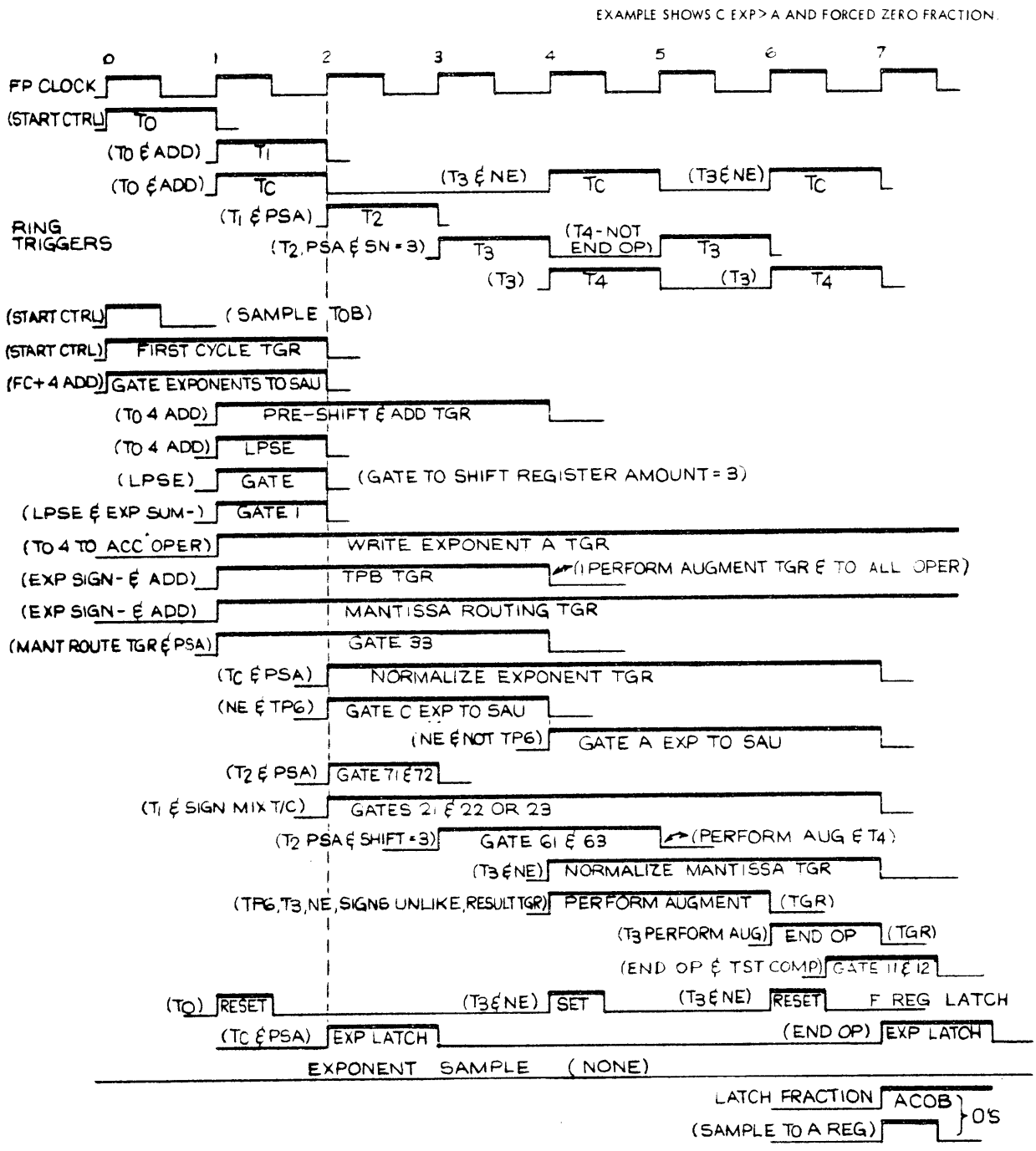
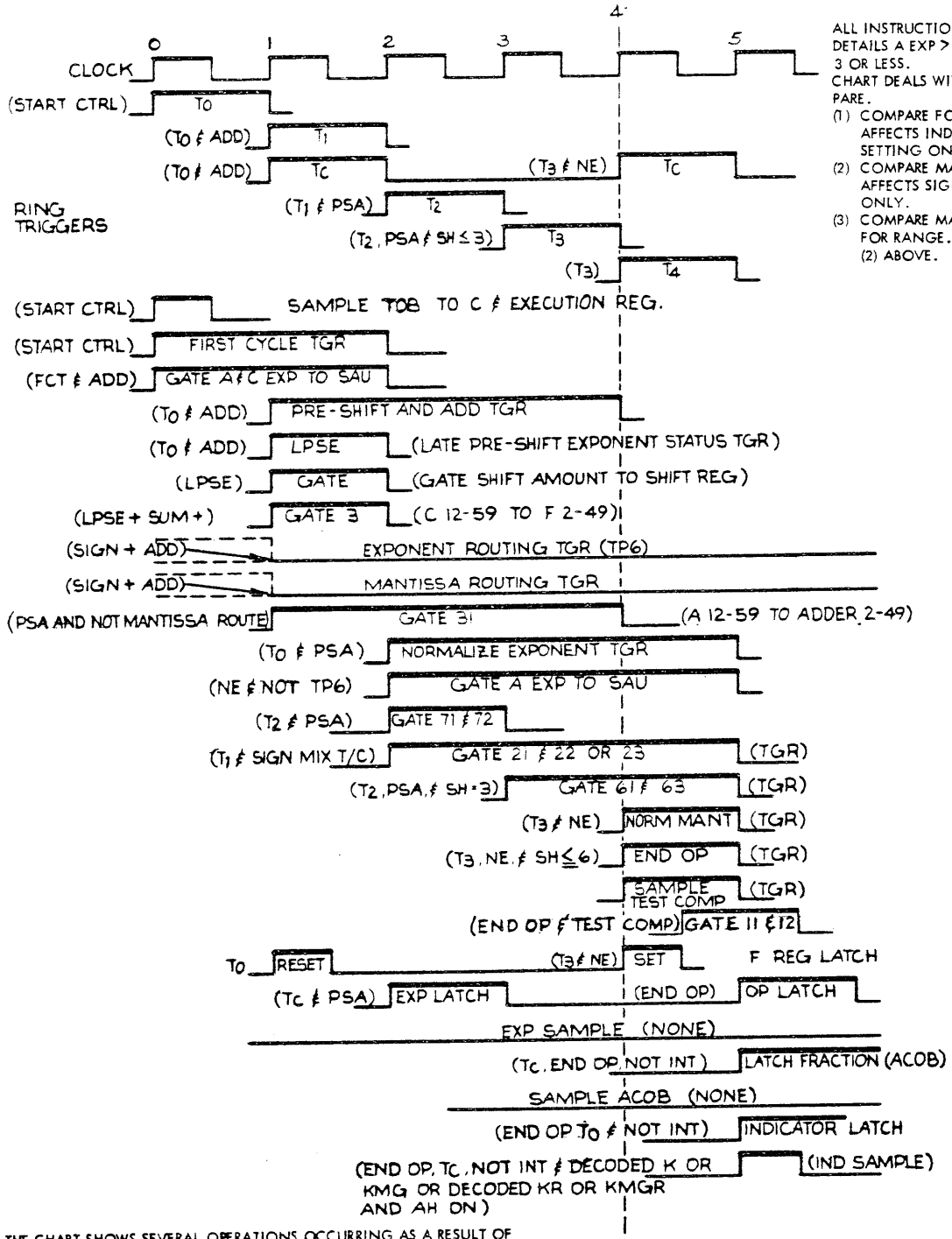


FIGURE 3.8.3. FLOATING POINT-ADD TO MAGNITUDE (TIMING)



NOTE: THE CHART SHOWS SEVERAL OPERATIONS OCCURRING AS A RESULT OF DECODED ADD CLASS INSTRUCTIONS. COMPARE IS AN ADD CLASS INST. AND THEREFORE USES MANY CONTROL LINES (USED ALSO FOR ADD).

FIGURE 3.8.4. FLOATING-POINT COMPARE (TIMING)

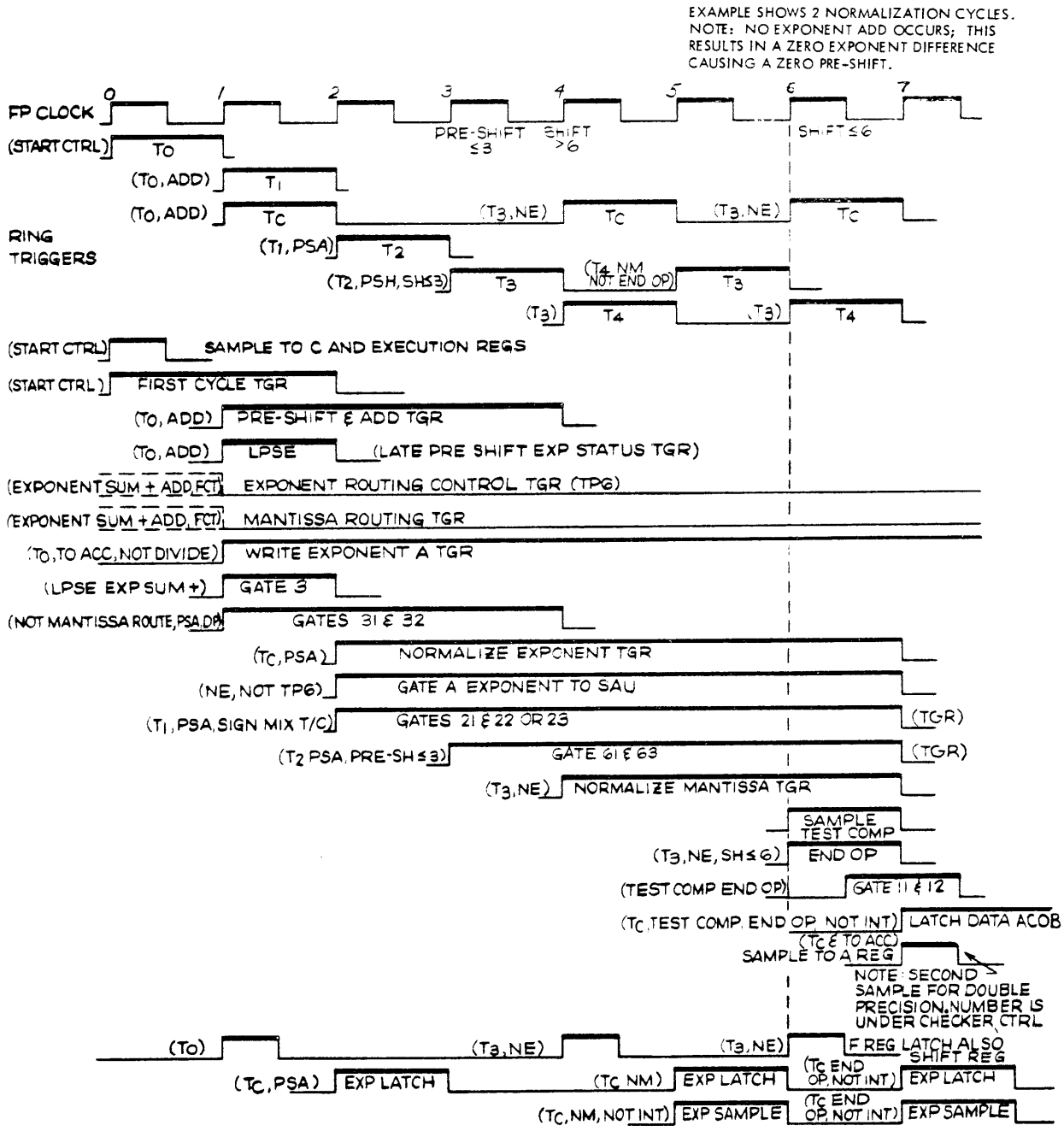


FIGURE 3.8.5. FLOATING-POINT ADD TO FRACTION (TIMING)

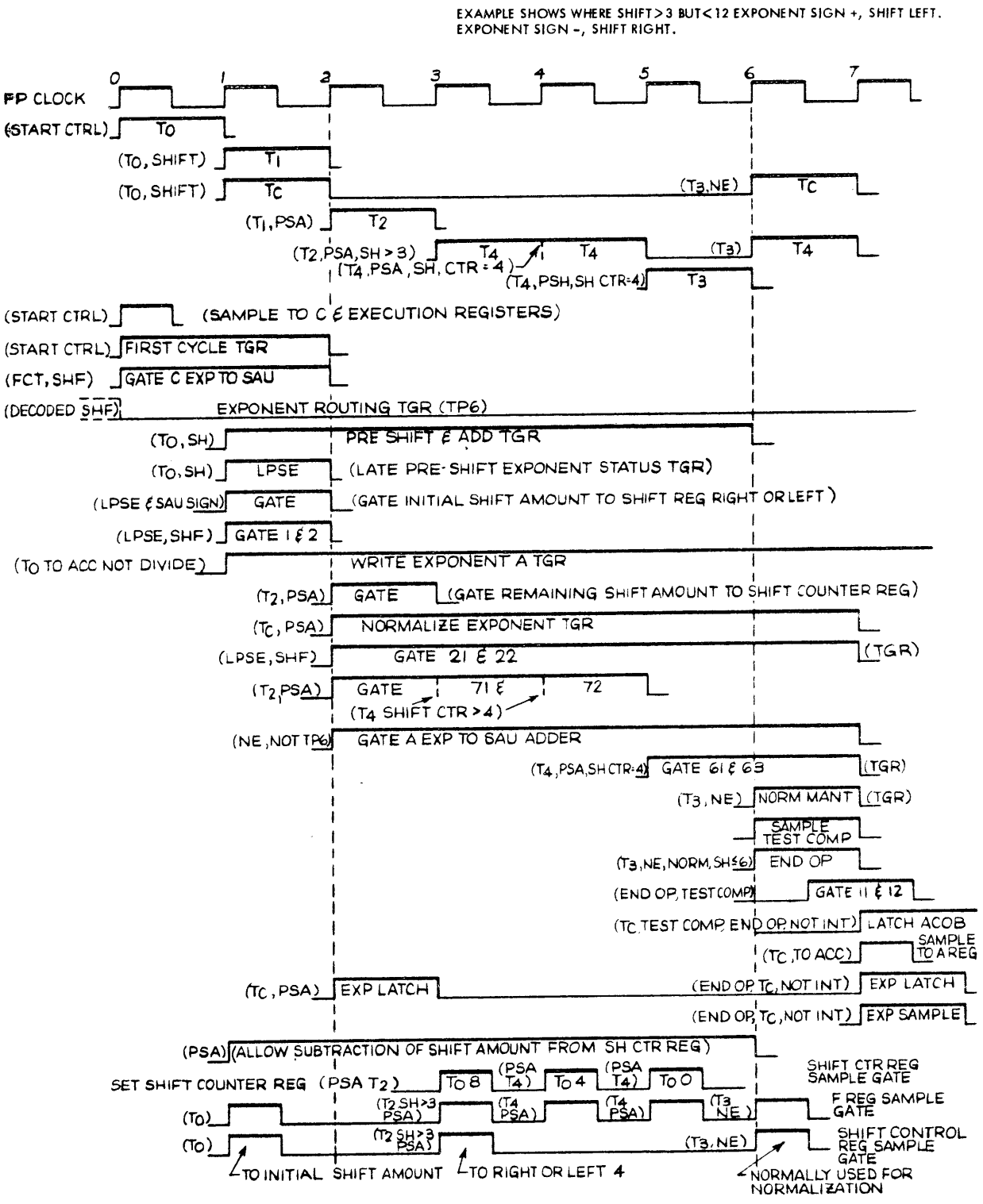


FIGURE 3.8.6. FLOATING-POINT SHIFT FRACTION (TIMING)

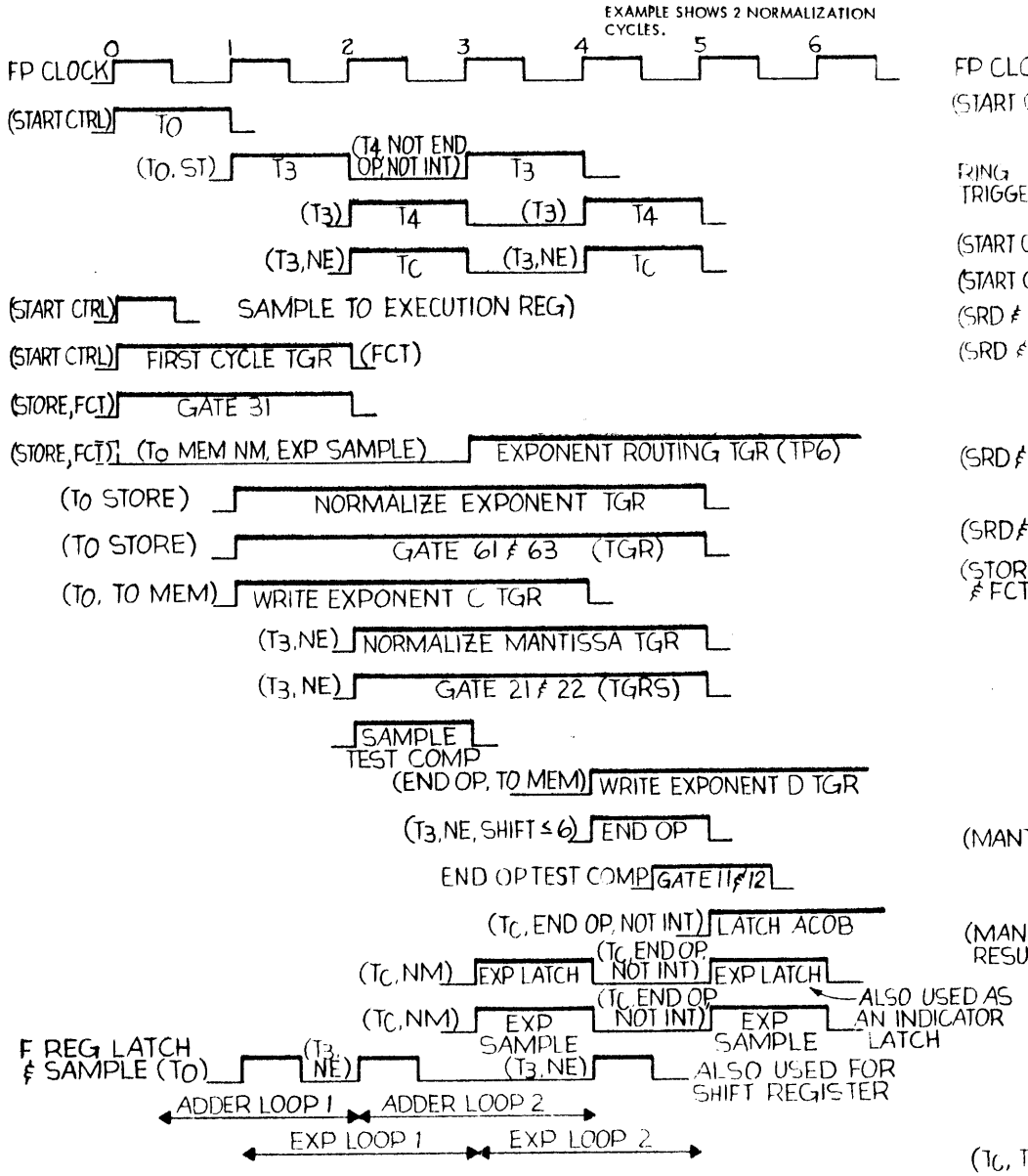


FIGURE 3.8.7. FLOATING-POINT STORE (TIMING)

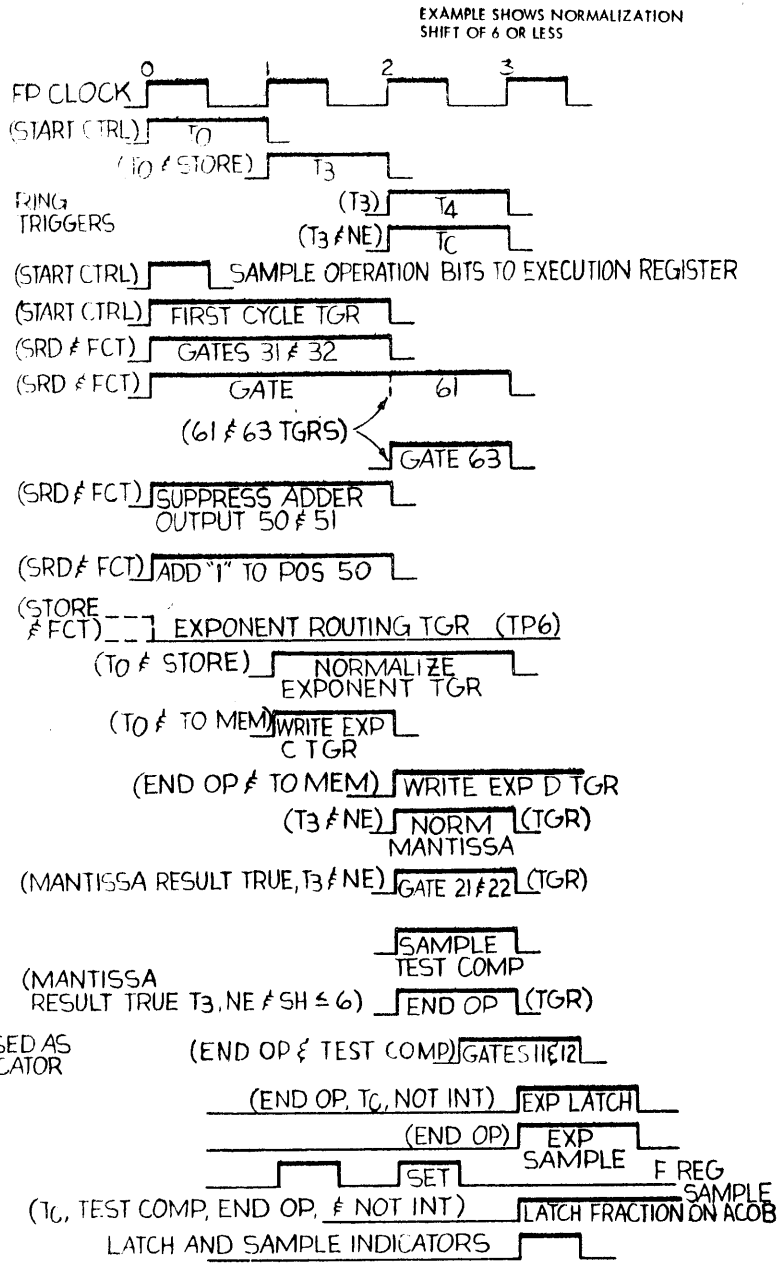


FIGURE 3.8.8. FLOATING-POINT STORE ROUNDED (TIMING)

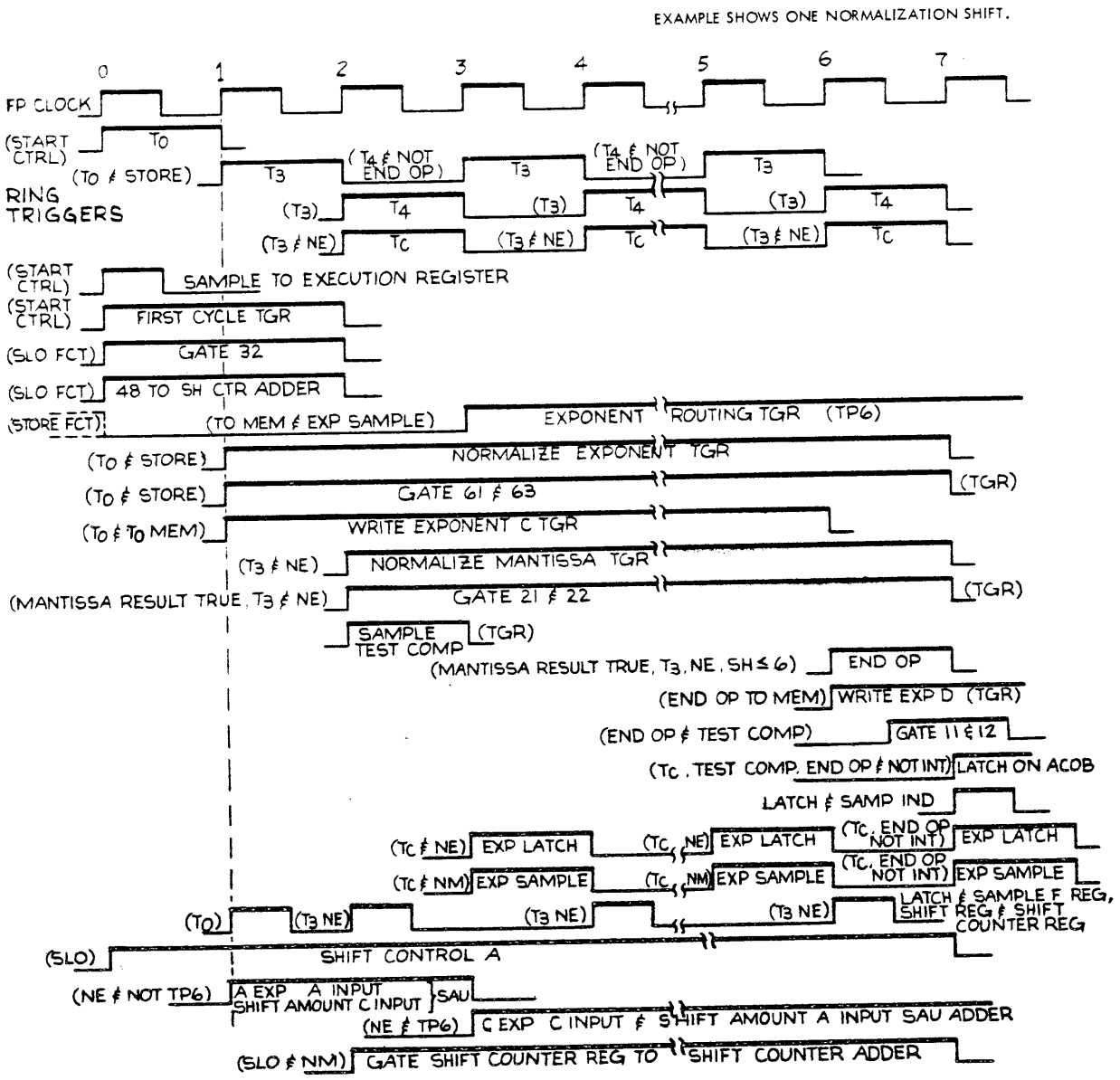


FIGURE 3.8.9. FLOATING-POINT STORE LOW ORDER (TIMING)

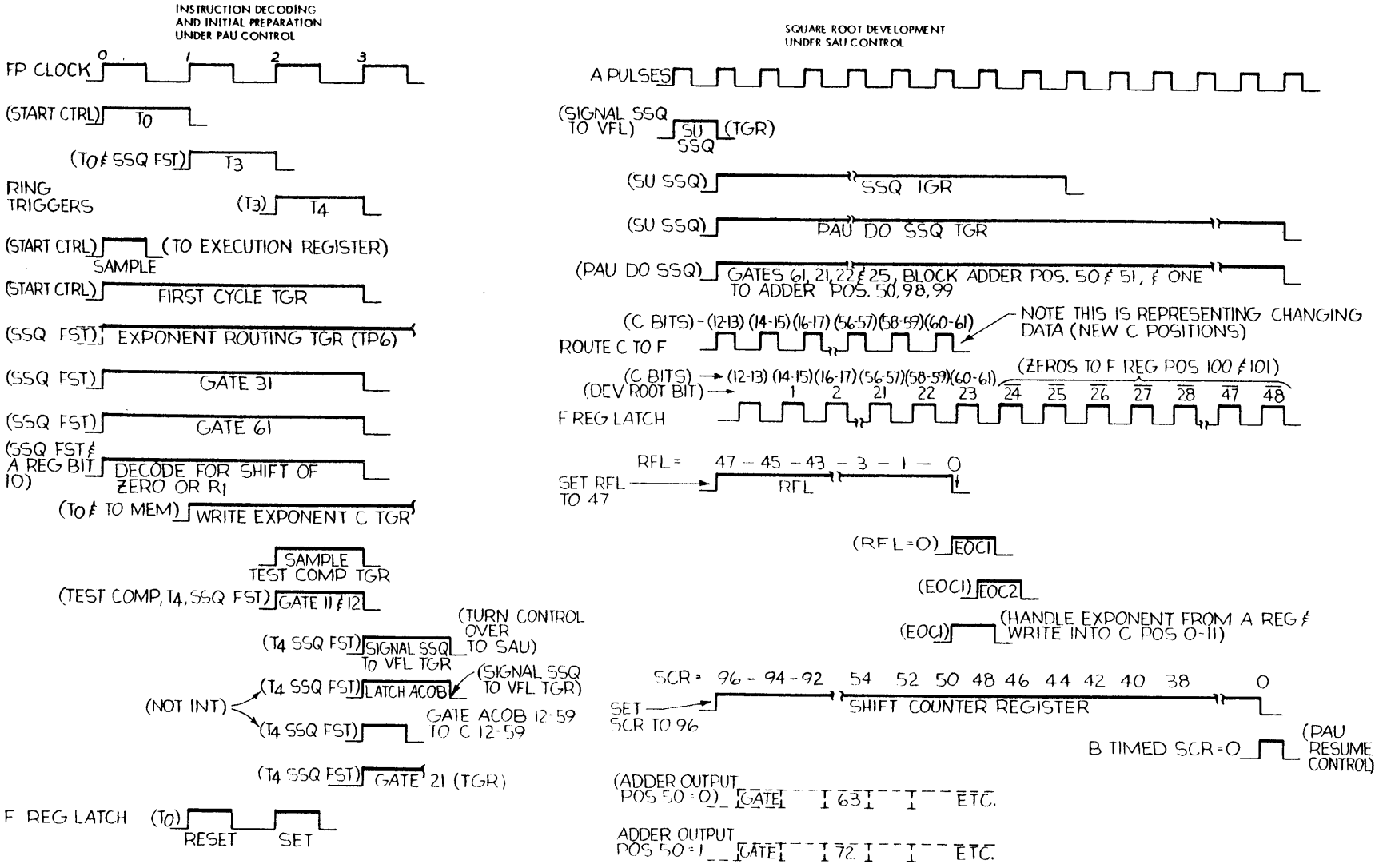


FIGURE 3.8.10. FLOATING-POINT STORE ROOT (TIMING) (SHEET 1 OF 2)

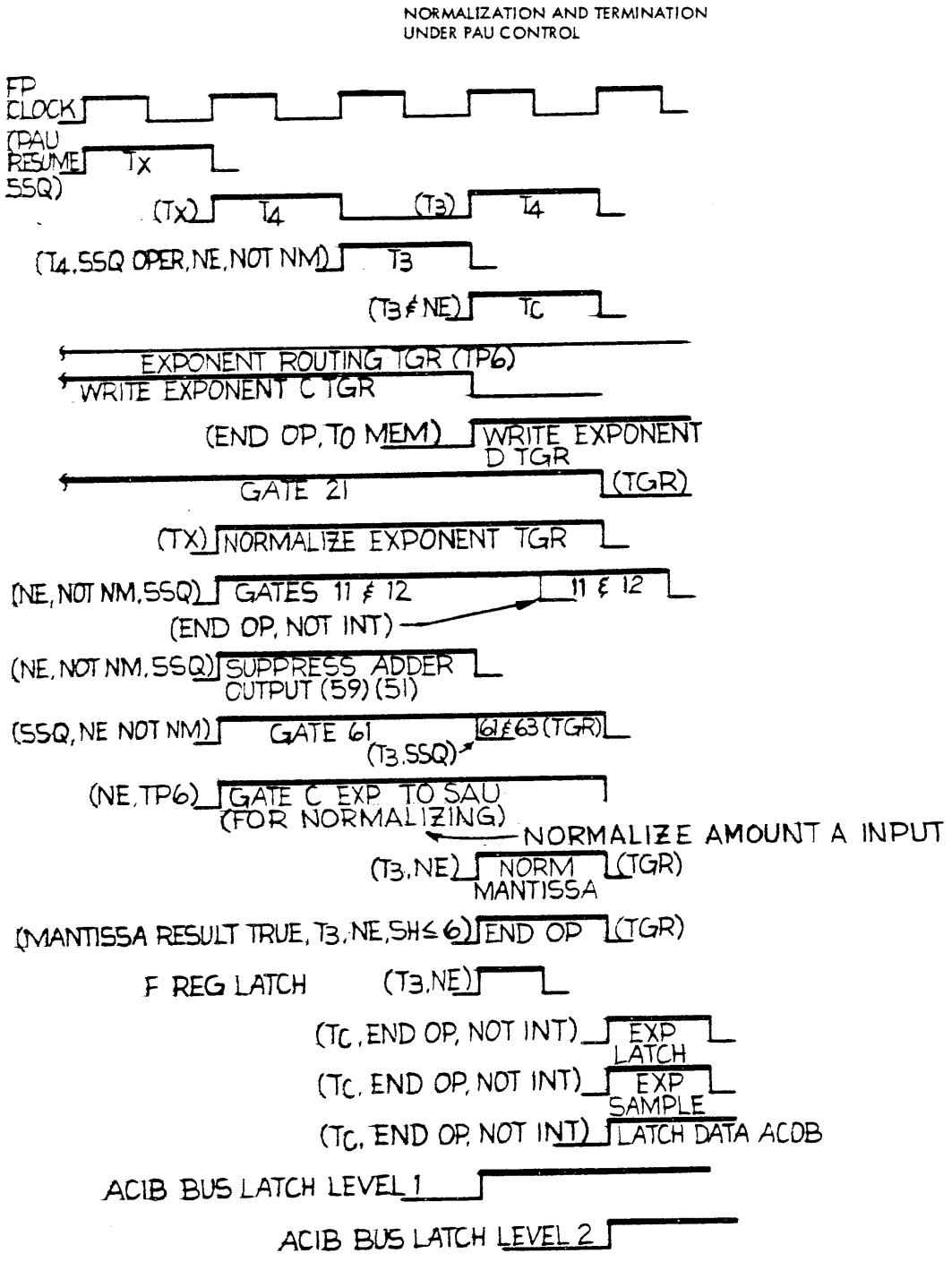


FIGURE 3.8.10. FLOATING-POINT STORE ROOT (TIMING) (SHEET 2 OF 2)

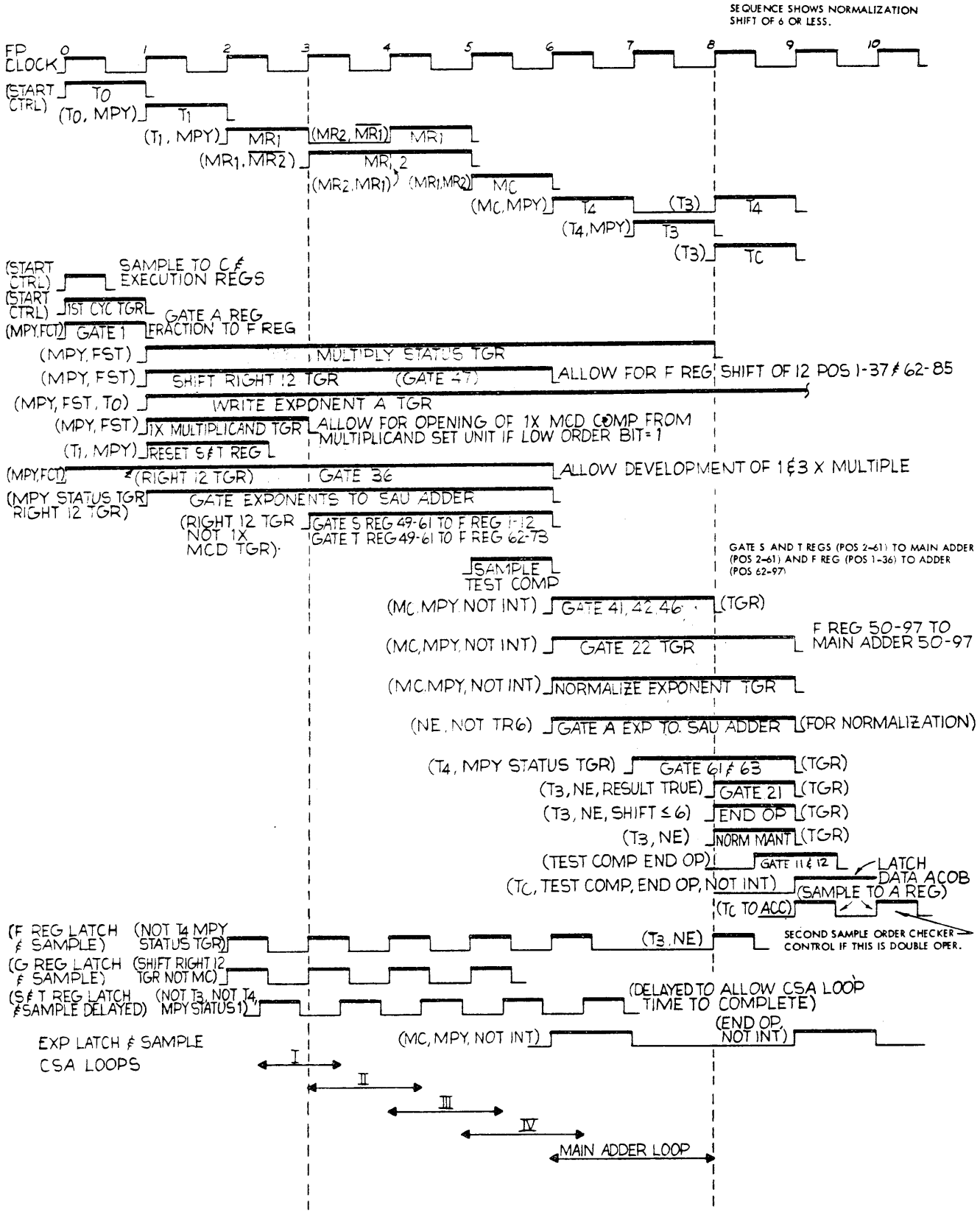


FIGURE 3.8.11. FLOATING-POINT MULTIPLY (TIMING)

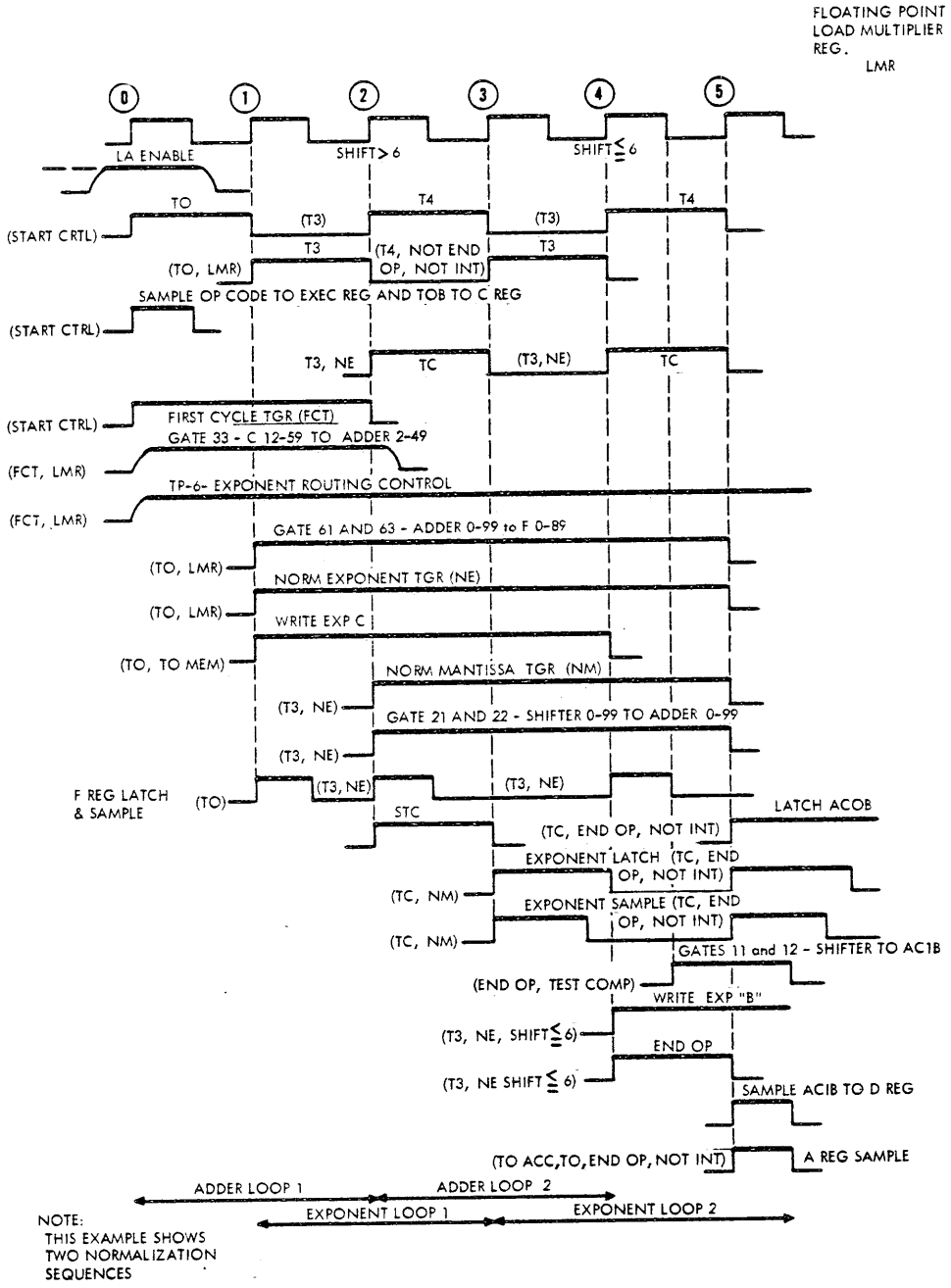


FIGURE 3.8.12. FLOATING-POINT LOAD MULTIPLER REGISTER (TIMING)

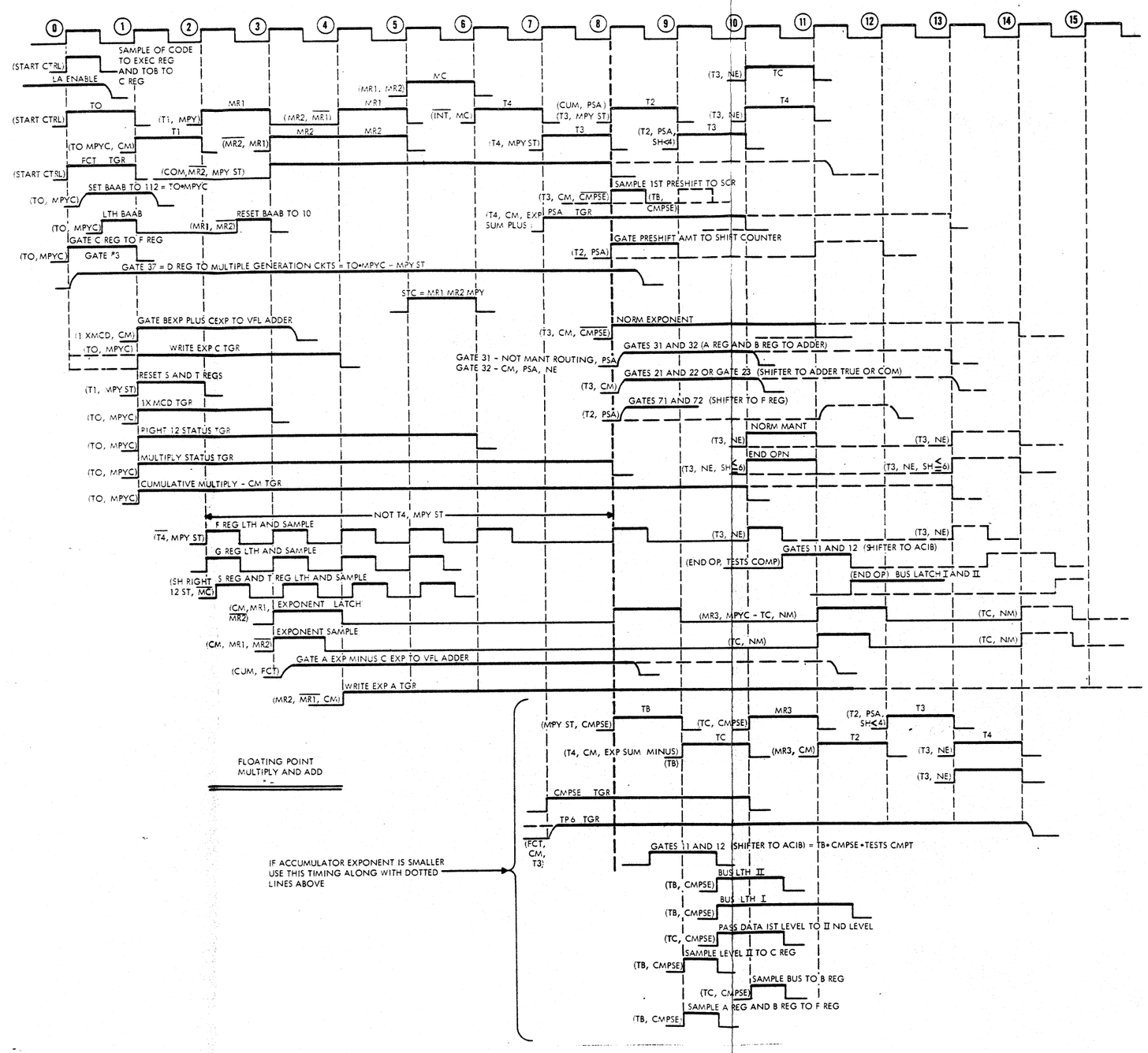


FIGURE 3.8.13. FLOATING-POINT MULTIPLY AND ADD (TIMING)

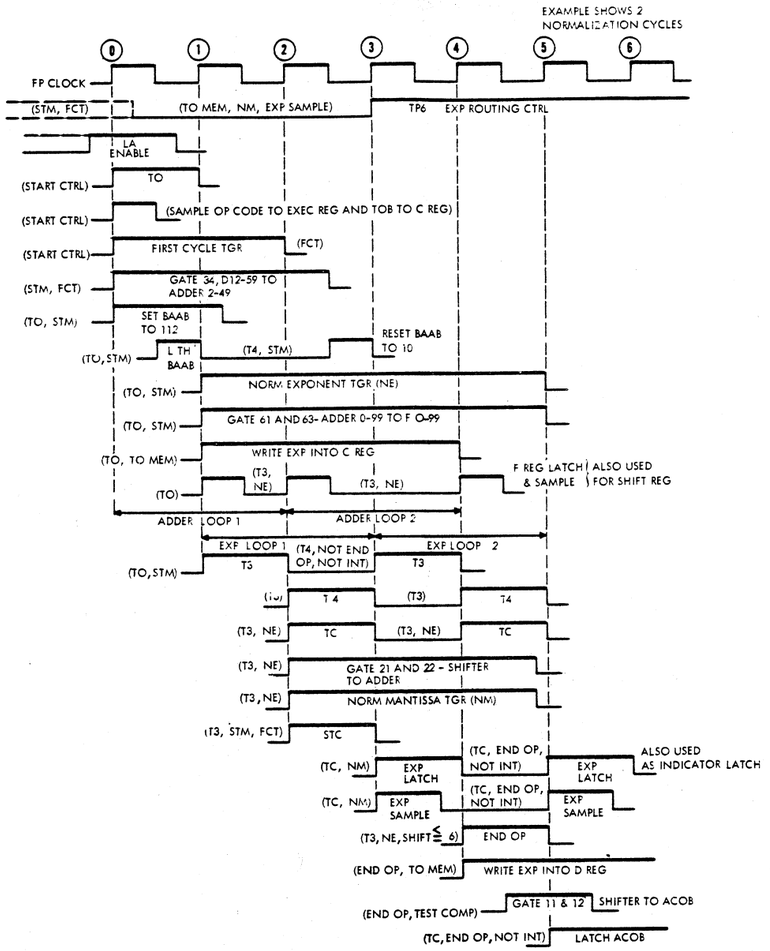


FIGURE 3.8.14. FLOATING-POINT STORE MULTIPLIER REGISTER (TIMING)

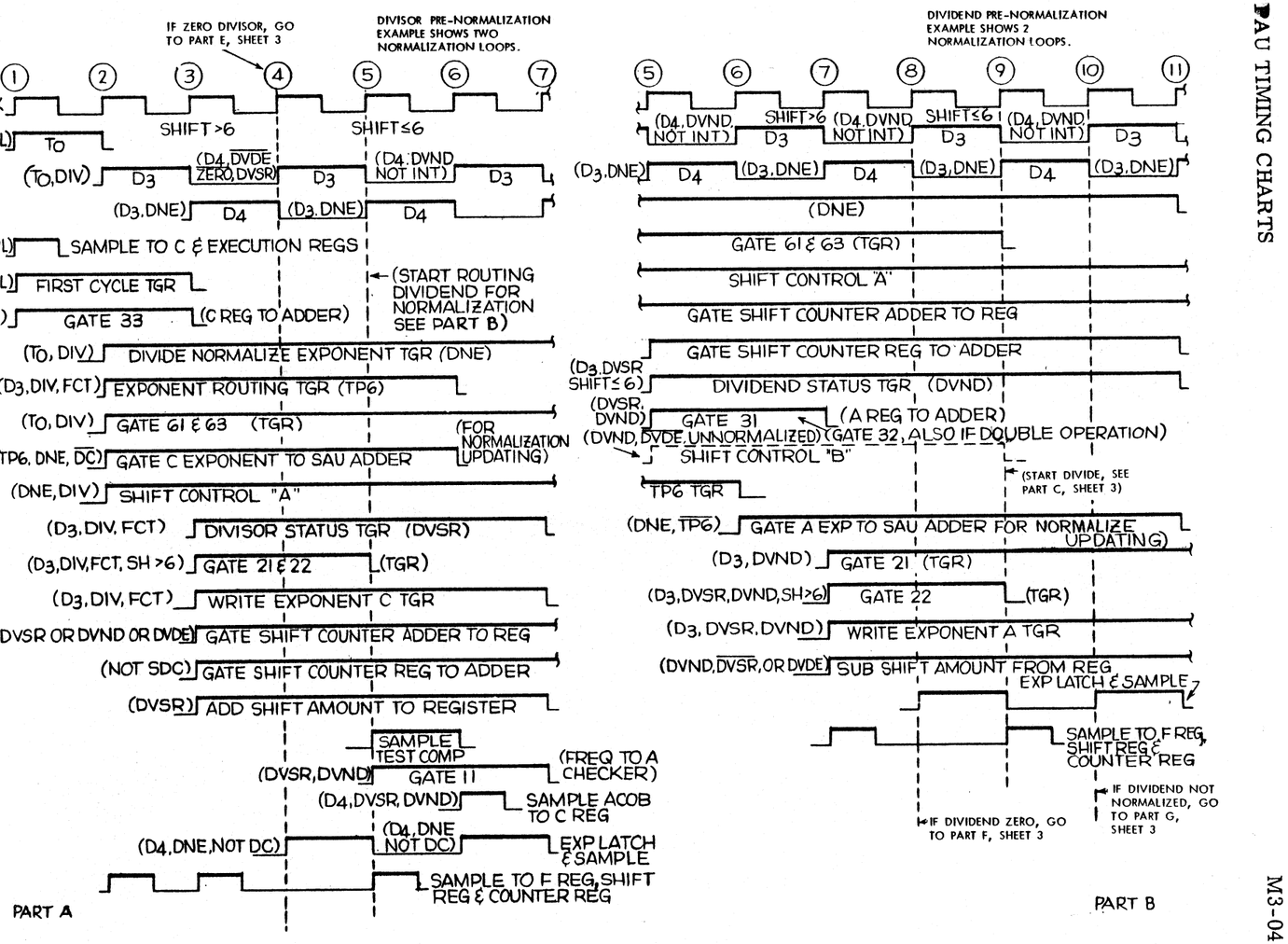


FIGURE 3.8.15. FLOATING-POINT DIVIDE (TIMING) (SHEET 1 OF 3)

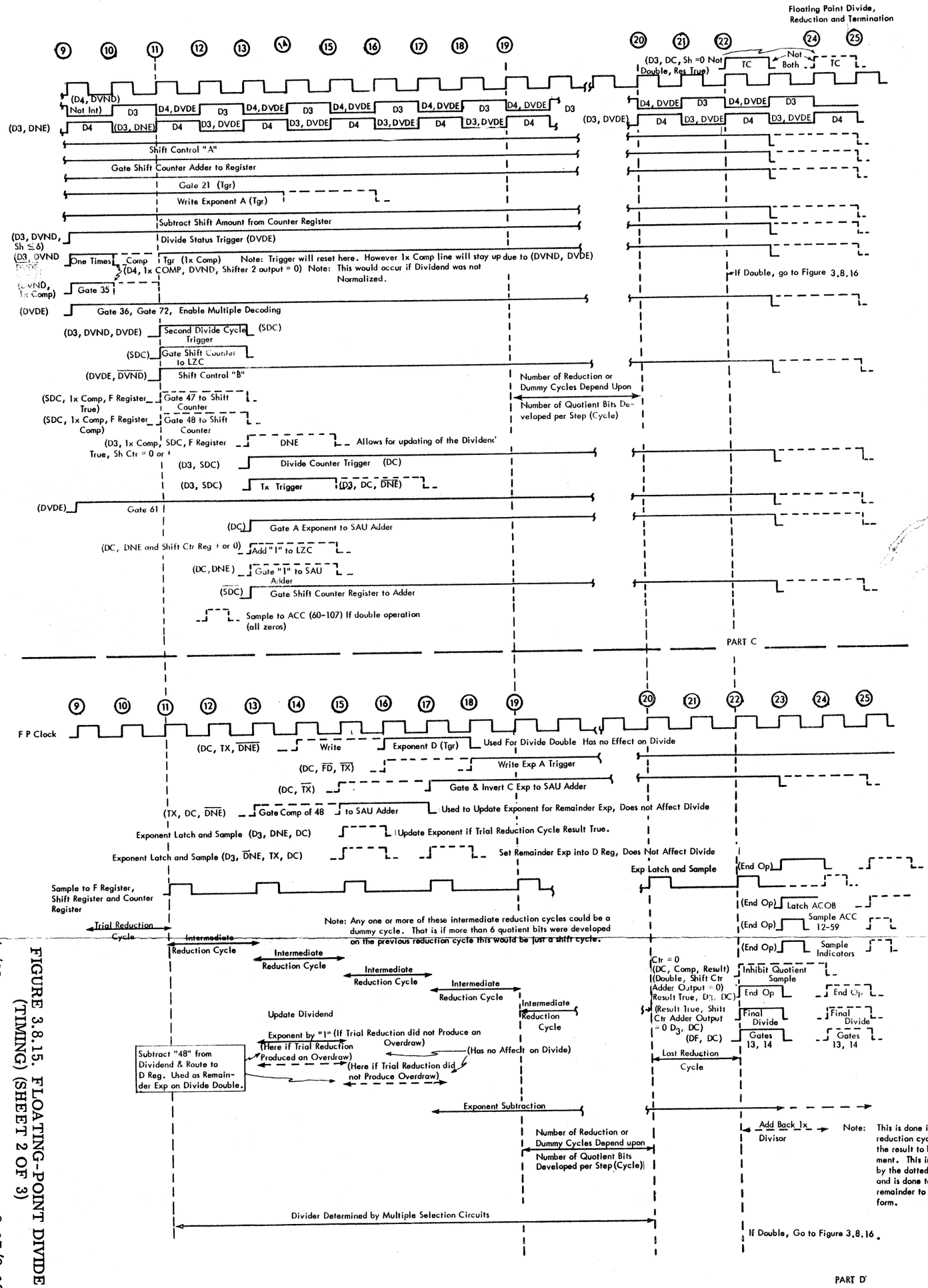


FIGURE 3.8.15. FLOATING-POINT DIVIDE (TIMING) (SHEET 2 OF 3)

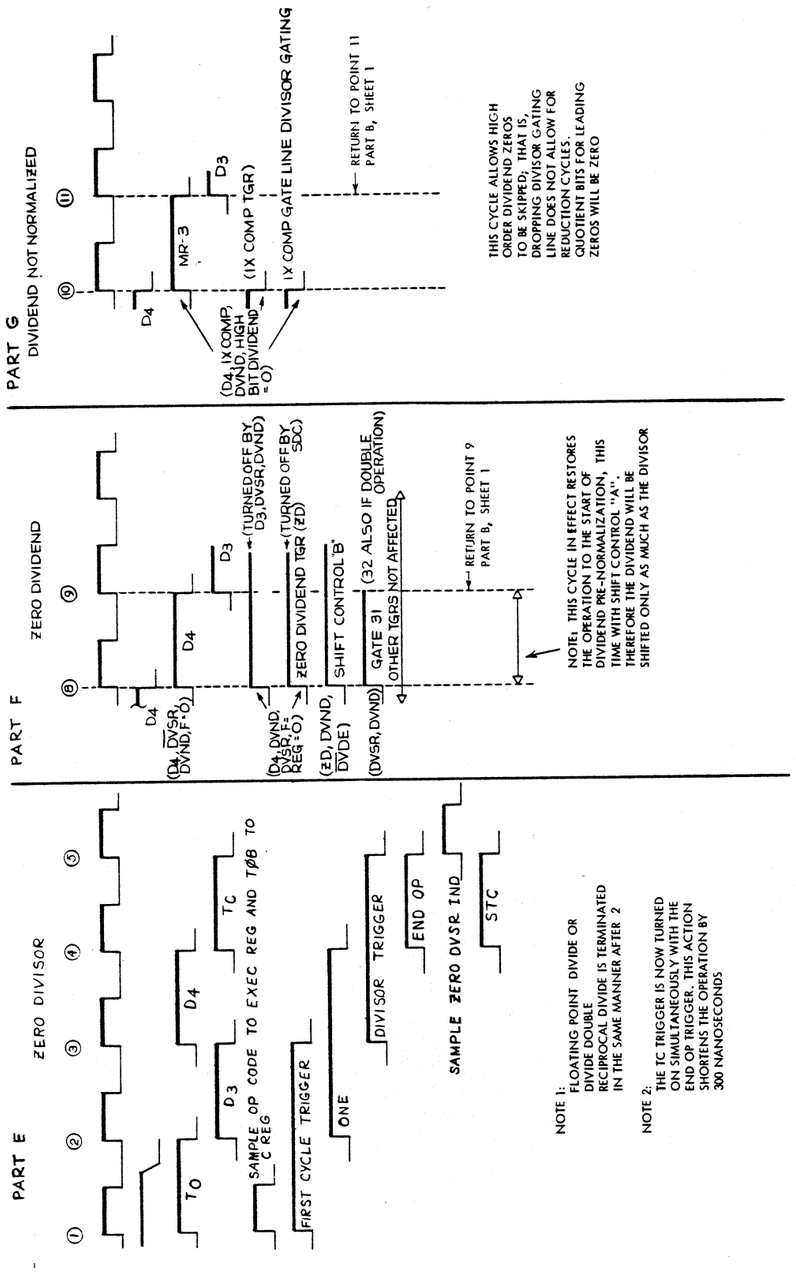


FIGURE 3.8.15. FLOATING-POINT DIVIDE (TIMING) (SHEET 3 OF 3)

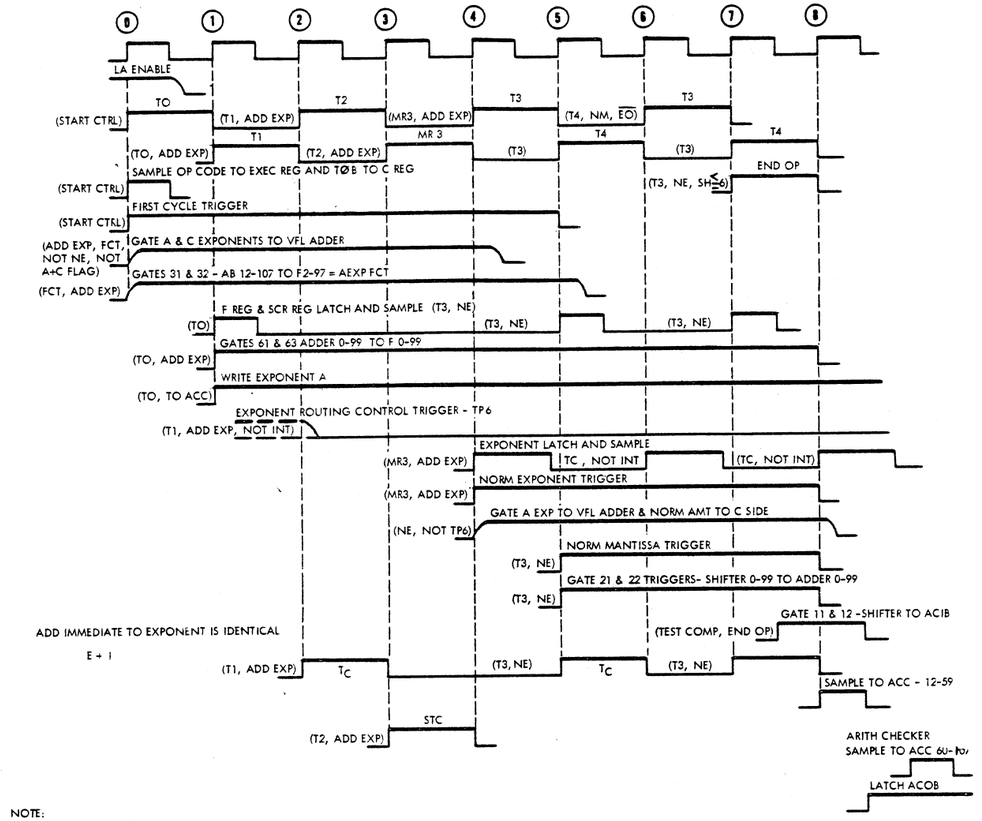


FIGURE 3.8.17. FLOATING-POINT ADD TO EXPONENT (TIMING)

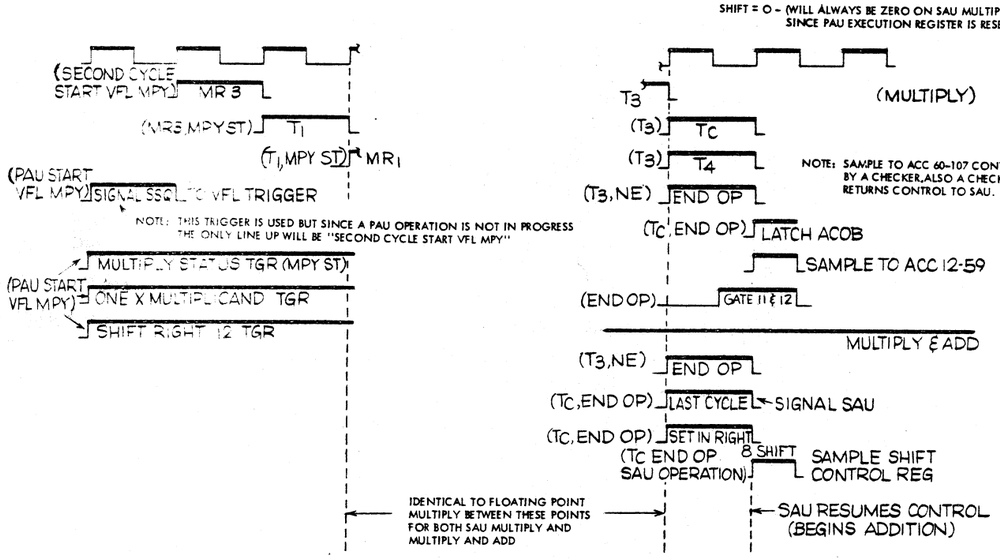


FIGURE 3.8.18. SAU MULTIPLY AND MULTIPLY AND ADD, PAU SECTION (TIMING)

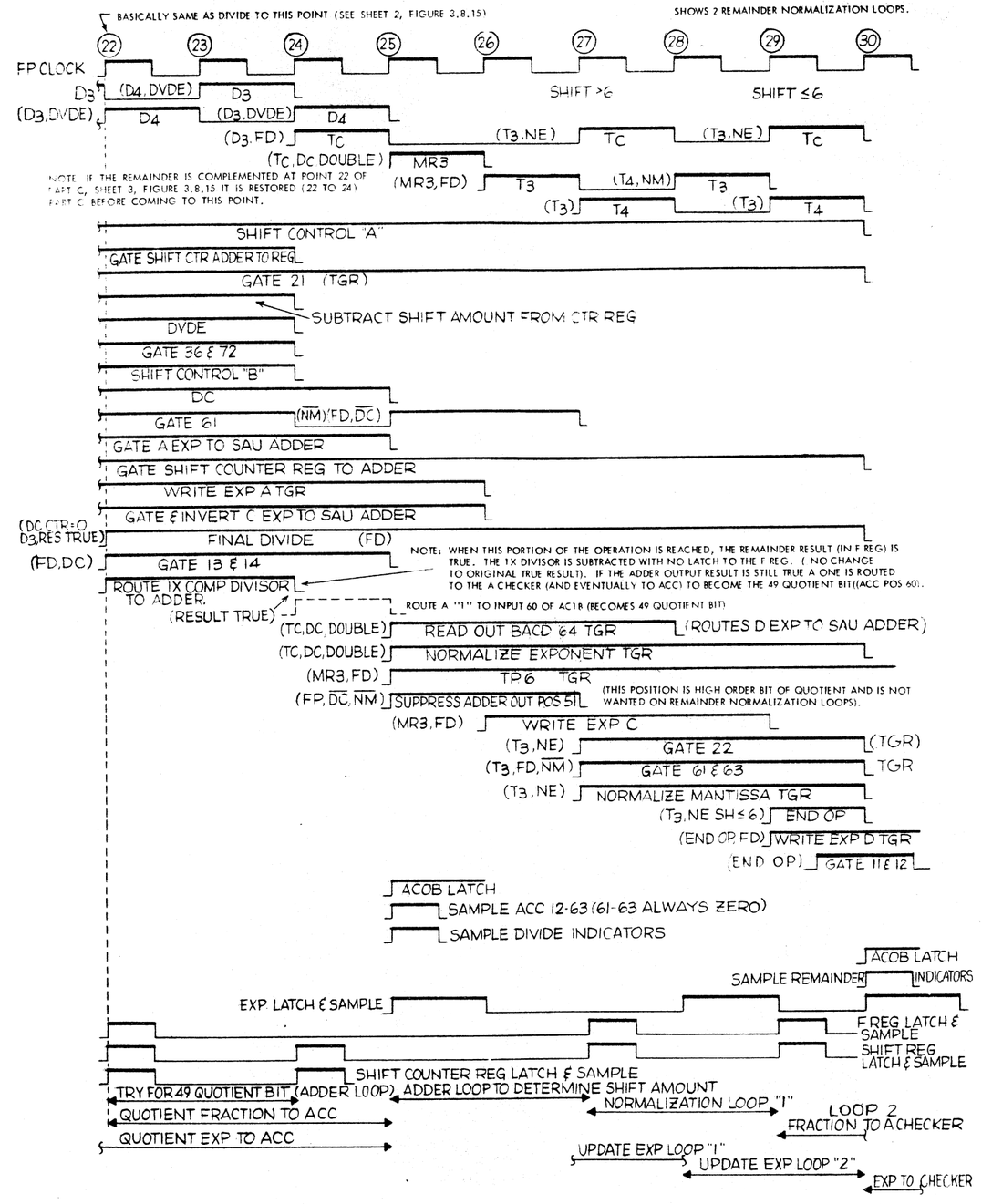


FIGURE 3.8.16. FLOATING-POINT DIVIDE DOUBLE (TIMING)

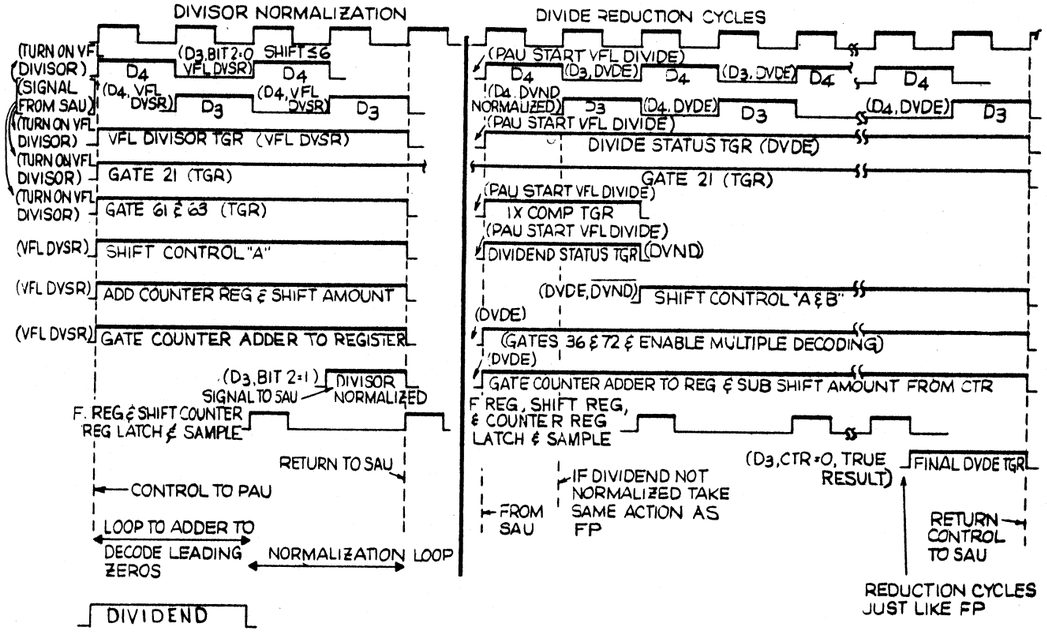


FIGURE 3.8.19. SAU DIVIDE (TIMING)

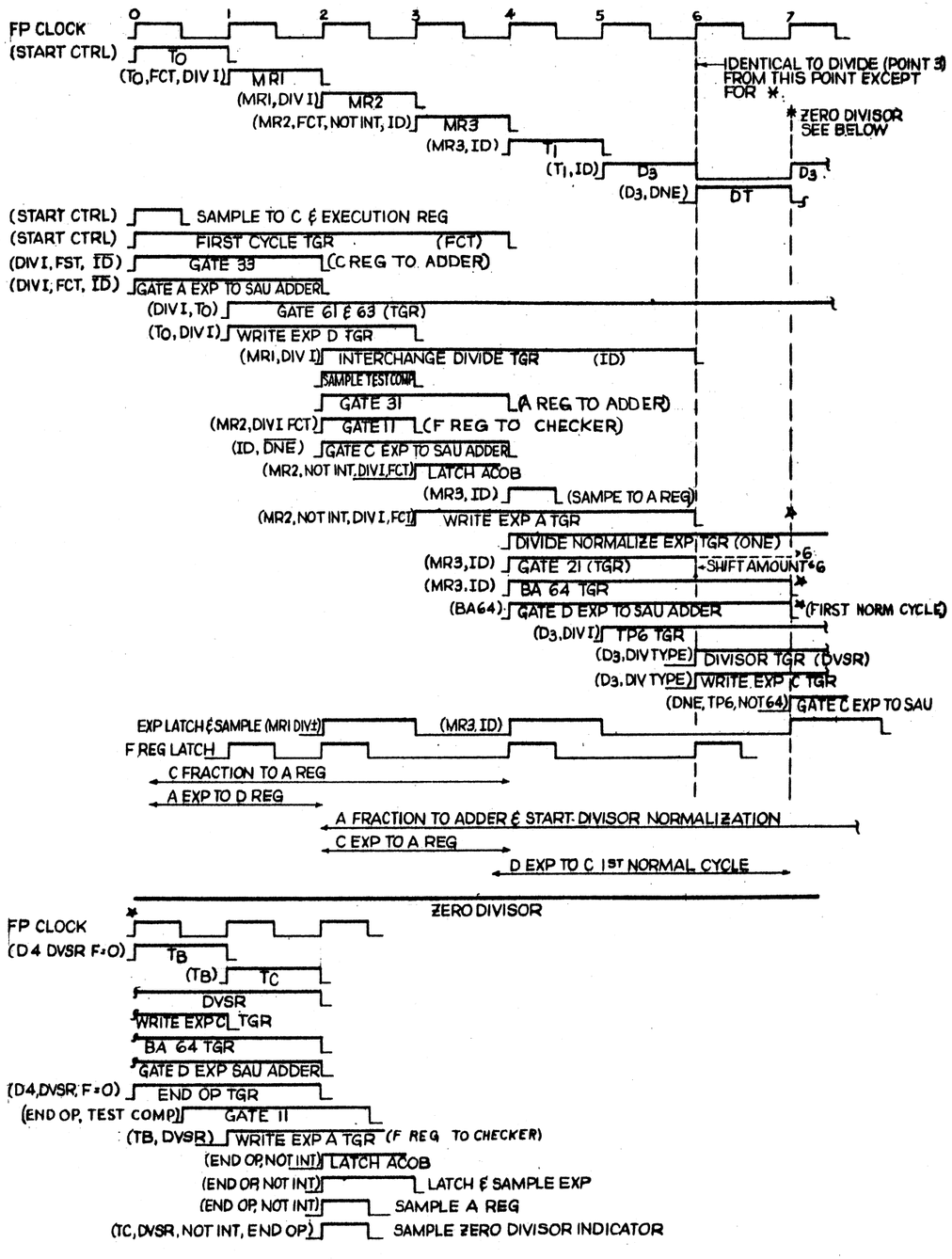


FIGURE 3.8.20. FLOATING POINT RECIPROCAL DIVIDE TIMING

SIGMA ERRORS THAT CAUSE A SCAN

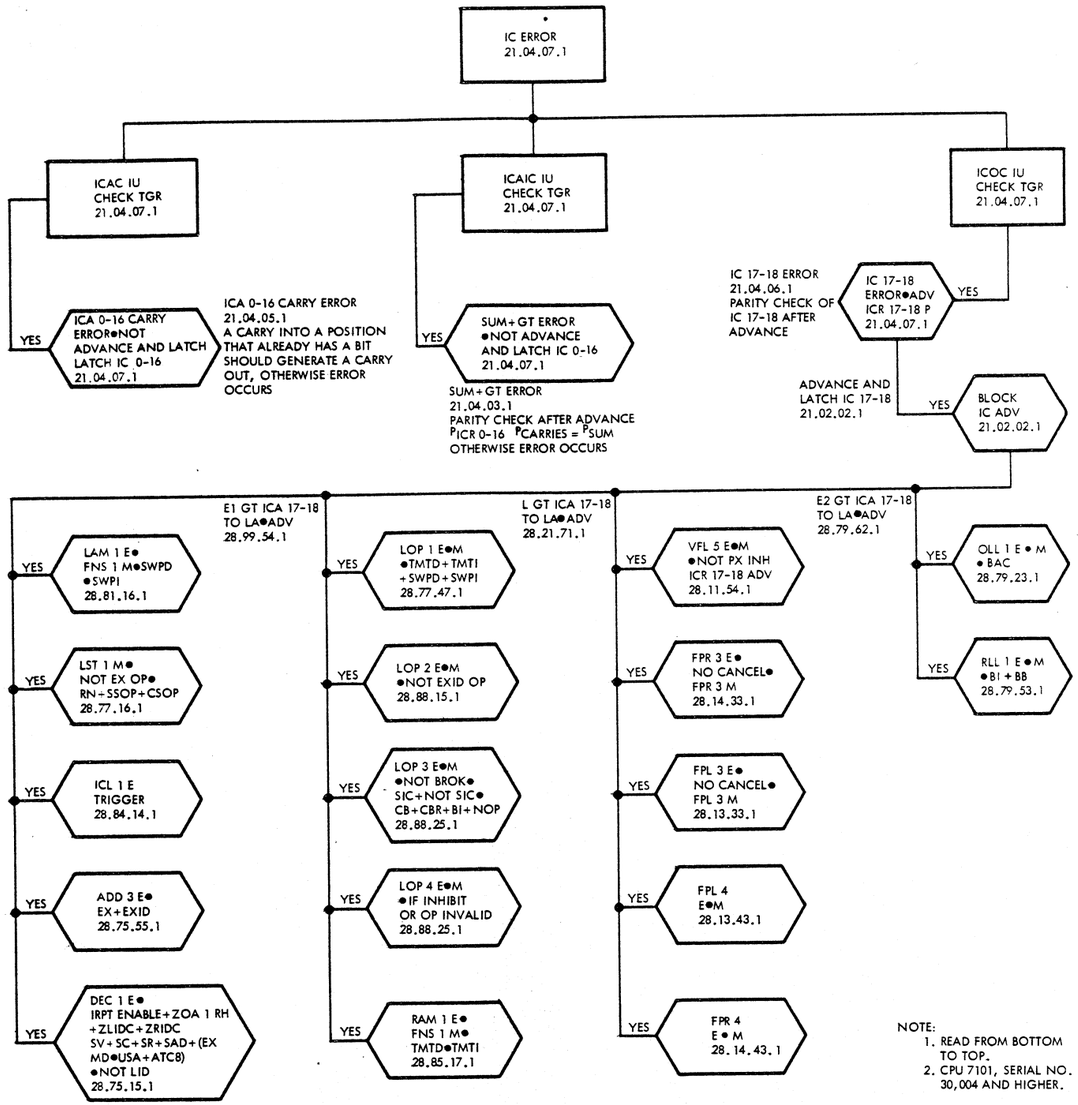
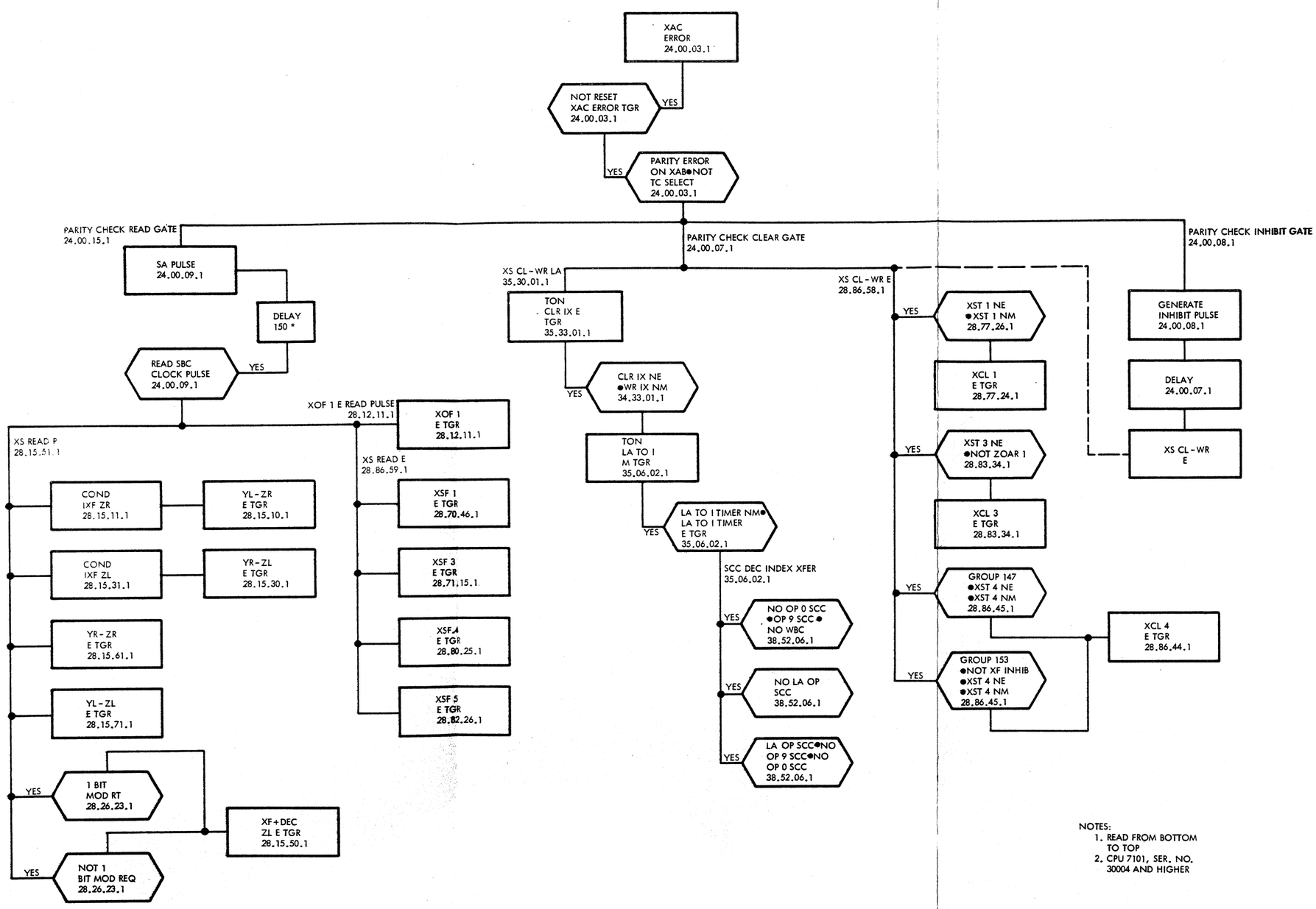


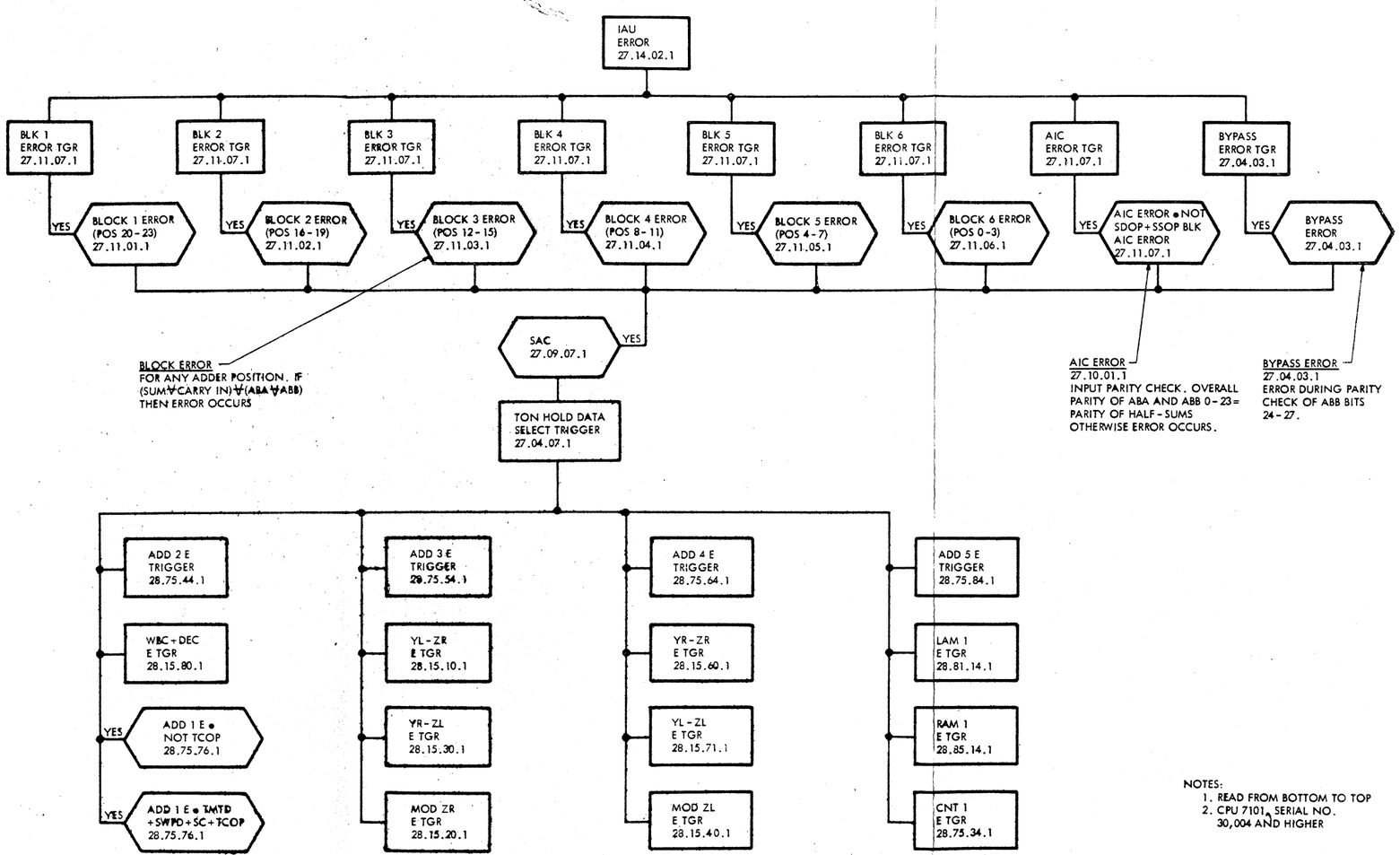
FIGURE 3.9.1. IC ERROR



NOTES:
1. READ FROM BOTTOM TO TOP
2. CPU 7101, SER. NO. 30004 AND HIGHER

FIGURE 3.9.2. XAC ERROR

SIGMA ERRORS THAT CAUSE A SCAN



NOTES:
1. READ FROM BOTTOM TO TOP
2. CPU 7101, SERIAL NO. 30,004 AND HIGHER

FIGURE 3.9.3. IAU ERROR

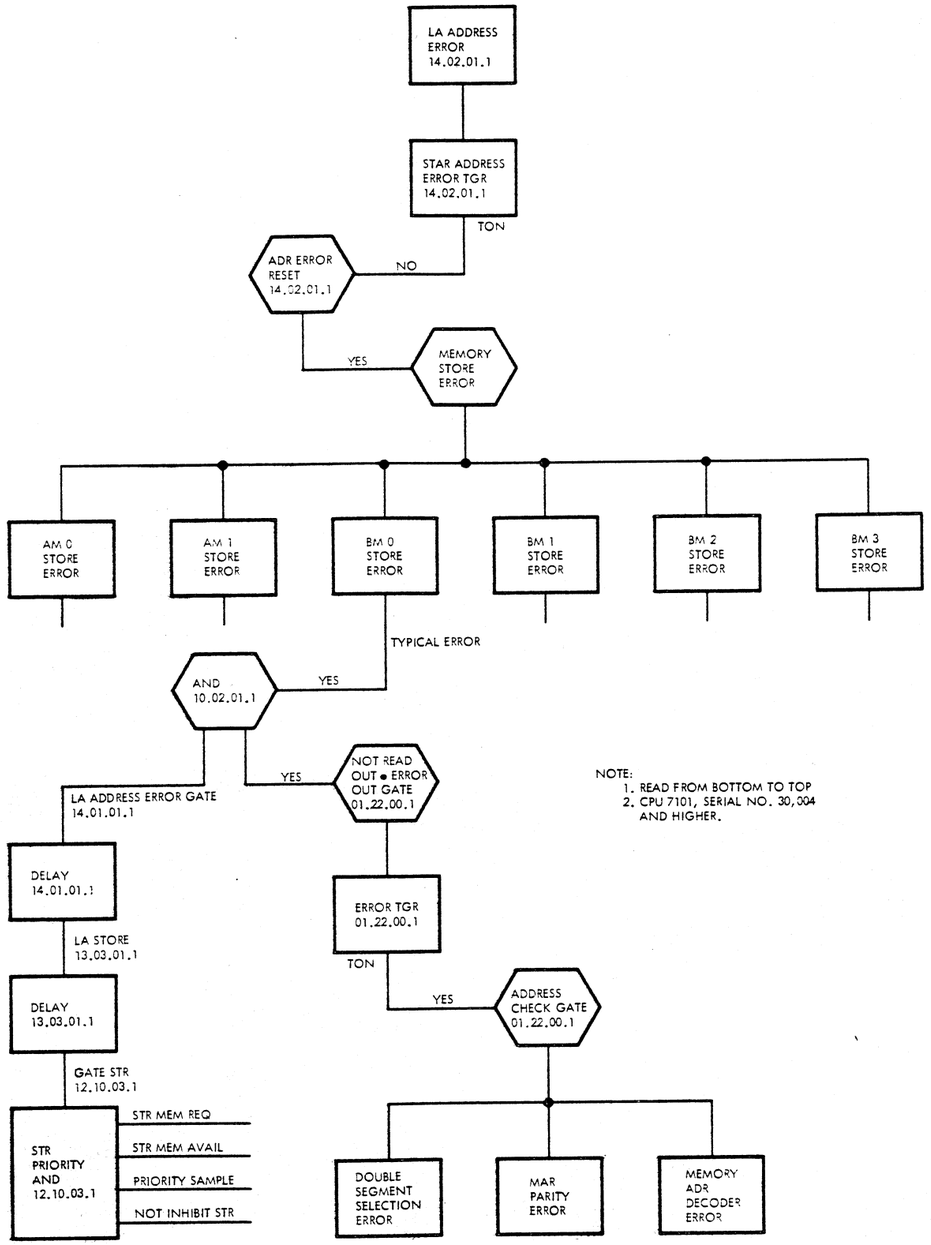
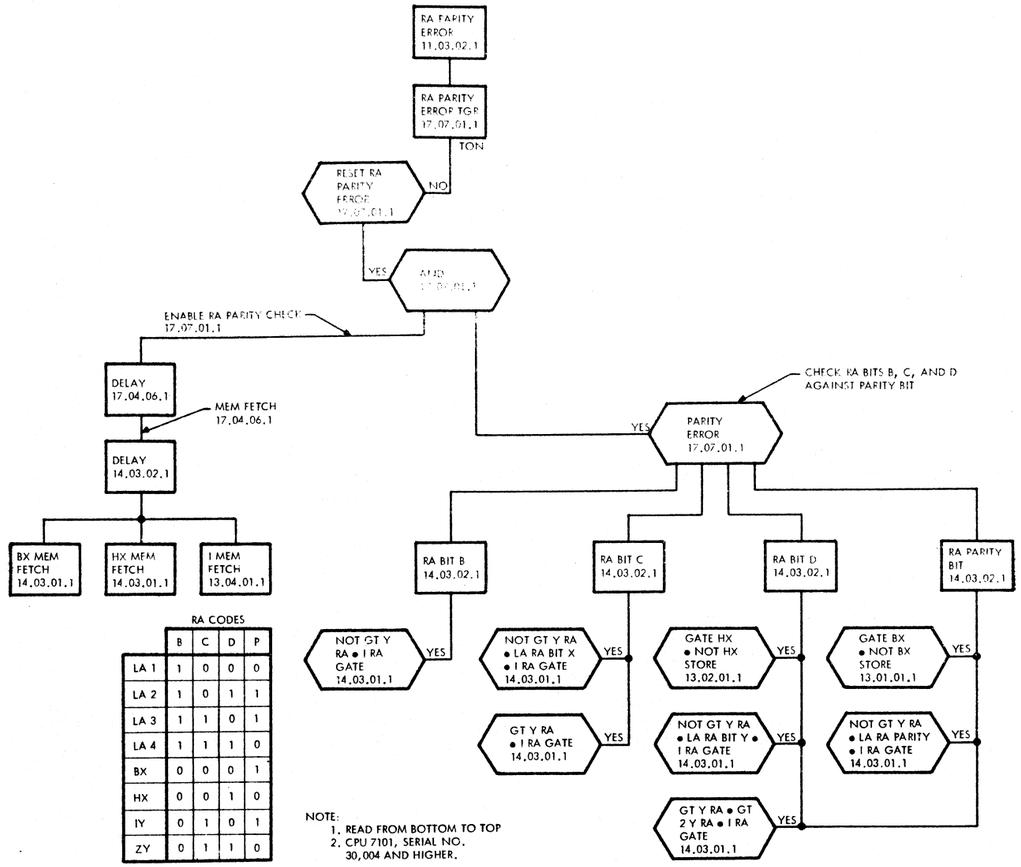
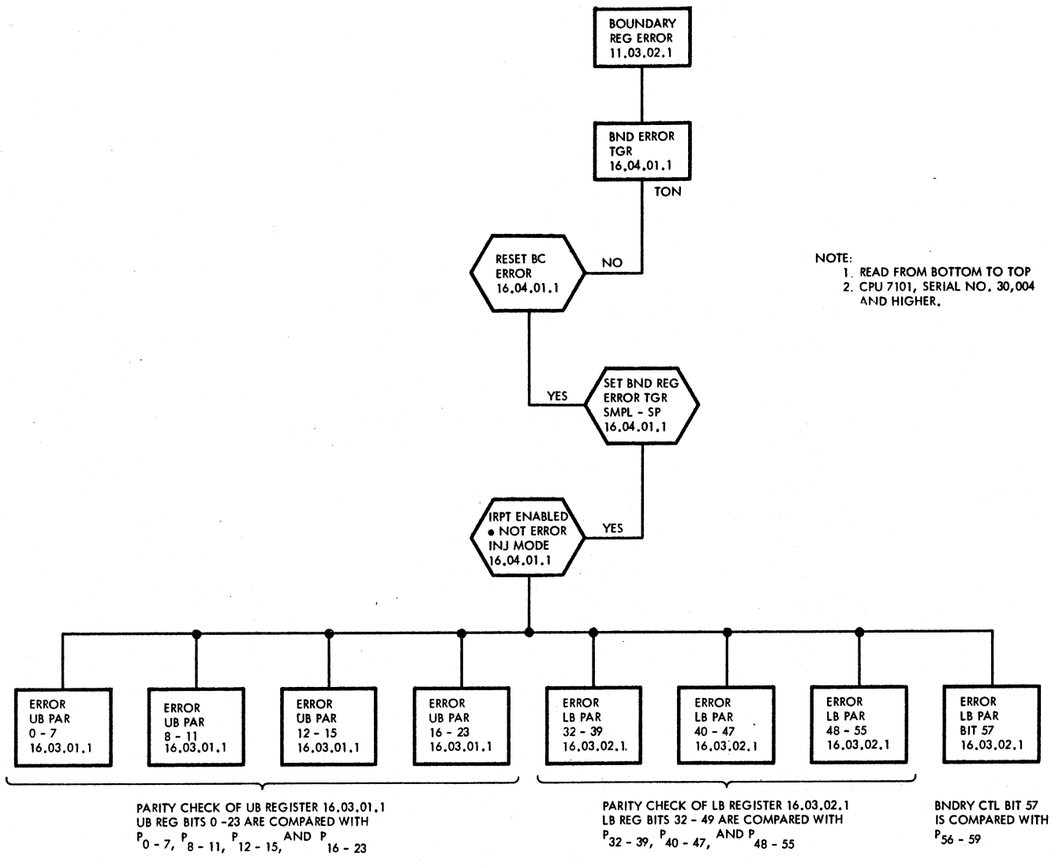


FIGURE 3.9.4. LA ADDRESS ERROR



	B	C	D	P
LA 1	1	0	0	0
LA 2	1	0	1	1
LA 3	1	1	0	1
LA 4	1	1	1	0
BX	0	0	0	1
HX	0	0	1	0
IY	0	1	0	1
ZY	0	1	1	0

FIGURE 3.9.6. RA PARITY ERROR



NOTE:
1. READ FROM BOTTOM TO TOP
2. CPU 7101, SERIAL NO. 30,004 AND HIGHER.

FIGURE 3.9.5. BOUNDARY REGISTER ERROR

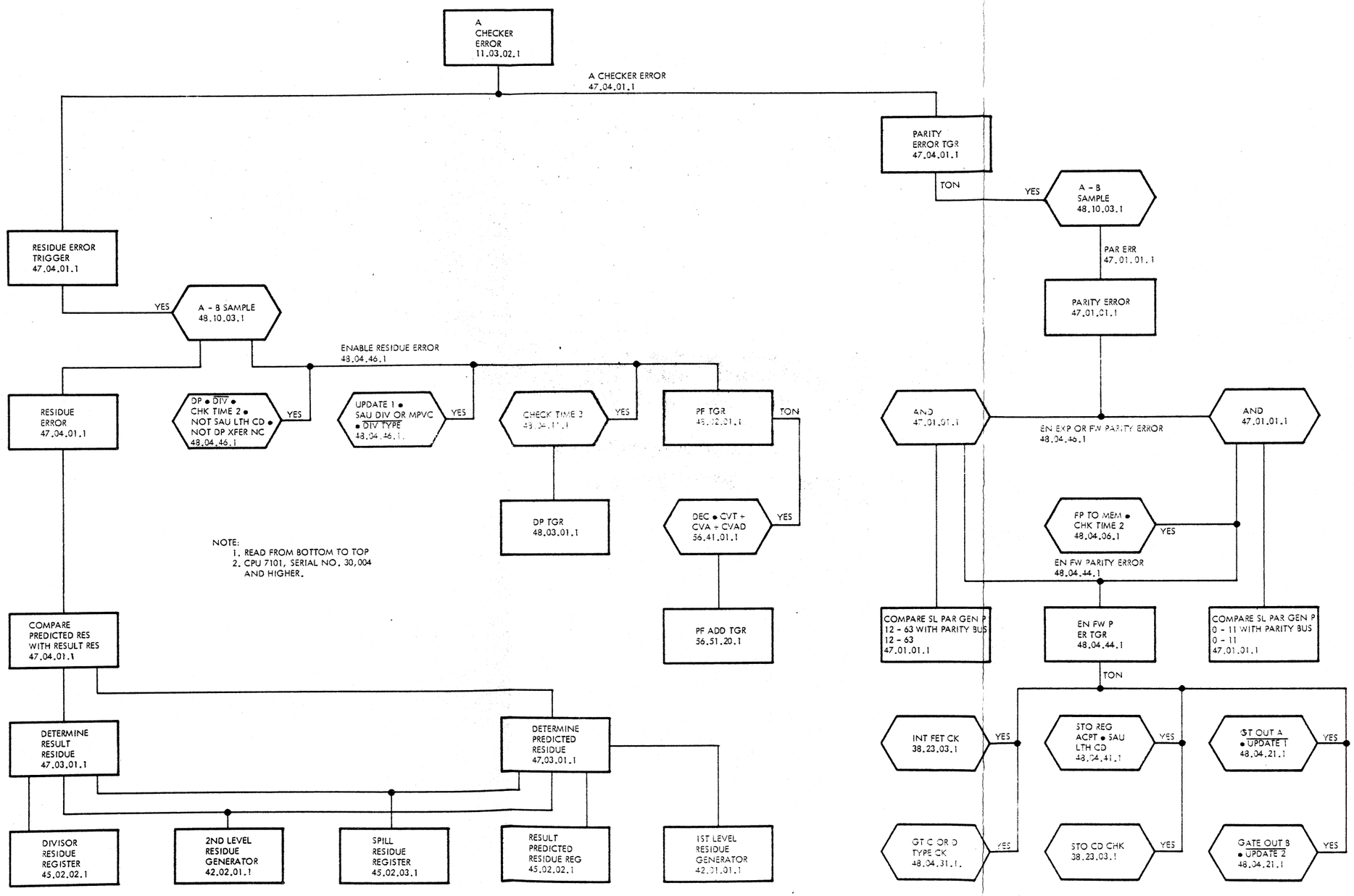


FIGURE 3.9.7. A-CHECKER ERROR

SIGMA ERRORS THAT CAUSE A SCAN

I CHECKER ERROR 11,03,02,1

ALLOW STOP ON SINGLE ERROR 34,08,51,1 — YES

ECC ERROR PERM TGR 34,08,51,1 — TON

NOT ERROR RESET TO I CHKR 34,08,51,1 — YES

LAST HALF CYCLE SAMPLE 34,08,51,1 — YES

CT NOT CTG • LAST HALF CYCLE SAMPLE 34,08,51,1 — YES

ECC ERROR 34,08,41,1

A 58
A 63

ECC ERROR LATCH 34,08,41,1

CO - C32 DO NOT COMPARE WITH COG - C32G (GENERATED ECC) 34,08,41,1

CHK ECC CYC 34,08,21,1

ECC CHK TGR 34,08,51,1 — TON

LAST HALF CYC SAMPLE 34,08,01,1 — YES

CHK ECC 34,08,11,1 — YES

NOT SUPPRESS CHECK • NOT INHIBIT I CHECK IN PROGRESS 34,08,11,1

SUPPRESS CHECK 34,08,11,1 — NO

LA CHECK ECC 35,15,01,1

OPD CHECK E • NM • NO OCC DEC COND MAINT. FETCH 35,15,01,1

RESET ECC ERROR TGR 1 34,08,02,1 — NO

ECC ERROR TEMP TGR 34,08,51,1 — TON

UNCOR ERROR TGR 34,08,51,1 — TON

NOT RESET TO I CHKR • LAST HALF CYCLE SMPL 34,08,51,1 — YES

UNCOR ERROR 34,08,01,1

INHIBIT I CHECK IN PROGRESS • I LAST HALF CORR 34,08,61,1 — NO

ERROR IS UNCORRECTABLE 34,08,61,1 — YES

UNCOR ERROR EXISTS IF ECC ERROR T TGR IS ON HAND AND:
1. CT IS GOOD, OR
2. C0 AND C32 ARE BAD, AND C2,C4, C8 OR C10 ARE BAD.

I CHECK ECC 28,44,14,1

IWC1 CHK ECC 28,41,51,1

IWC 1 E • NM • NOT BLOCK IWC 1 EDD CHK 28,41,23,1 — YES

E2 CHK ECC 28,98,04,1

E1 CHK ECC 28,98,04,1

IWC 2 I CHK ECC 28,41,61,1

IWC 2 E • NM • NOT BLOCK IWC 2 ECC CHK 28,41,61,1 — YES

LDX 4 E • NM • EMF 4 M 2 • BC 2 Y NM • GROUP 150 • USE 2 Y 28,86,36,1 — YES

LDX 6 E • NM • REFILL ADR VALID 28,86,25,1 — YES

LST 3 E • NM • EMF 3 M2 • BC 1 Y NM 28,83,15,1 — YES

LST 4 E • NM • BC 2 Y NM • SWPD + SWPI • EMF 4 M2 28,86,15,1 — YES

CHK 1 E • NM • BC 1 Y NM • USE 1 Y 28,73,15,1 — YES

CHK 1 E • NM • BC 2 Y NM • USE 2 Y 28,73,15,1 — YES

LDX 3 E • NM • GROUP 132 • BC 1 Y NM • EMF 3 M2 28,83,26,1 — YES

LDX 4 E • NM • EMF 4 M 2 • SWPD + SWPI + EX OP + EXID OP • EC 2 Y NM 28,86,36,1 — YES

LDX 4 E • NM • EMF 4 M 2 • BC 1 Y NM • USE 1 Y • GROUP 150 28,86,36,1 — YES

LDX 5 E • NM • SIC VALID ADR 28,87,15,1 — YES

I PARITY ERROR TGR 34,08,51,1 — TON

NOT RESET TO I CHKR • LAST HALF CYCLE SMPL 34,08,51,1 — YES

AND 34,08,41,1 — YES

ENABLE I PARITY ERROR 34,08,21,1

A 49
A 60

I PARITY ERROR LATCH 34,08,41,1

PARITY OF BITS 0 - 63 DO NOT AGREE WITH P BITS 66 - 73 34,08,41,1

I CHK PARITY TGR 34,08,21,1 — TON

LAST HALF CYCLE SMPL 34,08,21,1 — NO

I CHK PARITY 34,08,11,1 — YES

NOT SUPPRESS CHECK • NOT INHIBIT I CHECK IN PROGRESS 34,08,11,1

I CHK PARITY 28,98,07,1

LDX 1 E • NM • GROUP 104 28,75,26,1 — YES

LDX 3 E • NM • SWPD + SWPI • EMF 3 NM 2 28,83,26,1 — YES

LDX 4 E • NM • EMF 4 NM 2 28,86,36,1 — YES

LST 1 E • NM • GROUP 124 28,77,16,1 — YES

LST 3 E • NM • EMF 3 NM 2 28,83,15,1 — YES

LST 4 E • NM • EMF 4 NM 2 • SWPD + SWPI 28,86,15,1 — YES

CHK 4 E • NM 28,80,44,1 — YES

CHK 5 E • NM • NOT LID 28,82,45,1 — YES

CHK 6 E • NM 28,70,64,1 — YES

CHK 8 E • NM 28,72,24,1 — YES

LOP 3 E • NM • COND REAL EXT STO LA LEVEL 28,88,26,1 — YES

ADD 5 E • NM • ZLXA 28,75,85,1 — YES

LA PARITY ERROR TGR 34,08,51,1 — TON

NOT RESET TO I CHKR • LAST HALF CYCLE SAMPLE 34,08,51,1 — YES

LA PARITY ERROR 34,08,41,1

AND 34,08,21,1 — YES

ENABLE LA PARITY ERROR 34,08,21,1

A 51
A 56

LA PARITY ERROR LATCH 34,08,41,1

PARITY OF BITS 0 - 63 DO NOT AGREE WITH P BITS 64 - 72 34,08,41,1

LA CHECK PARITY TGR 34,08,21,1 — TON

LAST HALF CYCLE SAMPLE 34,08,01,1 — NO

SUPPRESS CHECK 34,08,11,1 — NO

LA CHECK PARITY 35,15,01,1

LA TO I TIMER E • NM 35,15,01,1

I CHECK PARITY 28,21,75,1

FPR 2 E • NM • ZR XS LTH • ZR NOT ADDR 8 LTHD 28,14,22,1 — YES

FPR 4 E • NM • FPR CL 1 + 2 ZRXS • ZR NOT ADDR 8 LTHD 28,14,42,1 — YES

VFL 1 E • NM 28,11,12,1 — YES

VFL 3 E • NM • COND VFL 3 TYPE 1 8 28,11,32,1 — YES

VFL 5 E • NM • COND VFL 5 TYPE 1 8 + 1 C 28,11,53,1 — YES

FPL 2 E • NM • ZL X S LTH • ZL NOT ADDR 8 LTHD 28,13,33,1 — YES

FPL 4 E • NM • ZL XS FPL EL 1 + 2 • ZL NOT ADDR 8 LTHD 28,13,42,1 — YES

VFL 2 E • NM • ZL XS LTH 28,11,22,1 — YES

VFL 4 E • NM • COND VFL 4 TYPE 1 28,11,42,1 — YES

I CHECK PARITY E 2 28,79,63,1

OLL 1 E • NM 28,79,22,1 — YES

FLL 1 E • NM • BB AND ZLXS 28,79,34,1 — YES

RLL 1 E • NM 28,79,54,1 — YES

I P CHECK PARITY 28,15,42,1

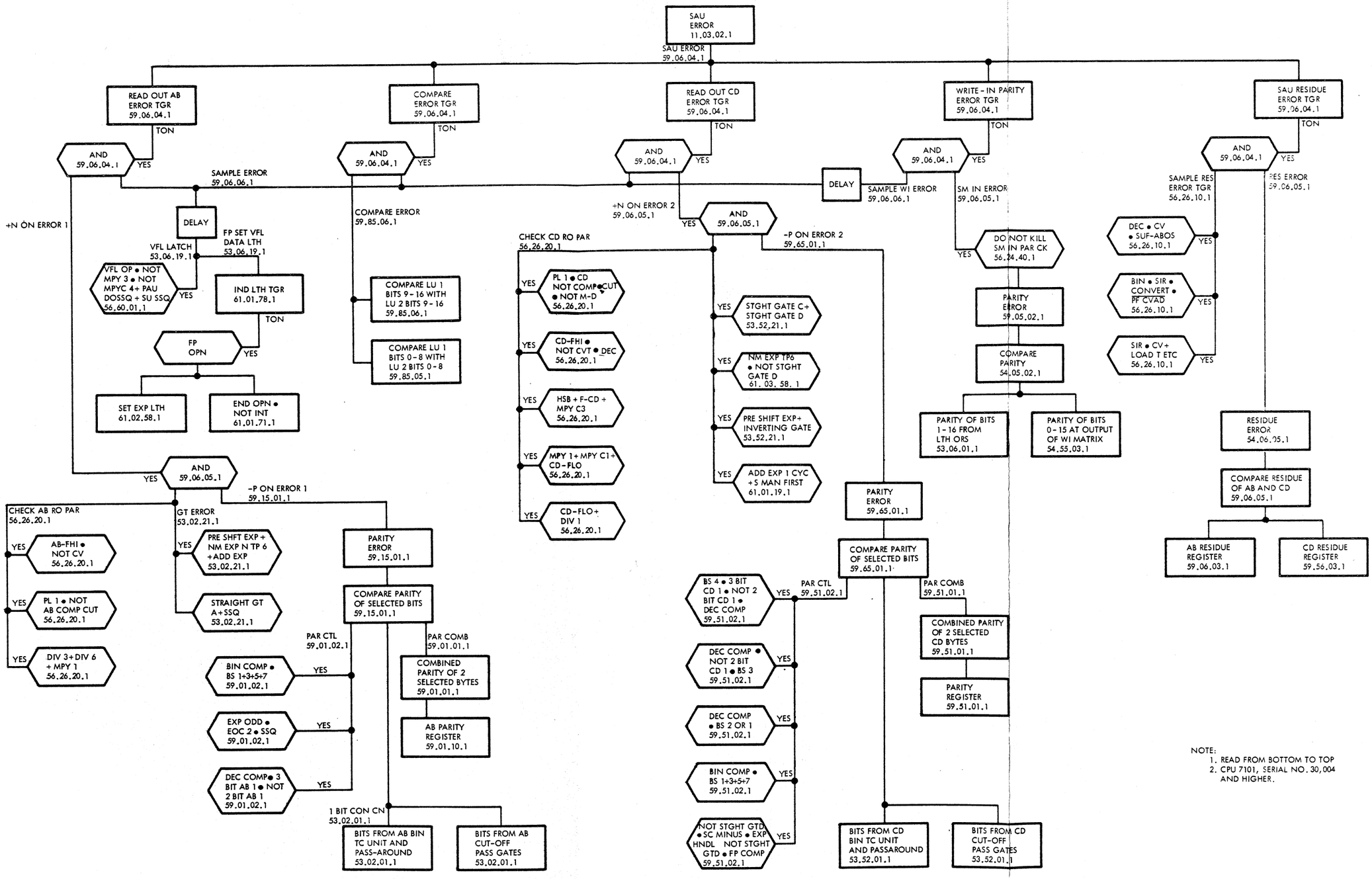
MOD ZL M TGR 28,15,42,1 — NO

MOD ZLE • PX Y • FW NOT S • XF + DEC ZL M 28,15,42,1 — YES

NOTE:
1. READ FROM BOTTOM TO TOP
2. CPU 7101, SERIAL NO. 30,004 AND HIGHER.

FIGURE 3.9.8. I-CHECKER ERROR

SIGMA ERRORS THAT CAUSE A SCAN



NOTE:
1. READ FROM BOTTOM TO TOP
2. CPU 7101, SERIAL NO. 30,004 AND HIGHER.

FIGURE 3.9.9. SAU ERROR

TEST EQUIPMENT, TOOLS, AND MAINTENANCE SUPPLIES REQUIRED TO TEST TUNNEL DIODE ARRAY

Test Equipment	Part No.
Vacuum Tube Voltmeter	5231703
Preamplifier, Oscilloscope, Sampling Tektronix Type N	5231736
Probe, Oscilloscope, Tektronix P6025	5231737
Test Set, Transistor Curve Tracer Tektronix Type 575	5231792
Oscilloscope, Tektronix Type 555	523004
Preamplifier Type B	460998
Preamplifier Type CA	460999

Tools	
Tweezer	801908
Soldering Iron (1/8-inch tip)	5230119
Brush, Acid	2108025
Pliers, Chain Nose, 5-inch	450786
Pliers, Diagonal Cutting, 4-inch	5230009
Loupe, 5-power	450785
Jig Assembly, Card Holding	5230007
Needle, Ground off Hypodermic	Local Purchase
Safety Can	Local Purchase
Toothpicks, Round	Local Purchase
Screwdriver, Jeweler 0.007-inch Blade	2108286

Maintenance Supplies	
Fuse, 1/20 ampere	361575
Solder	2102023
Wire 22 PVC Yellow, Bulk	556332
Flux	5230037
Adhesive Epoxy	5230042
Wire 26	523283
Wire 28	595036

Maintenance Supplies (cont'd)

	Part No.
Board Assembly, Tunnel Diode Memory	361572
Segment, Wire Wound Line	361574
Board, Connector	361555
Diode, Tunnel	361564
Cell, Memory (Field Replacement)	361575
Flux	5230037
*Solvent	As furnished
*Sleeving	177285
*Finished Bar Stock 0.050-inch hex	5246694

*A tuning tool should be made from the finished bar stock. Using about six inches of the bar stock, slip a 6-inch piece of sleeving which has been expanded in the solvent over the bar stock so that a minimum of 1/4 inch of the bar stock is exposed and about 1/8 inch of the sleeving extended over the other end of the bar stock; then let sleeving dry. If a larger handle is required, a radio knob with a setscrew may be applied to the insulated portion of the bar stock. Note: Mark the sleeving or radio knob so that a precise count may be made of the number of turns while turning.

This tool is absolutely necessary for tuning.

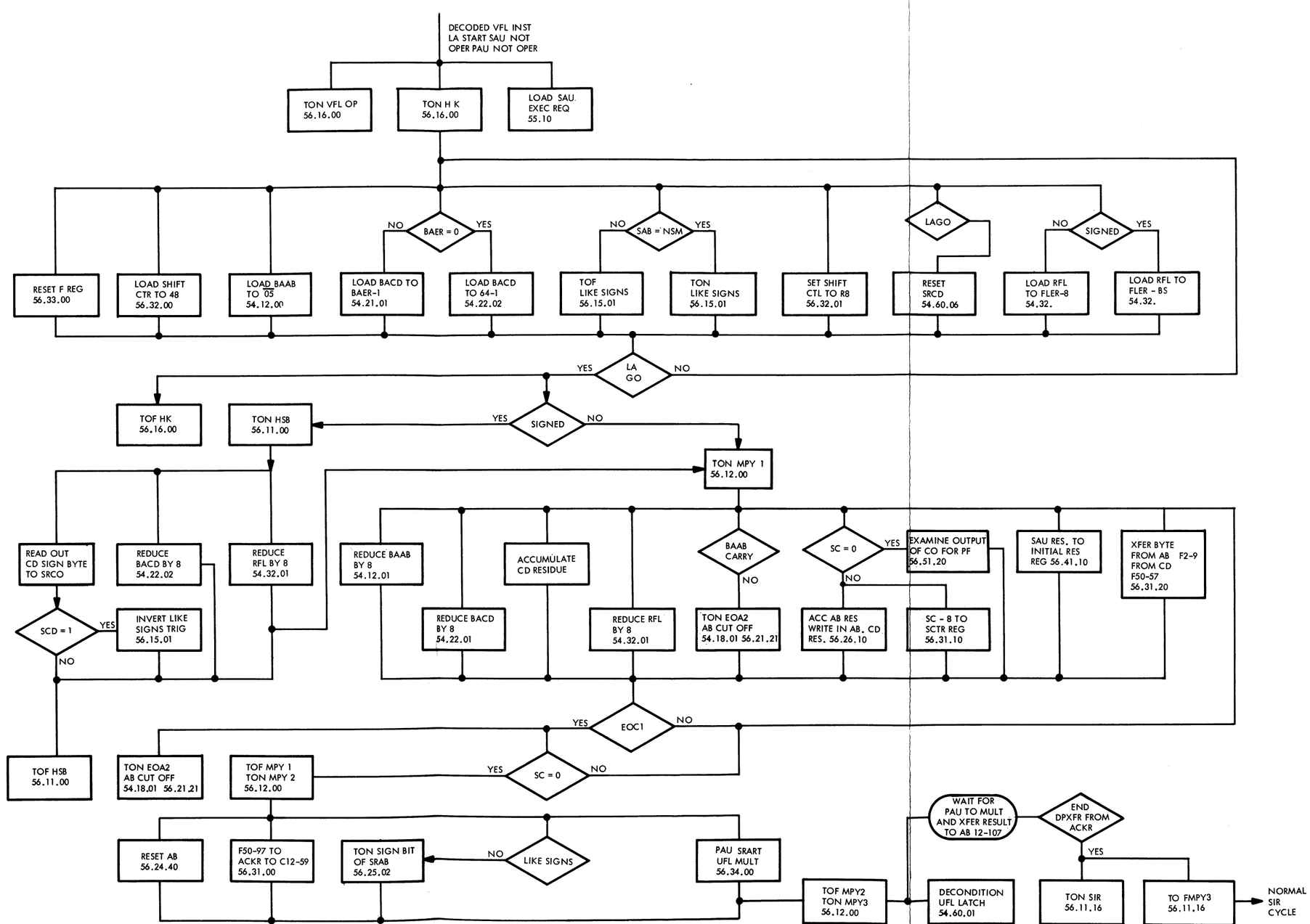


FIGURE 3.11.1. BINARY MULTIPLY

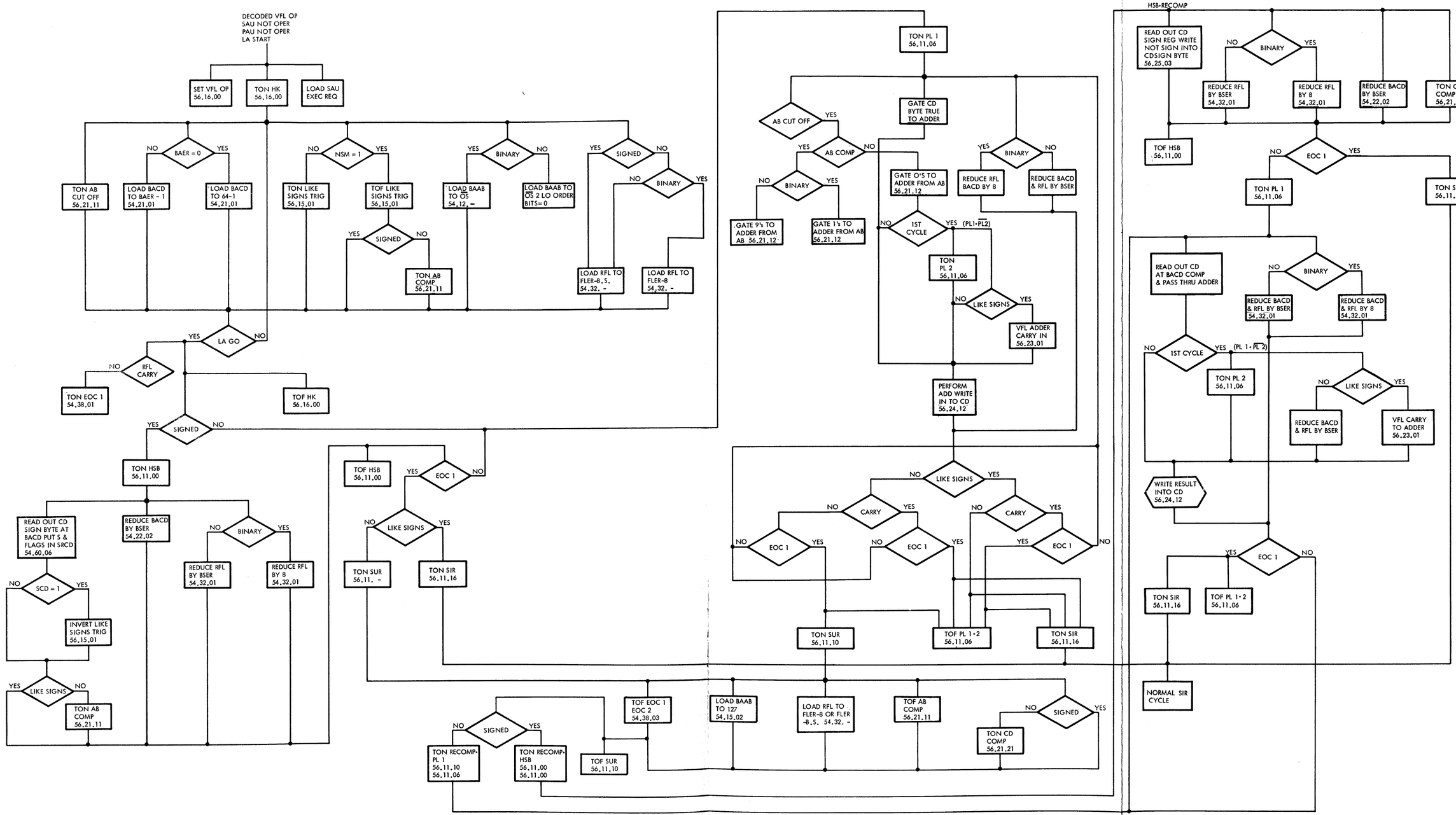


FIGURE 3.11.2. VFL ADD 1 TO MEMORY

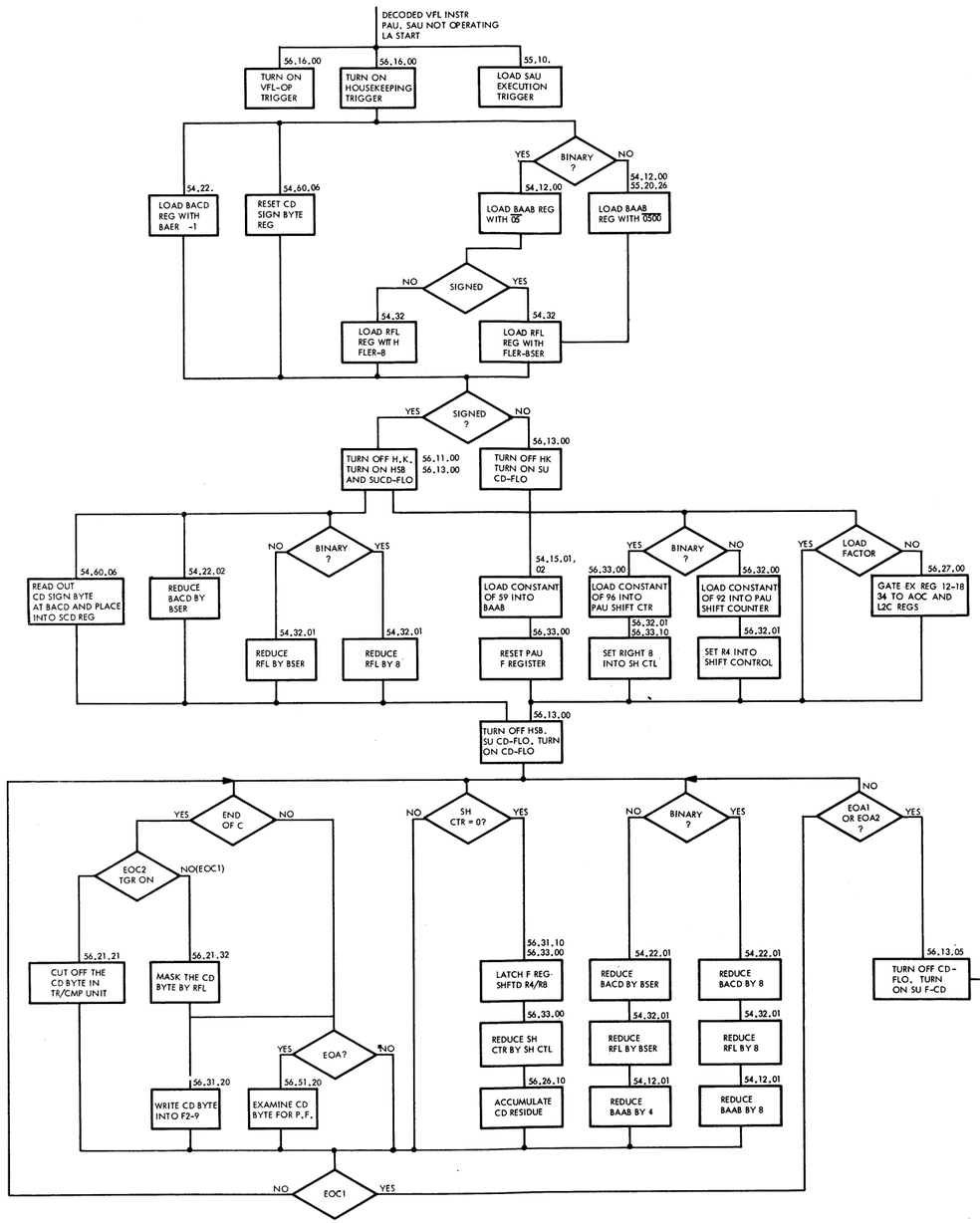


FIGURE 3.11.3. VFL LOAD TRANSIT AND SET, DECIMAL MULTIPLY, DECIMAL MULTIPLY AND ADD, DECIMAL DIVIDE, OR LOAD FACTOR

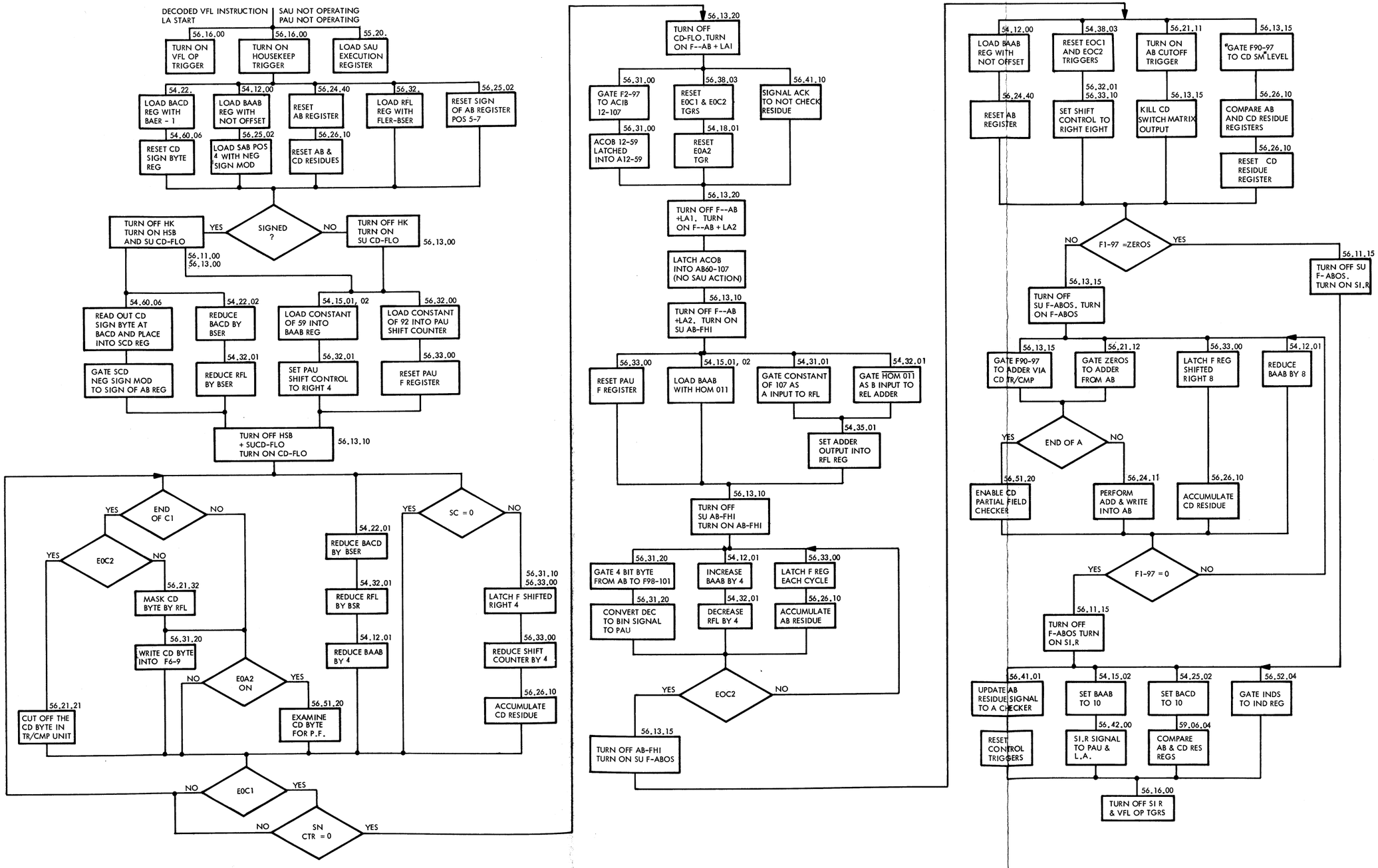


FIGURE 3.11.4. VFL LOAD CONVERTED DECIMAL TO BINARY

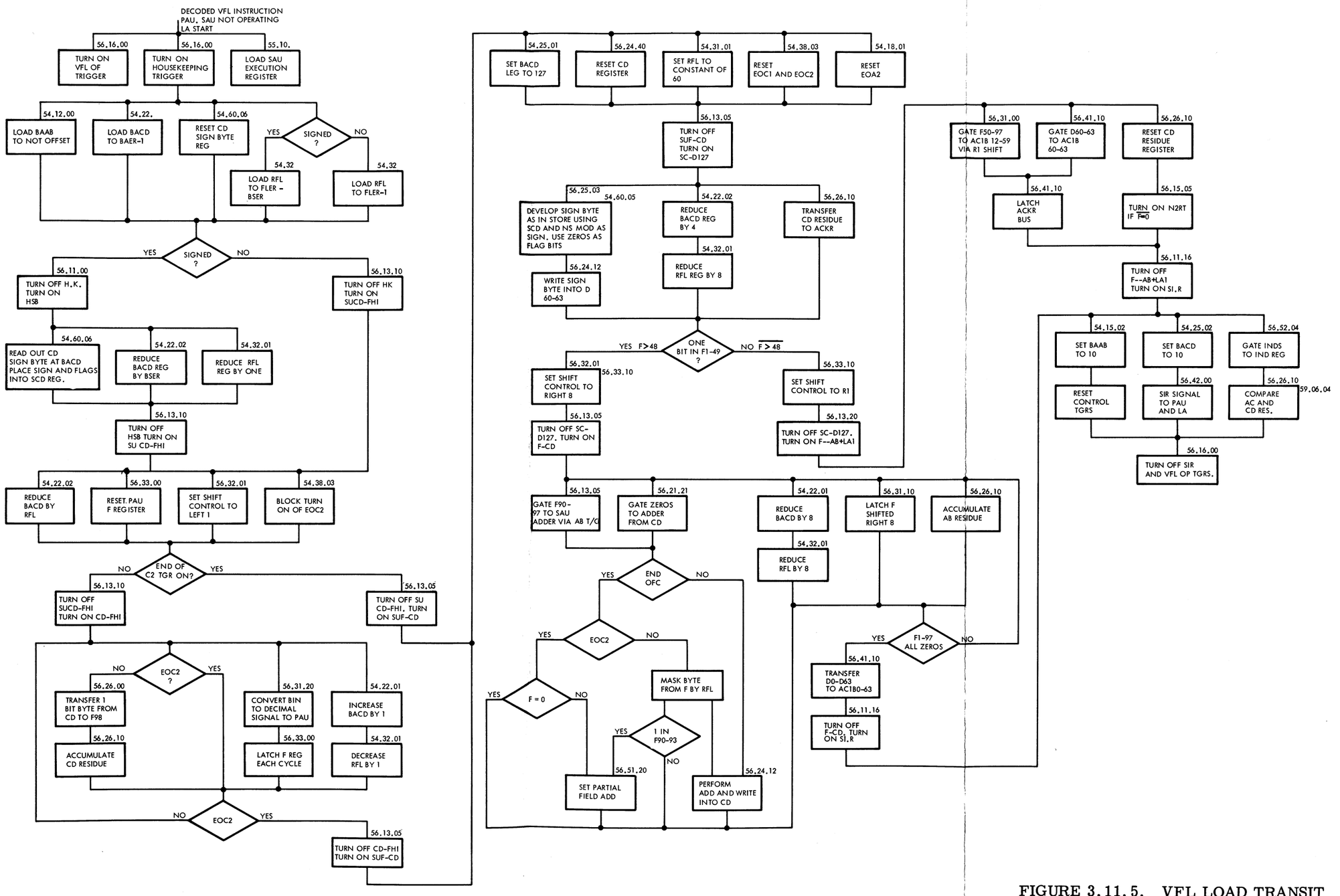
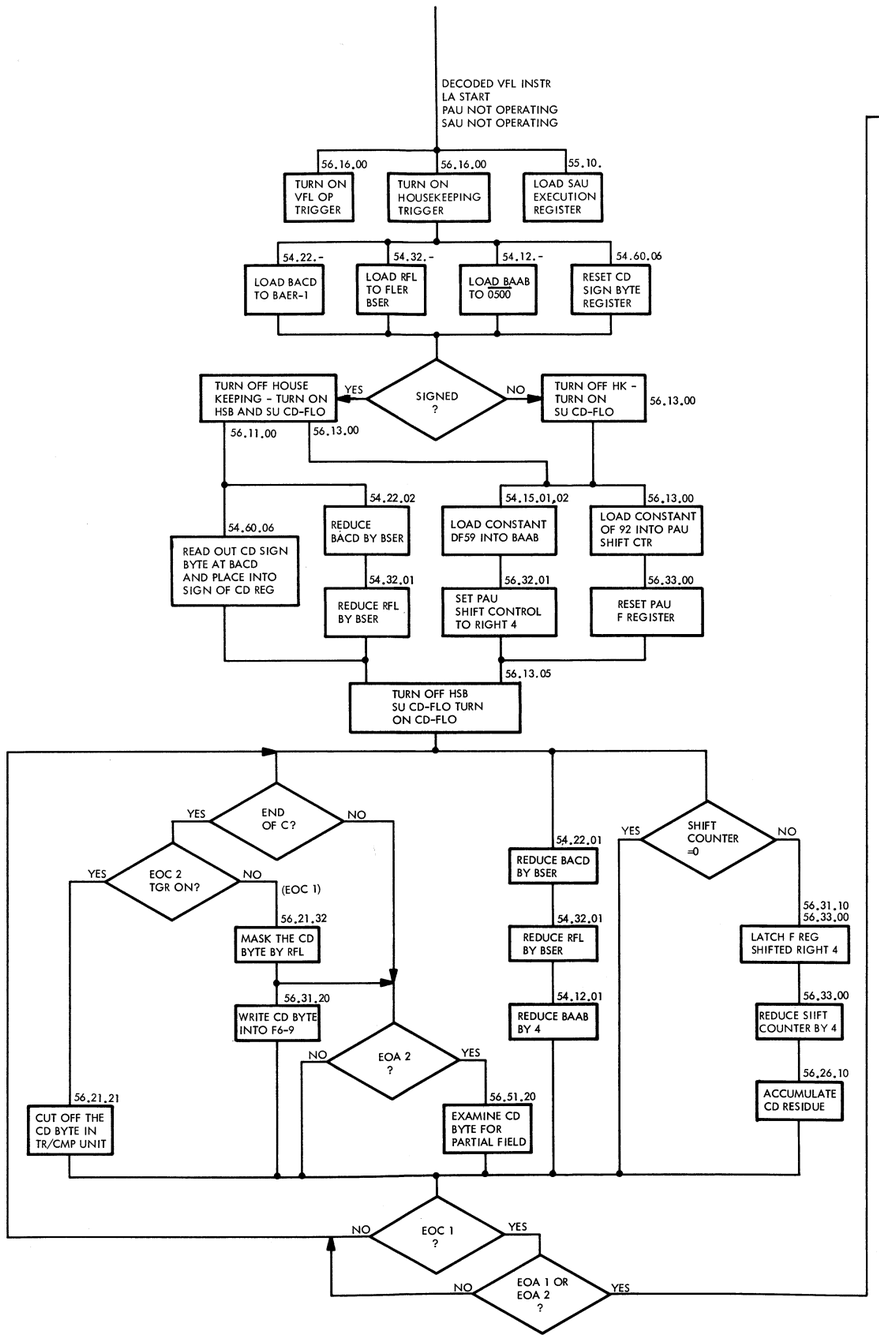
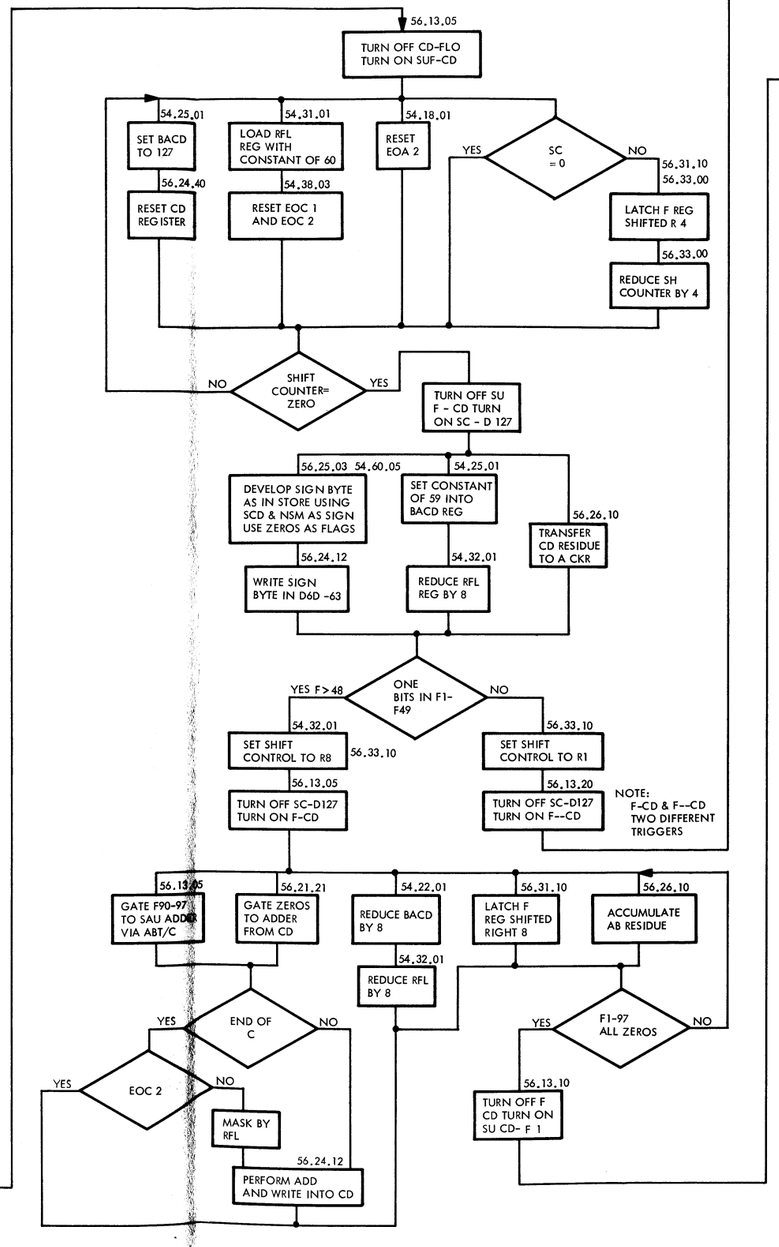


FIGURE 3.11.5. VFL LOAD TRANSIT CONVERTED BINARY TO DECIMAL





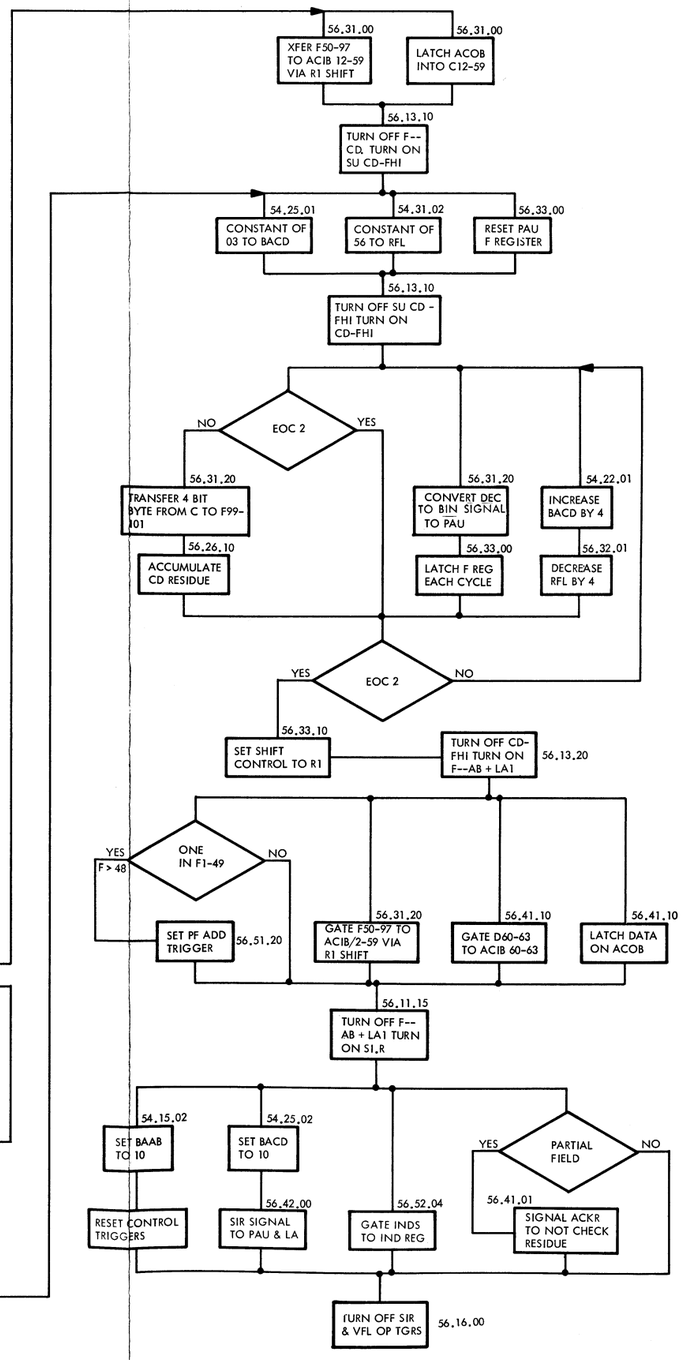


FIGURE 3.11.6. VFL LOAD TRANSIT CONVERTED DECIMAL TO BINARY

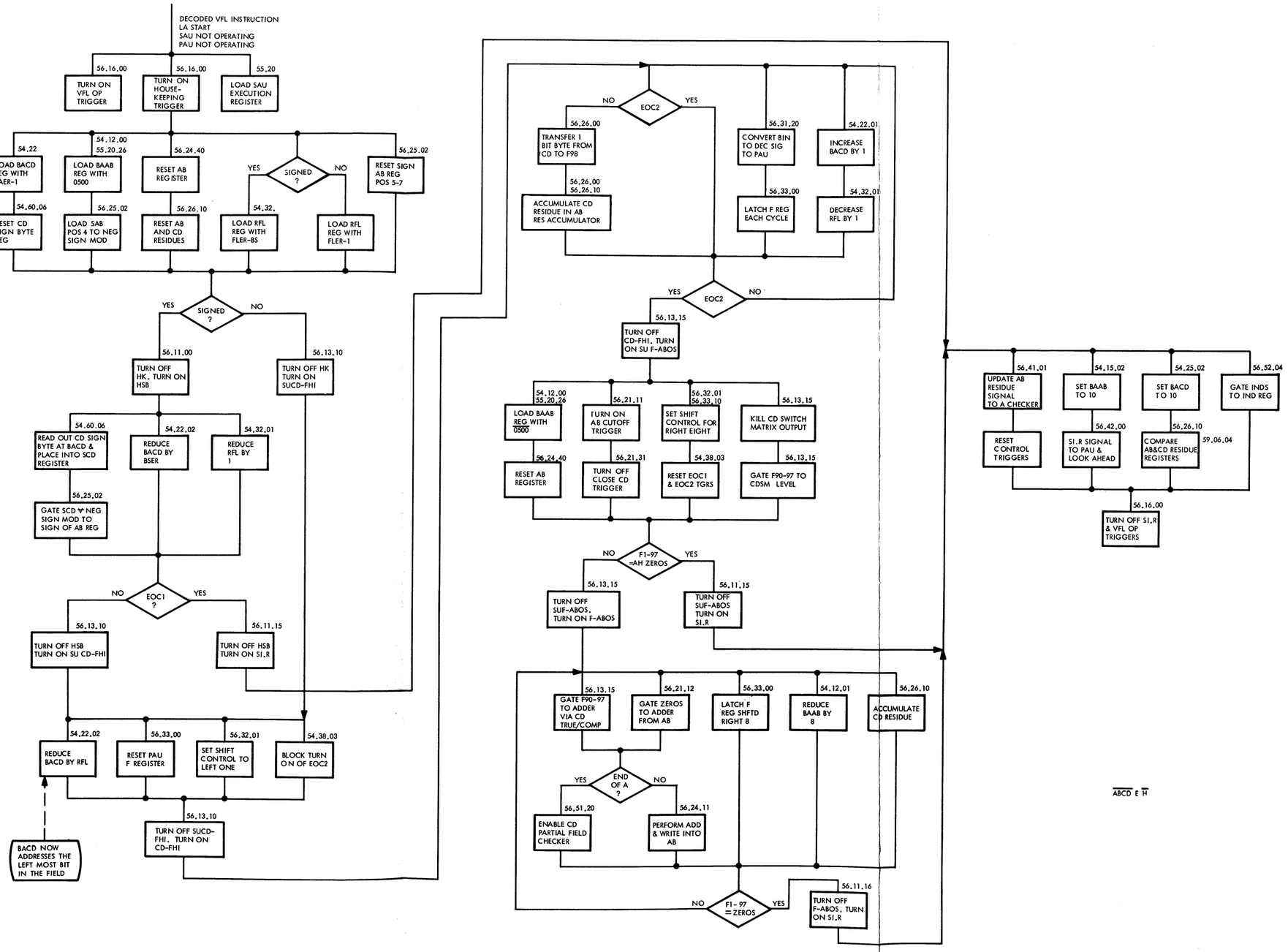


FIGURE 3.11.7. VFL LOAD CONVERTED BINARY TO DECIMAL

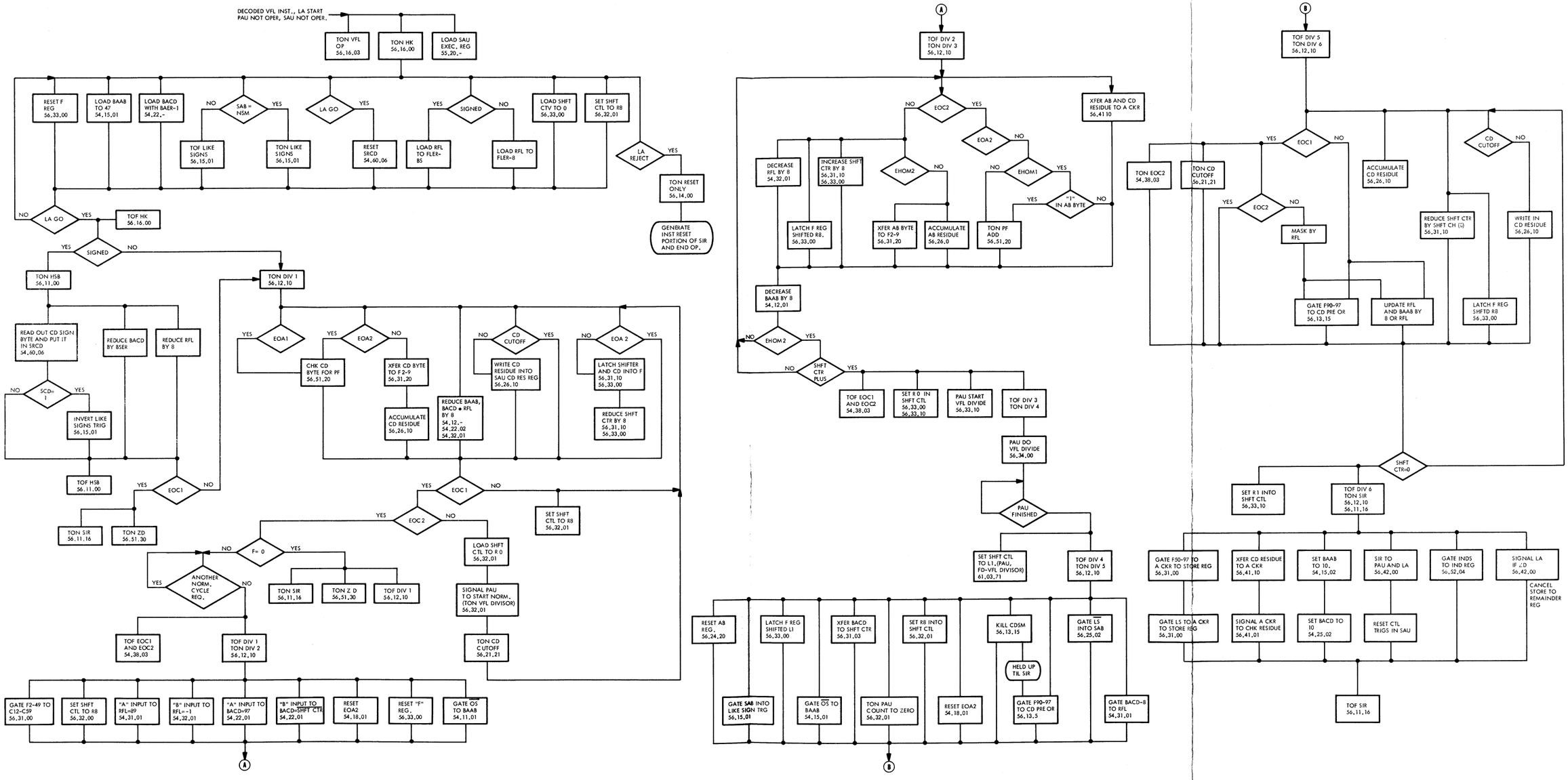


FIGURE 3.11.8. BINARY DIVIDE

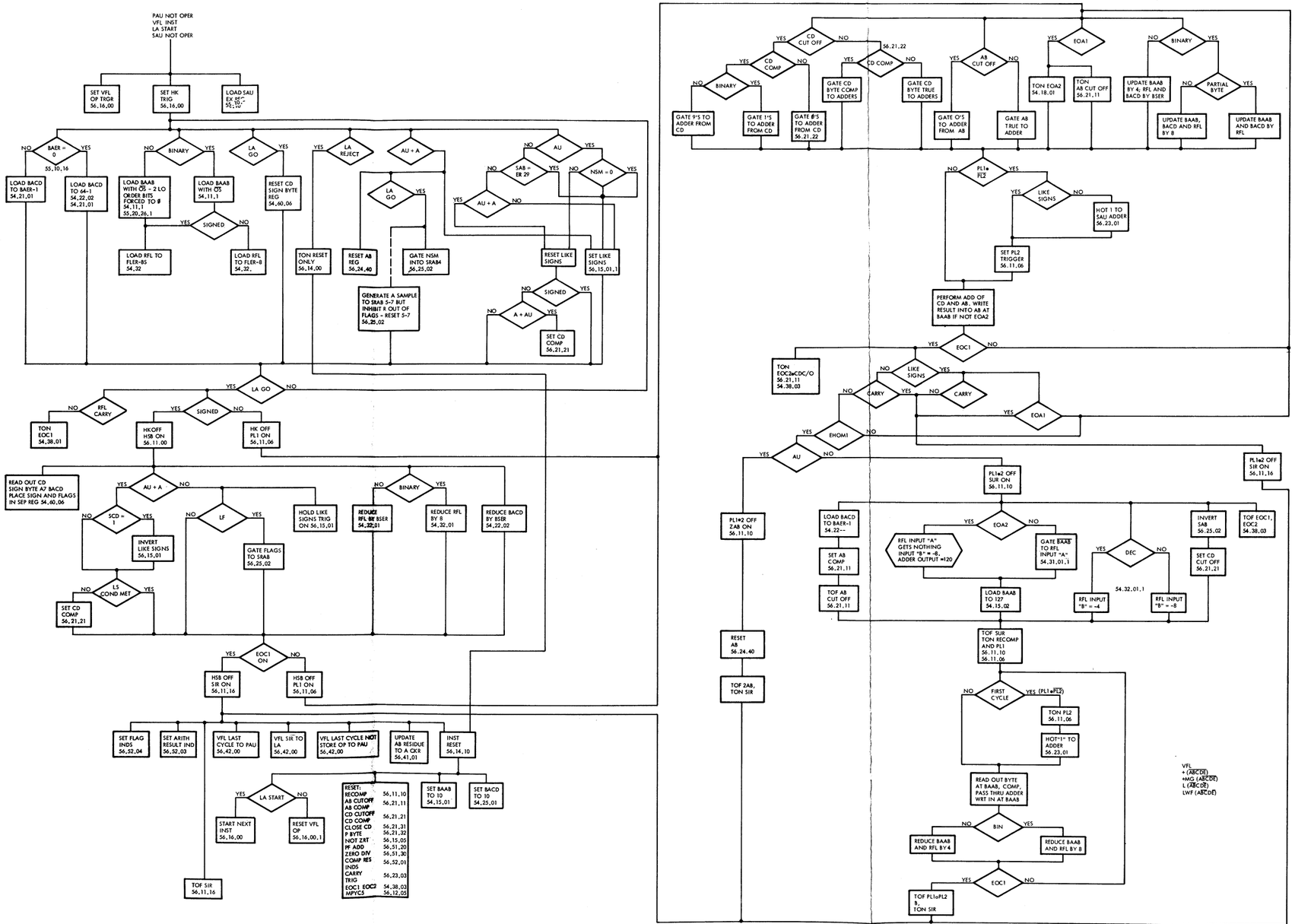


FIGURE 3.11.9. VFL ADD, ADD TO MAGNITUDE, LOAD, OR LOAD WITH FLAGS

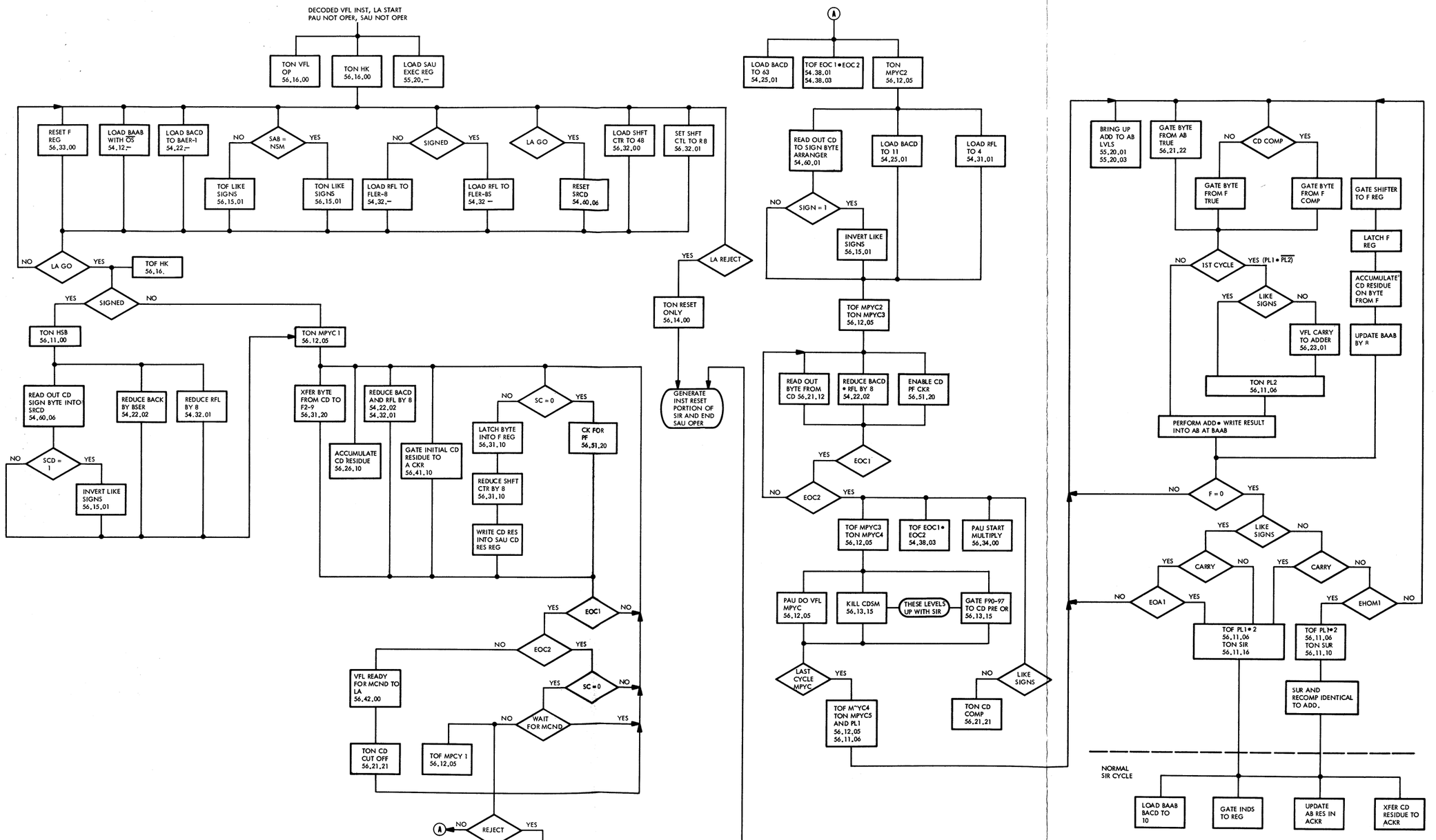


FIGURE 3.11.10. BINARY MULTIPLY AND ADD

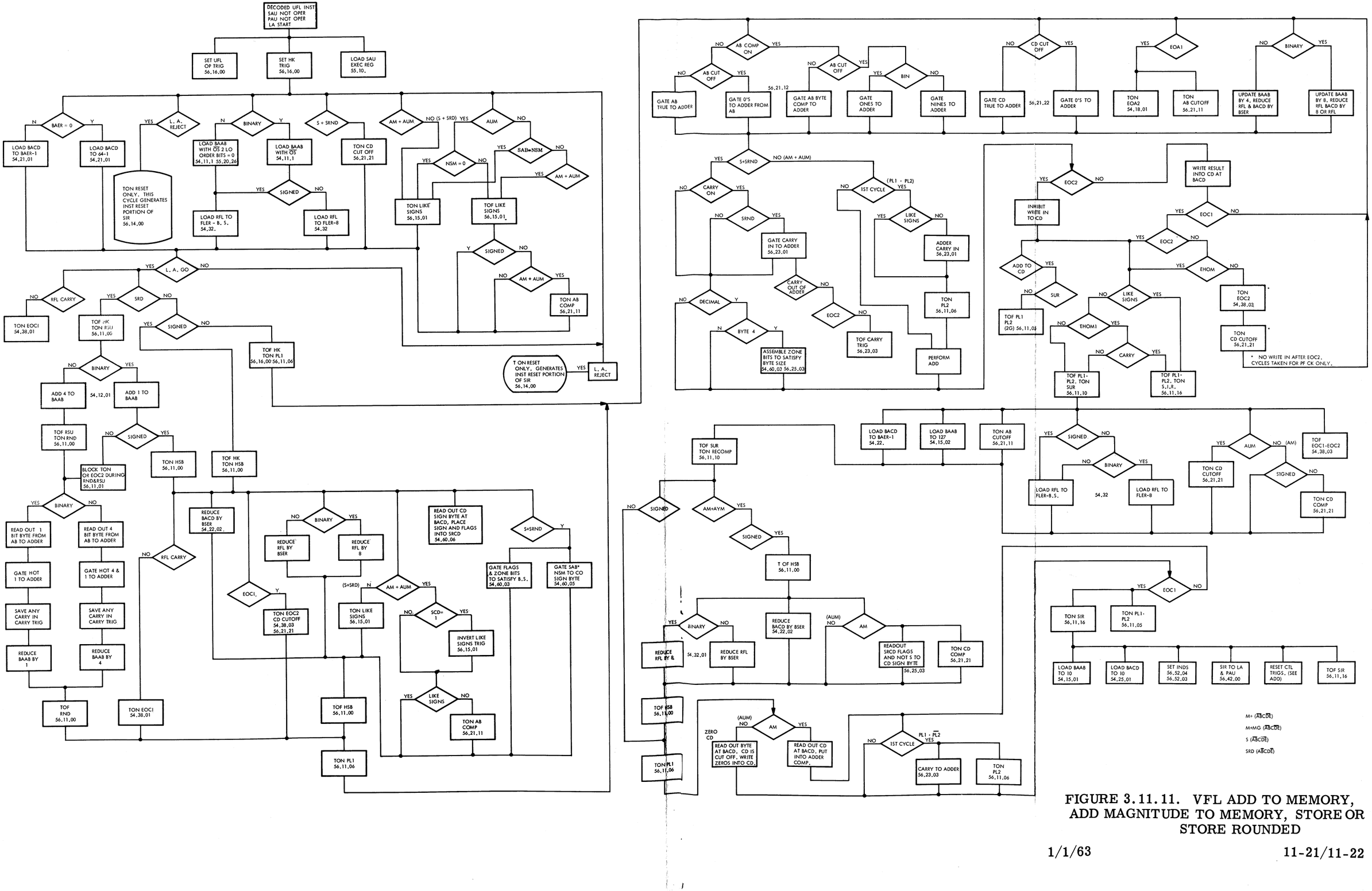
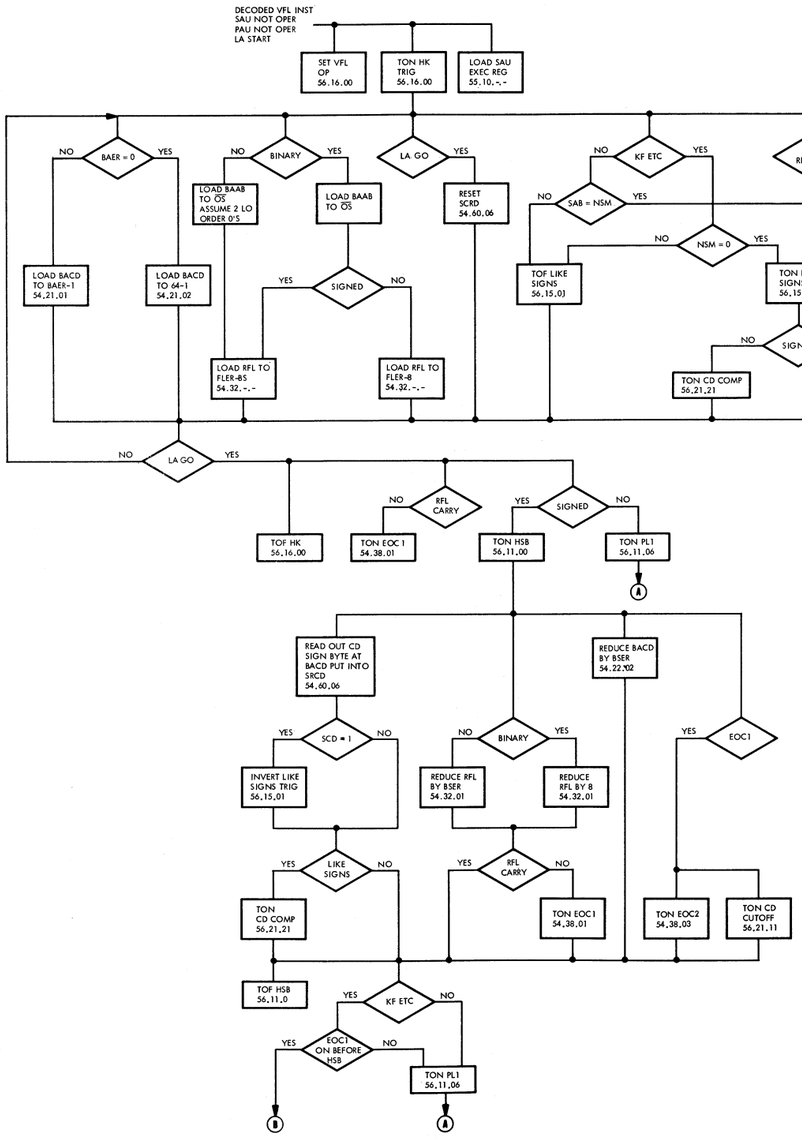


FIGURE 3.11.11. VFL ADD TO MEMORY, ADD MAGNITUDE TO MEMORY, STORE OR STORE ROUNDED



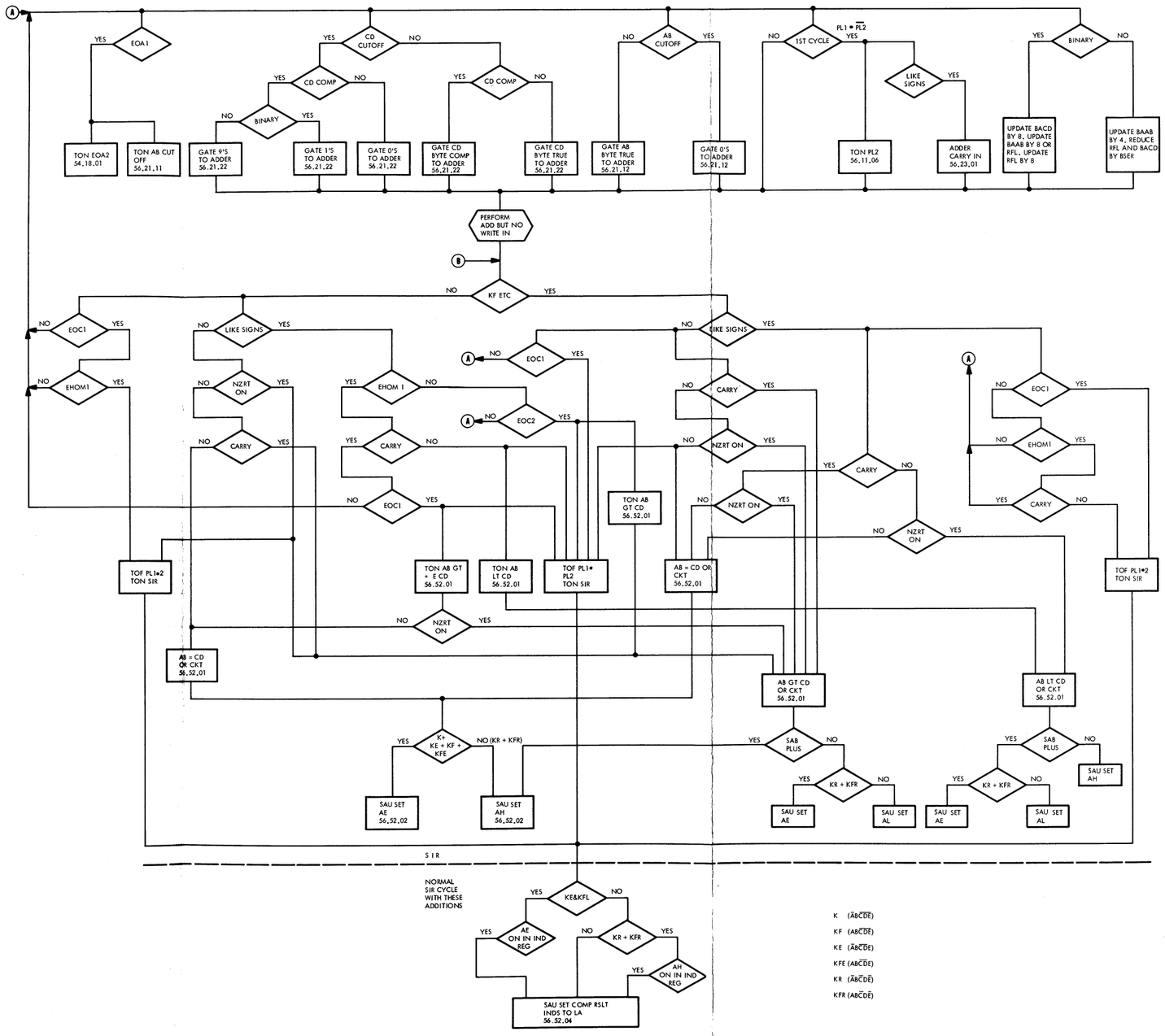


FIGURE 3.11.12. VLF COMPARE INSTRUCTIONS

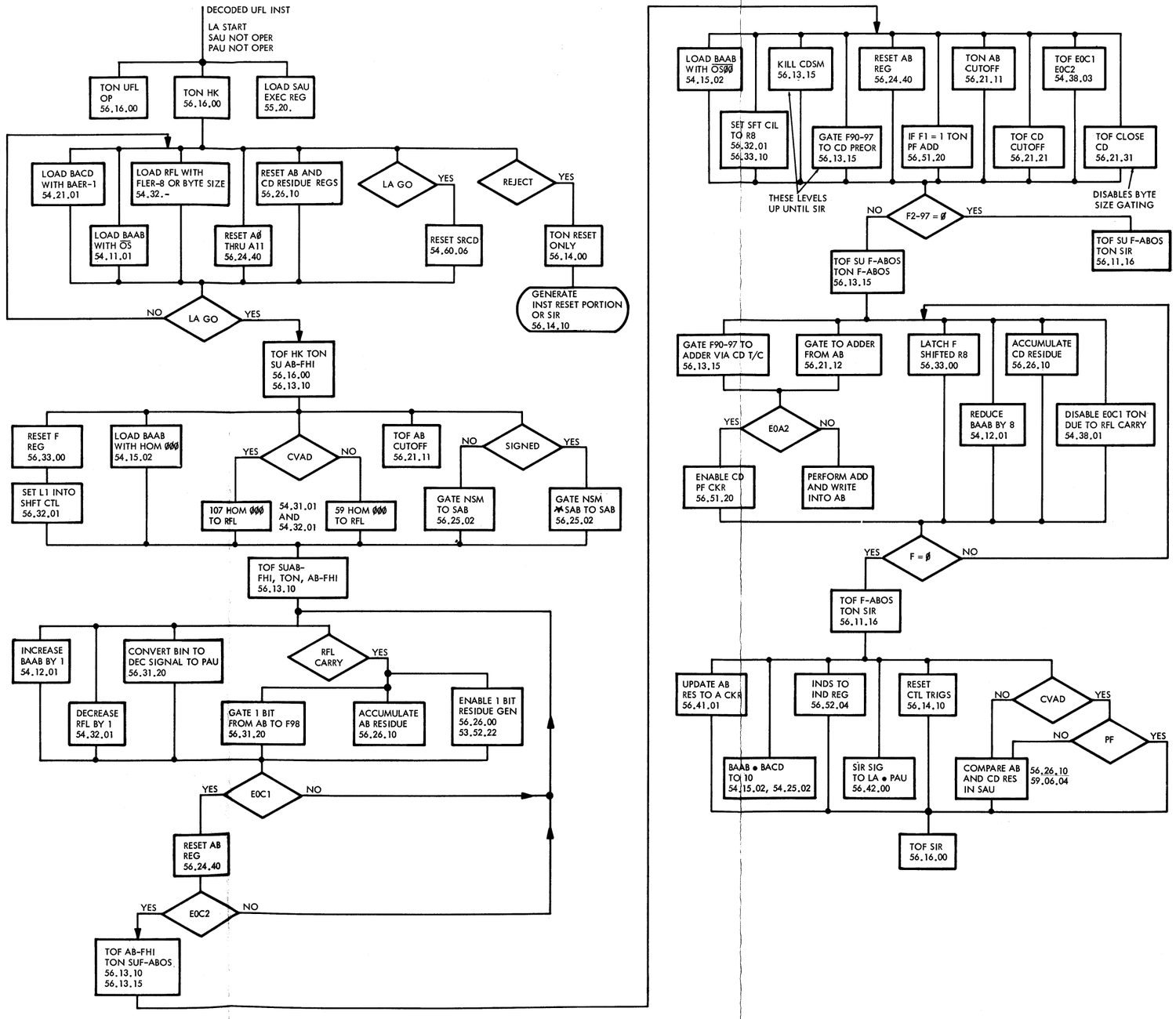


FIGURE 3.11.13. BINARY CONVERT AND BINARY CONVERT DOUBLE

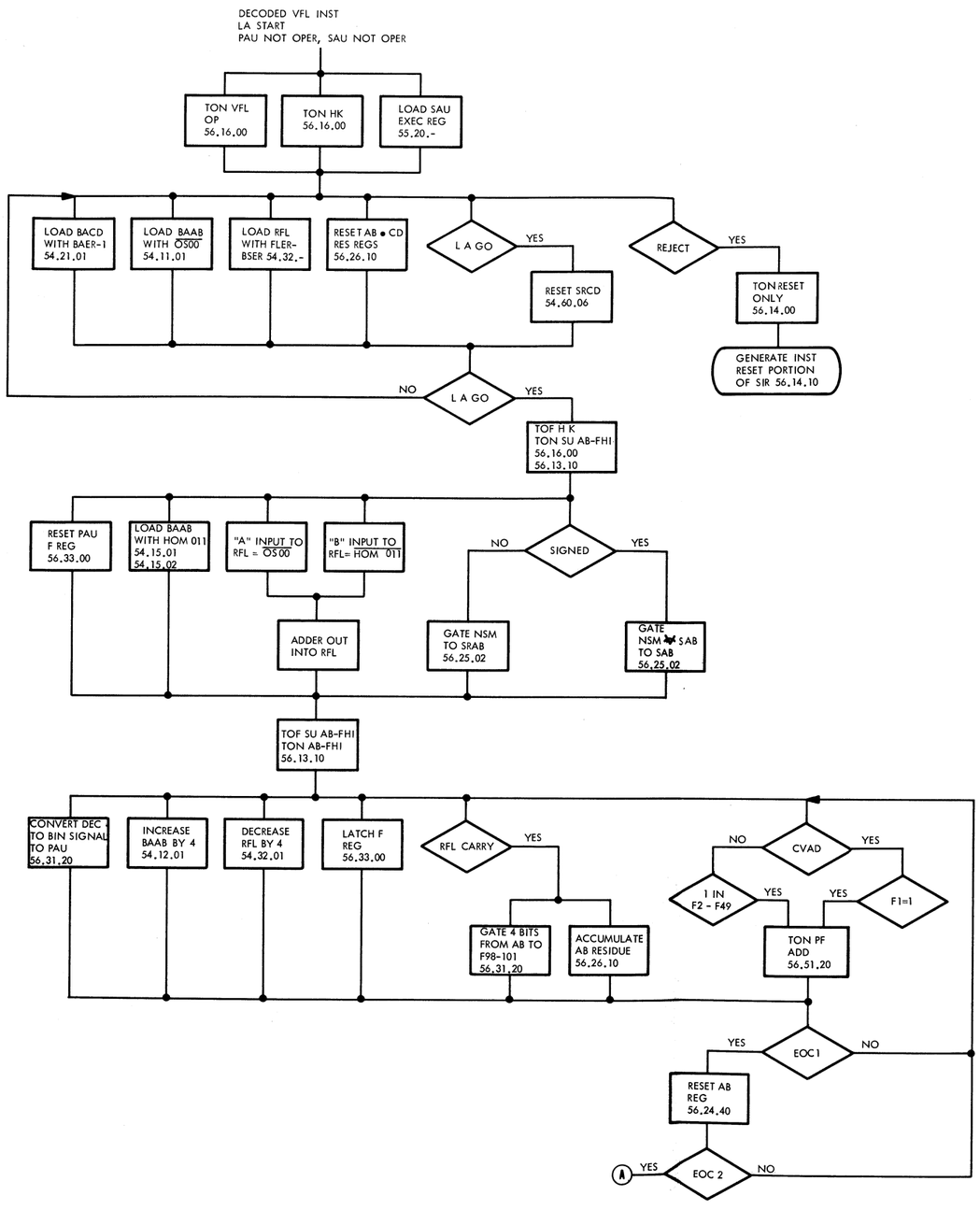


FIGURE 3.11.14. DECIMAL CONVERT AND DECIMAL CONVERT DOUBLE

INDEX 4-1. CORRECTIVE PROCEDURES

PROCEDURE NUMBER	PROCEDURE TITLE	ISSUE DATE
1	Adjustment of Storage Bus Control and Core Storage Timing	2/1/62
2	+12VDC Power Supply Voltage Adjustment	1/1/63
3	XTD Tunnel Diode Replacement	1/1/63
4	XTD Memory Cell Replacement	1/1/63
5	Word Driver Tuning, New Word- Driver Card	1/1/63
6	XTD Fuse or Resistor Replacement	1/1/63
7	Index Tunnel Diode Storage Tuning Procedure	1/1/63

INDEX 4-2. LIST OF ILLUSTRATIONS

FIGURE NUMBER	FIGURE TITLE	ISSUE DATE
4.1.1	Data-Out Gate Timing	2/1/62
4.1.2	Select 1Y Pulse Timing	2/1/62
4.1.3	Select 2Y Pulse Timing	2/1/62
4.1.4	MEM SEL LA Pulse Timing	2/1/62
4.2.1	+12VDC Power Supply and Adjustment Chart	1/1/63
4.3.1	Tunnel Diode Array Card	1/1/63
4.3.2	Tunnel Diode Storage Panel	1/1/63
4.3.3	Memory Cell Assembly	1/1/63
4.3.4	Tunnel Diode	1/1/63
4.4.1	Memory Cell	1/1/63
4.4.2	Soldering of Tunnel Diode to Array Card	1/1/63
4.6.1	XTD Fuse Replacement	1/1/63

INDEX 4-3. LIST OF TABLES

TABLE NUMBER	TABLE TITLE	ISSUE DATE
4.1.1	Memory Select Pulse Delay Line Card Locations	2/1/62
4.1.2	Memory Select LA Level Pulse Delay Line Locations	2/1/62
4.7.1	Octal Bit Designation	1/1/63

This procedure describes how to check and adjust the timing between core storage units (CSU's) and the storage bus control of the 7101 Central Processor Unit, Serial No. 30,004 and higher. The procedure sets test conditions for each CSU by executing store and fetch operations from the CPU, exchange, and disk synchronizer CE consoles and then checking and adjusting the fixed and/or tapped delays of the intercommunication lines between the core storage and storage bus control units.

The storage bus control and CSU timing relationship must be checked and adjusted whenever the CPU clock frequency is changed or CPU clock sample pulses are realigned.

EQUIPMENT

Oscilloscope - Tektronix type 551 dual-beam, with type 53/54L,fast-rise, calibrated preamplifiers.

PROCEDURAL STEPS

A. Preparation

1. Allow warmup period of 30 minutes for CSU's, CPU, exchange, disk synchronizer, and oscilloscope.

2. During latter part of warmup period, check transfer and execution of instructions from 7101 CE console to ensure that associated CPU controls, registers, and timing sequencers are functioning properly. This test is accomplished as follows:

   a. Set Load Index (LX)instruction into both half-words of 7101 CE console PANEL KEYS.

   b. Set MAINT MOD level switch to DOWN position.

   c. Set RPT INST level switch to DOWN position.

   d. Set TIME CLOCK level switch to DOWN position.

   e. Set IRPT level switch to DOWN position.

f. Set INH SCAN level switch to DOWN position.

g. Depress MASTER (Reset) pushbutton.

h. Depress START (Clock) pushbutton.

i. Depress START (Program) pushbutton.

3. If instruction transfer between PANEL KEYS and 1Y and 2Y registers is not satisfactorily timed, temporarily adjust PANEL KEYS timing delay line on card 11A2H16 (logic 18.05.01.1)

4. Repeat step 2, using Store Index (SX) instruction.

5. After warmup period, compensate oscilloscope probes, using internal oscilloscope calibrator.

6. Execute Sample Pulse Alignment Check procedure (Check Procedure 1 of this manual) to ensure accuracy of clock sample pulse adjustments.

B. Timing of Store Operations

1. Set CPU store test routine on 7101 CE console:

a. Set Store Index (SX) instruction to CSU A0 into both half-words of PANEL KEYS.

b. Depress MASTER (Reset) pushbutton.

c. Depress START (Clock) pushbutton.

d. Depress START (Program) pushbutton.

2. Adjust SM memory-select timing pulse (measured at card socket pin 11A2H21F, logic 11.12.02.1) so it is 200 nanosec wide and occurs 150 nanosec after leading edge of an SP pulse (measured at card socket pin 11A2K24F, logic 11.12.02.1). The delay lines for these adjustments are on cards 11A2F24 and 11A2F23 (logic 11.12.02.1).

3. Adjust MEM SEL pulse delay so changing memory address bus (MAB) information will be properly sampled into memory address register (MAR) of CSU A0 (logics 01.02.00.1 through 01.02.04.1). The delay line for this adjustment is on card 11A3J27 (logic 13.06.01.1).

4. Adjust MEM RD out pulse delay line (contained on card 11B1E21, logic 14.01.01.1) so MEM RD out pulse will arrive at readout trigger of CSU A0 (measured at pin 3 of card socket 01C1C13, logic 01.02.04.1) at same time that MAB information arrives at MAR (logics 01.02.00.1 through 01.02.04.1).

5. Adjust Busy trigger reset delay line so that Busy trigger (logic 13.05.01) is on for 1800 nanosec. The delay line for this adjustment is on card 01B1B22 (logic 01.12.00.1) of the selected CSU.

6. Change address portion of Store Index (SX) instruction in 7101 CE console PANEL KEYS to specify next sequential CSU. Repeat steps 1 through 5 to adjust delay lines associated with MEM SEL pulse, MEM RD out pulse, and Busy trigger reset pulse for CSU's A1, B0, B1, B2, and B3. The location of the MEM SEL delay line card for each of these CSU's is shown in table 4.1.1.

TABLE 4.1.1. MEMORY SELECT PULSE DELAY LINE CARD LOCATIONS

Core Storage Unit	Delay Line Card Location	Logic Page
A1	11A3J24	13.06.02.1
B0	11A3J26	13.06.01.1
B1	11A3J25	13.06.01.1
B2	11A3J23	13.06.02.1
B3	11A3J22	13.06.02.1

7. After above operations, adjust data-in-gate pulse delay lines (contained on CSU cards 01B1B18 and 01B1B16, logic 01.12.02.1) to sample selected index register data into memory data register (MDR) of each CSU (logics 01.18.04.1 through 01.18.07.1).

C. Timing of Fetch Operations

1. Set CPU fetch test routine on 7101 CE console:

   a. Set Load Index (LX) instruction to CSU A0 in both half-words of PANEL KEYS.

   b. Depress MASTER (Reset) pushbutton.

   c. Depress START (Clock) pushbutton.

   d. Depress START (Program) pushbutton.

2. Adjust RA DCR STROBE pulse (measured at pin E of card socket 12B1J21, logic 17.05.02.1) so it samples RA parity bit (measured at pin E of card socket 12B1J22, logic 17.05.02.1). The delay line for this adjustment is on card 12B1K19 (logic 17.04.06.1).

3. Adjust data-out-gate pulse (measured at pin A of CSU card 01B1B10, logic 01.12.03.1) so it is 290 nanosec wide by varying delay line on card 01B1C13 (logic 01.12.03.1). Check data-out-gate pulse (measured at card socket pin 01A1H24B, logic 01.13.00.1) to ensure that it does not occur earlier than 1050 nanosec after select-memory pulse (measured at card socket pin 01B1C06D, logic 01.12.00.1). If time difference is too short, increase delay by adjusting delay line on card 01B1C19 (logic 01.12.00.1). Simultaneously, check read/write trigger (measured at card socket pin 01D2J06B, logic 01.08.00.1) to ensure that it is changing state between X- or Y read/write timing pulses (measured at card socket pins 01D2K09B and 01D2K04G, logic 01.12.02.1). The delay line for adjusting the setting of this trigger is also on card 01B1C19 (logic 01.12.00.1).

The IMOB data pulses measured at the 1Y register (logic 22.11.01.1) through 22.11.37.1) and at lookahead level 4 (logic 31.01.01.1 through 31.02.10.1) should bracket (overlap) the sixth SP pulse (measured at card socket pin 11A3B20F, logic 12.10.04.1) that is generated after the SP pulse which initiated the gate I pulse (measured at card socket pin 11A3B20G; refer to step 3). If above condition does not exist, adjust data-out-gate pulse timing by varying delay line on card 01A1F26 (logic 01.13.00.1). Adjust accurately even though pulse may have to be realigned after select pulses have been adjusted. (See fig. 4.1.1.)

4. Check timing of SEL 1Y pulse (measured at card socket pin 17A2C25U, logic 28.72.41.1) to ensure that pulse brackets (overlaps) fifth and sixth SP pulses (measured at card socket pin 17A2C25-3) that occur after SP pulse which initiated gate I pulse (measured at card socket pin 11A3B20G; refer to step 3). If above condition does not exist, adjust SEL 1Y pulse timing by varying delay line on card 12B1K15 (logic 17.06.01.1). (See fig. 4.1.2.)

5. Check timing of SELECT 2Y pulse (measured at card socket pin 17A2C21U, logic 28.72.51.1) to ensure that pulse brackets (overlaps) fifth and sixth SP pulses (measured at card socket pin 17A2C21-3) that occur after SP pulse which initiated gate I pulse (measured at card socket pin 11A3B20G; refer to step 3). If above condition does not exist, adjust SEL 2Y pulse timing by varying delay line on card 12B1K16, logic 17.06.01.1. (See fig. 4.1.3.)

6. Set CPU to test timing of the four MEM SEL LA pulses at 7101 CE console:

   a. Set a Load instruction (from CSU A0) into both half-words of PANEL KEYS.

   b. Depress MASTER (Reset) pushbutton.

   c. Depress START (Clock) pushbutton.

   d. Depress START (Program) pushbutton.

7. Check and adjust timing of the four MEM SEL LA level pulses by using signal measuring points and delay line location information listed in table 4.1.2. When checking one of these pulses, bypass other lookahead levels by means of LA disable switches on 7101 CE console. Adjust each MEM SEL LA pulse so it brackets (overlaps) fifth SP pulse that occurs after SP pulse which initiated gate I pulse (measured at card socket pin 11A3C13G; refer to step 3). (See fig. 4.1.4.)

TABLE 4.1.2. MEMORY SELECT LA LEVEL PULSE DELAY LINE LOCATIONS

Test Pulse	Signal Measuring Points			Delay Line	
	LA Pulse	SP Pulse	Logic Page	Location	Logic Page
MEM SEL LA 1	18A3A21B	18A3A21C	36.01.05.1	12B1K18	17.06.01.1
MEM SEL LA 2	18A3A21-6	18A3A21-5	36.01.06.1	12B1K10	17.06.02.1
MEM SEL LA 3	18A3C21B	18A3C21C	36.01.07.1	12B1K12	17.06.02.1
MEM SEL LA 4	18A3C21-6	18A3C21-5	36.01.08.1	12B1K13	17.06.02.1

8. Use Load Index instruction test routine (refer to step 1) to check time at which data-in-gate pulse samples IMOB data into 1Y register. Next, use Load instruction test routine (refer to step 5) to check time at which data-in-gate pulse samples IMOB data into lookahead level 4 (LA 4). If IMOB data is not being correctly sampled into 1Y register and/or LA level 4, refer to step 3 and vary timing of data-out-gate pulse so that both transfers are made correctly.

9. Repeat step 3 for each of the other CSU's to ensure that IMOB data at 1Y and LA 4 registers is identical in width and relative position for all CSU's. Also, repeat step 7 for each of the other CSU's to ensure that IMOB data will be correctly transferred into 1Y and LA 4 registers from all CSU's.

10. Set up Load Index instruction test routine (refer to step 1) to check timing of data transfer from PANEL KEYS. Using RA-decoder-strobe pulse (measured at card socket pin 12B1J25F, logic 17.05.01.1) as a sync point, check time relationship between a pulse on a data line from CSU A0 and a pulse on a data line from PANEL KEYS. If these two pulses do not coincide, adjust PANEL KEYS delay line on card 11A2H16 (logic 18.05.01.1) so that the two data pulses coincide.

11. Set up exchange CE console controls to execute a data fetch operation from CSU A0:

    a. Depress SIM WR switch.

    b. Set a valid A0 address in WORD ADDRESS switches.

    c. Set a DATA WORD XFER switch to select a channel.

    d. Set selected channel address in EXCHANGE MEM ADR switches.

    e. Store address in control word by depressing EX MEM TEST switch, setting LOAD MEM switch down, depressing SINGLE CYCLE PB twice, and clearing LOAD MEM switch.

f. Depress MN MEM (Main Memory) TEST switch.

g. Depress MACHINE RESET.

h. Set BLK CW MOD switch down.

i. Depress START pushbutton.

12. Adjust SET BX-BFR pulse by varying delay line on card 12B1J13 (logic 17.06.03.1) so BUS SET BR pulse samples data on BX MOB to BX buffer register.

13. Set disk synchronizer CE console controls to execute a data fetch operation from CSU A0:

    a. Store a control word containing an A0 memory address into memory by means of PANEL KEYS on 7101 CE console.

    b. On disk sync console, set TEST switch to DS to SIGMA position.

    c. Set following switches down:

        (1) BLOCK WCO

        (2) SUP +1 SWC

        (3) WR STA

        (4) SUP + 1 MOD

    d. Depress WR pushbutton.

    e. Set control word address into CONTROL WORD ADDRESS switches.

    f. Depress following pushbuttons in order:

        (1) GEN RESET

        (2) CW TC

        (3) WORD CYCLE

        (4) SEL DS MEM (depress twice)

    g. Depress RD/WRT START pushbutton.

14. Adjust SEL HX pulse by varying delay line on card 12B1J12 (logic 17.06.03.1) so HX MOB-to-WDR pulse samples data on HX MOB into word register.

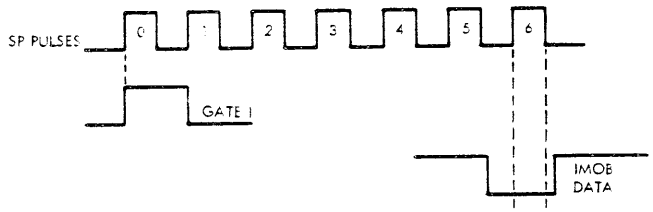


FIGURE 4.1.1. DATA-OUT GATE TIMING

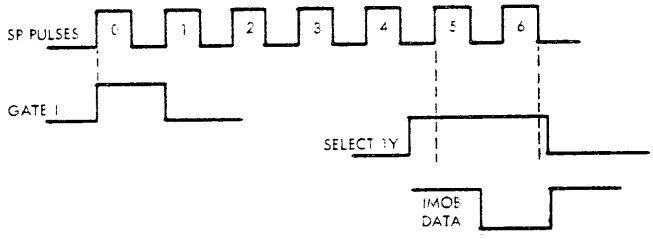


FIGURE 4.1.2. SELECT 1Y PULSE TIMING

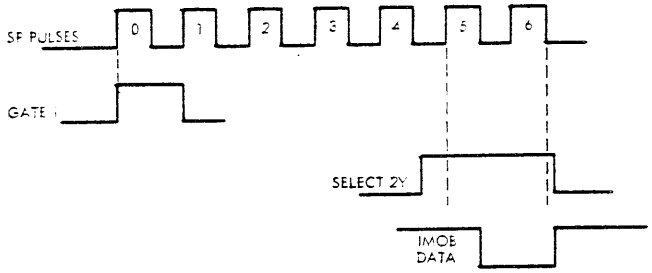


FIGURE 4.1.3. SELECT 2Y PULSE TIMING

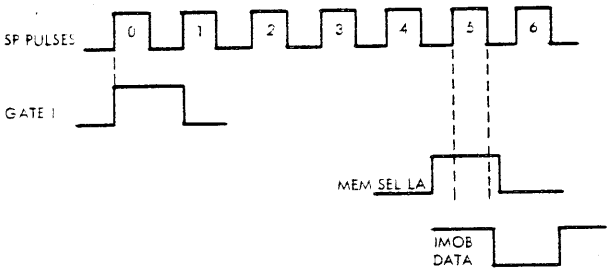


FIGURE 4.1.4. MEM SEL LA PULSE TIMING

+12VDC POWER SUPPLY VOLTAGE ADJUSTMENT

DESCRIPTION

This procedure is used to adjust the +12vdc power supply (P/N 5246540).

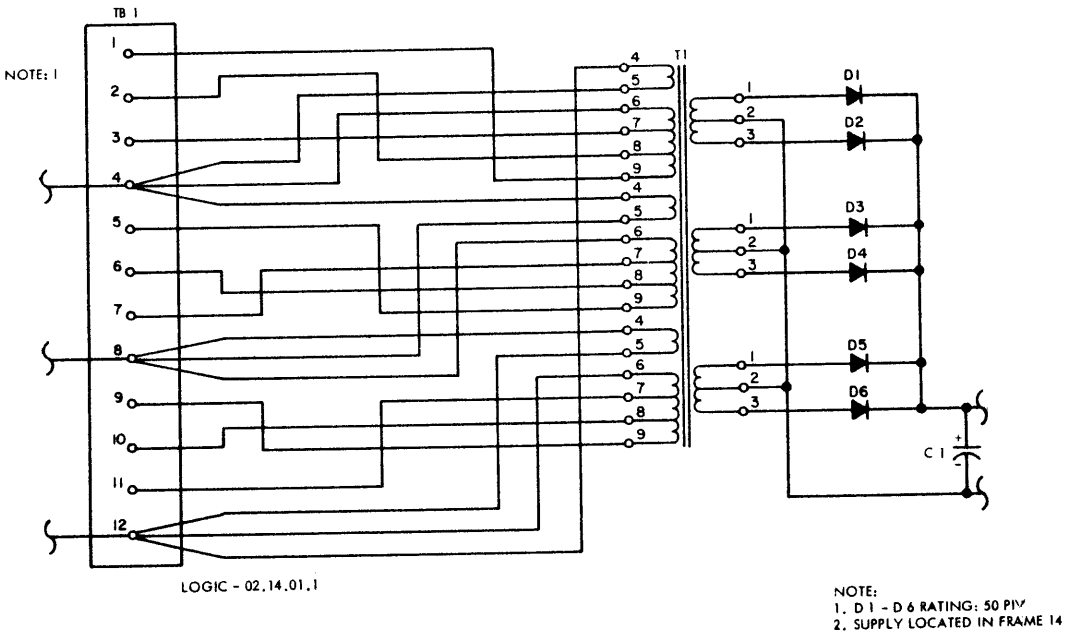
PROCEDURAL STEPS

DANGER

Make sure that all power to the power supply is off before attempting power supply adjustments. Use a voltmeter to determine whether voltages are present. Make certain that the voltage adjustment procedure is understood before attempting any adjustments.

For adjustments of the supply, first determine the present adjustment of the supply. If the adjustment is at the center position (table in fig. 4.2.1), then to increase or decrease the voltage, move those wires required for that particular increase or decrease as shown in the table. For example, for an increase of 0.12v, move following wires and read output voltage to see that change has been made correctly.

Wire	From Pin	To Pin
Gray	4	3
Orange	8	7
Yellow	12	11



A. Power Supply Schematic

VOLTAGE ADJUSTMENT CHART ON TB-1

VOLTAGE CHANGE FROM CENTER POSITION	1	2	3	4	5	6	7	8	9	10	11	12
	CONNECT WIRES											
INCREASE MAGNITUDE .72	GY			01 BL	O			02 BR	Y			03 V
INCREASE MAGNITUDE .60	GY		01 BL		O		02 BR		Y		03 V	
INCREASE MAGNITUDE .48		GY		01 BL		O		02 BR		Y		03 V
INCREASE MAGNITUDE .36		GY	01 BL			O	02 BR			Y	03 V	
INCREASE MAGNITUDE .24	GY	01 BL			O	02 BR			Y	03 V		
INCREASE MAGNITUDE .12			GY	01 BL			O	02 BR			Y	03 V
CENTER POSITION				01 BL GY				02 O BR				03 Y V
DECREASE MAGNITUDE .12			01 BL	GY			02 BR	O			03 V	Y
DECREASE MAGNITUDE .24	01 BL	GY			02 BR	O			03 V	Y		
DECREASE MAGNITUDE .36		01 BL	GY			02 BR	O			03 V	Y	
DECREASE MAGNITUDE .48		01 BL		GY		02 BR		O		03 V		Y
DECREASE MAGNITUDE .60	01 BL		GY		02 BR		O		03 V		Y	
DECREASE MAGNITUDE .72	01 BL			GY	02 BR			O	03 V			Y

NOTE: 2

V = VIOLET GY = GRAY
BL = BLUE O = ORANGE
BR = BROWN Y = YELLOW

01 = INPUT WIRE FOR PHASE 1
02 = INPUT WIRE FOR PHASE 2
03 = INPUT WIRE FOR PHASE 3

NOTES:

1 - THE +12V SUPPLY IS ADJUSTED BY RECONNECTING THE WIRES ON TB-1 AS INDICATED IN VOLTAGE ADJUSTMENT CHART TO OBTAIN THE DESIRED OUTPUT VOLTAGE.

2 - ALL BLACK WIRES ARE TO REMAIN ON THE POSITION TO WHICH THEY ORIGINALLY WERE CONNECTED.

B. Adjustment Chart

FIGURE 4.2.1. +12VDC POWER SUPPLY AND ADJUSTMENT CHART

DESCRIPTION

This procedure is used to replace tunnel diodes.

EQUIPMENT

Jig Assembly (P/N 523007)

Soldering Iron (P/N 5230119)

Connector Board (P/N 361555)

Field Replacement Memory Cell (P/N 361569)

Tunnel Diode (P/N 361564)

Flux (P/N 5230037)

Chain Nose Pliers (P/N 450786)

PROCEDURAL STEPS

1. Remove array card (fig. 4.3.1) from panel (fig. 4.3.2) by alternately applying a steady at first pull the top and then the bottom of the card.

2. Place array card in jig assembly.

3. Using soldering iron, apply heat to lead on connector board, which comes from memory cell (fig. 4.3.3). Apply pressure to connector board with chain nose pliers, toward memory cell. This will loosen joint so that tunnel diode negative leads can be straightened. Apply minimum amount of heat. When tunnel diode negative leads are straight (one lead is for the tunnel diode to be replaced; the other is for the adjacent cell), remove the tunnel diode and connector board as a unit.

4. Curve-trace the new tunnel diode before it is used as a replacement.

5. Place new tunnel diode (fig. 4.3.4) on a new connector board as shown in figure 4.3.3. Pull tunnel diode up to connector board and bend and trim wires. Pull connector board down so that tunnel diode cap rests on standoff block of memory cell.

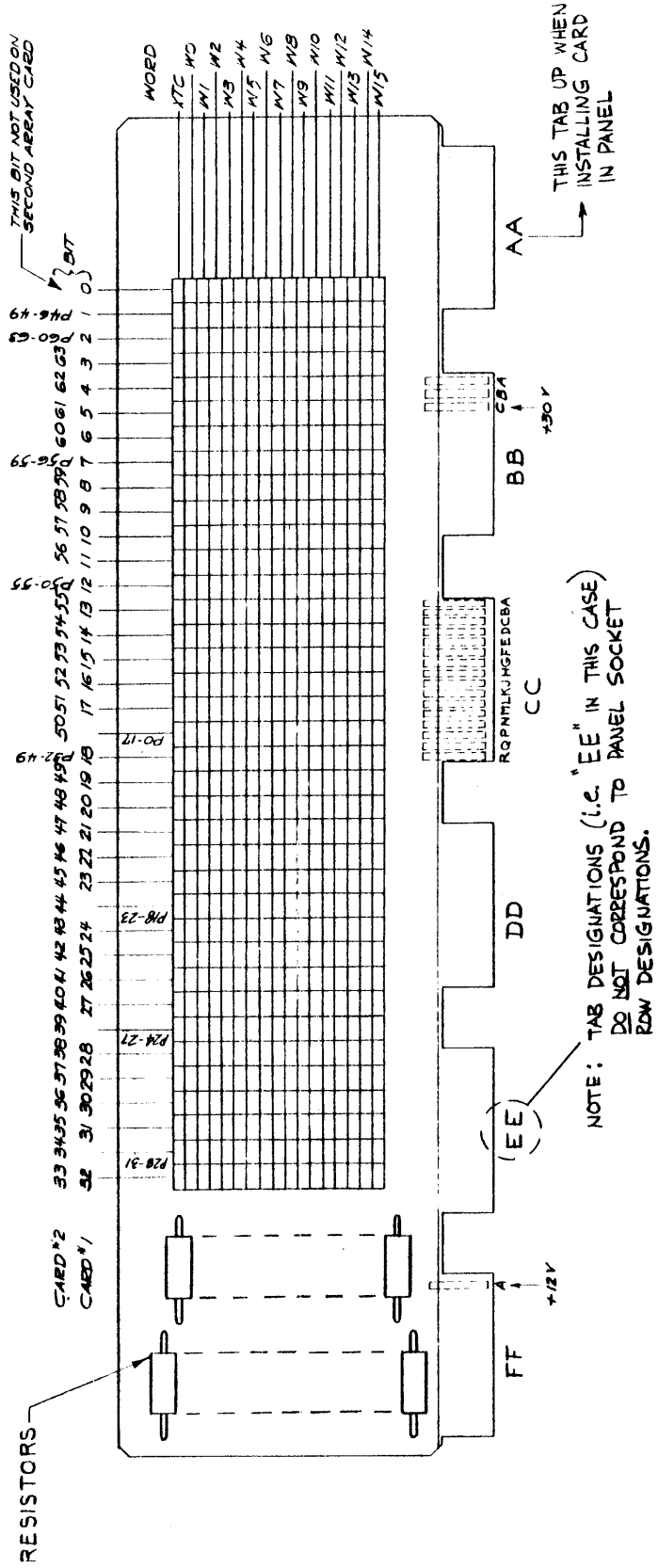


FIGURE 4.3.1. TUNNEL DIODE ARRAY CARD

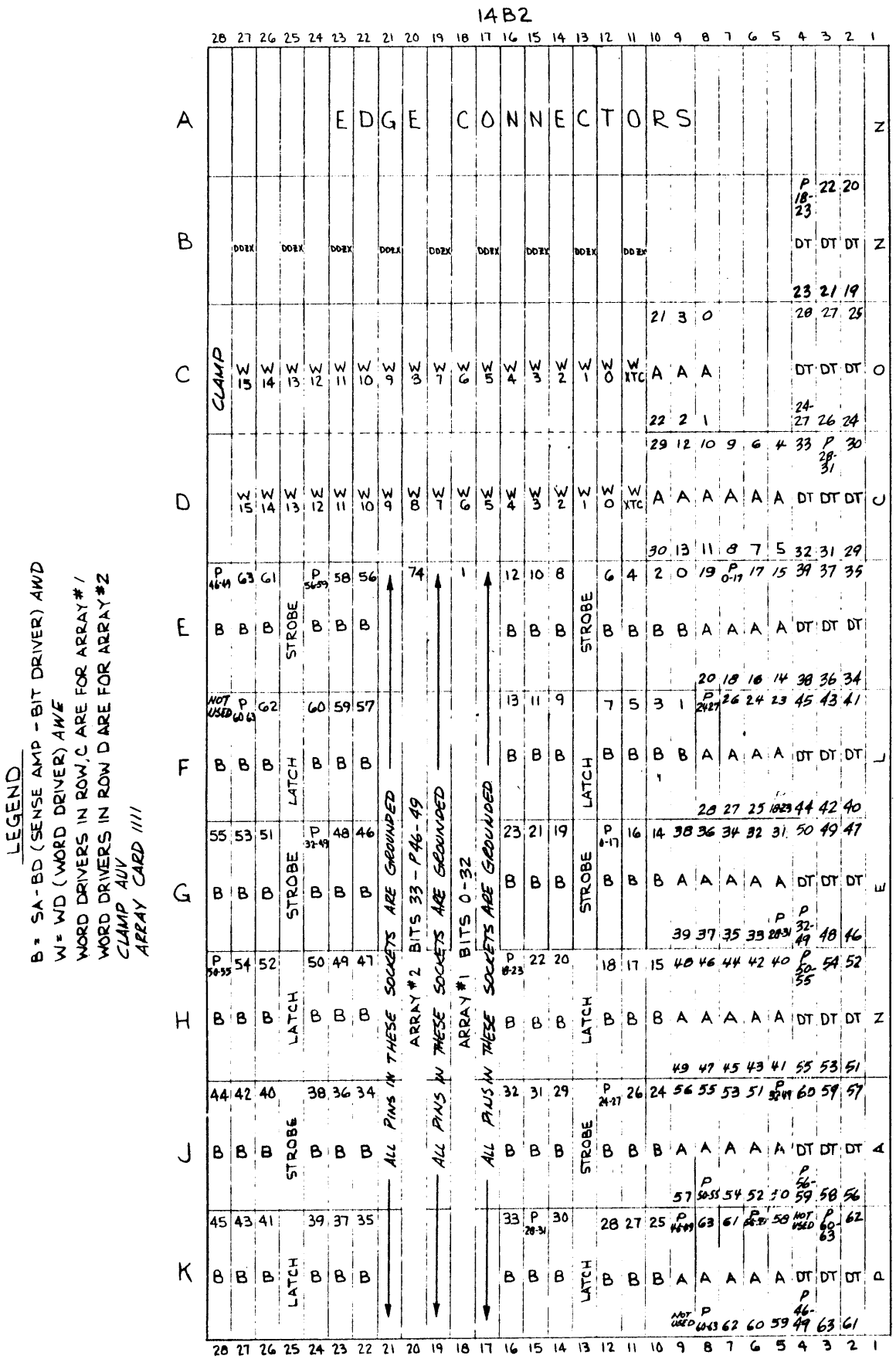


FIGURE 4.3.2. TUNNEL DIODE STORAGE PANEL

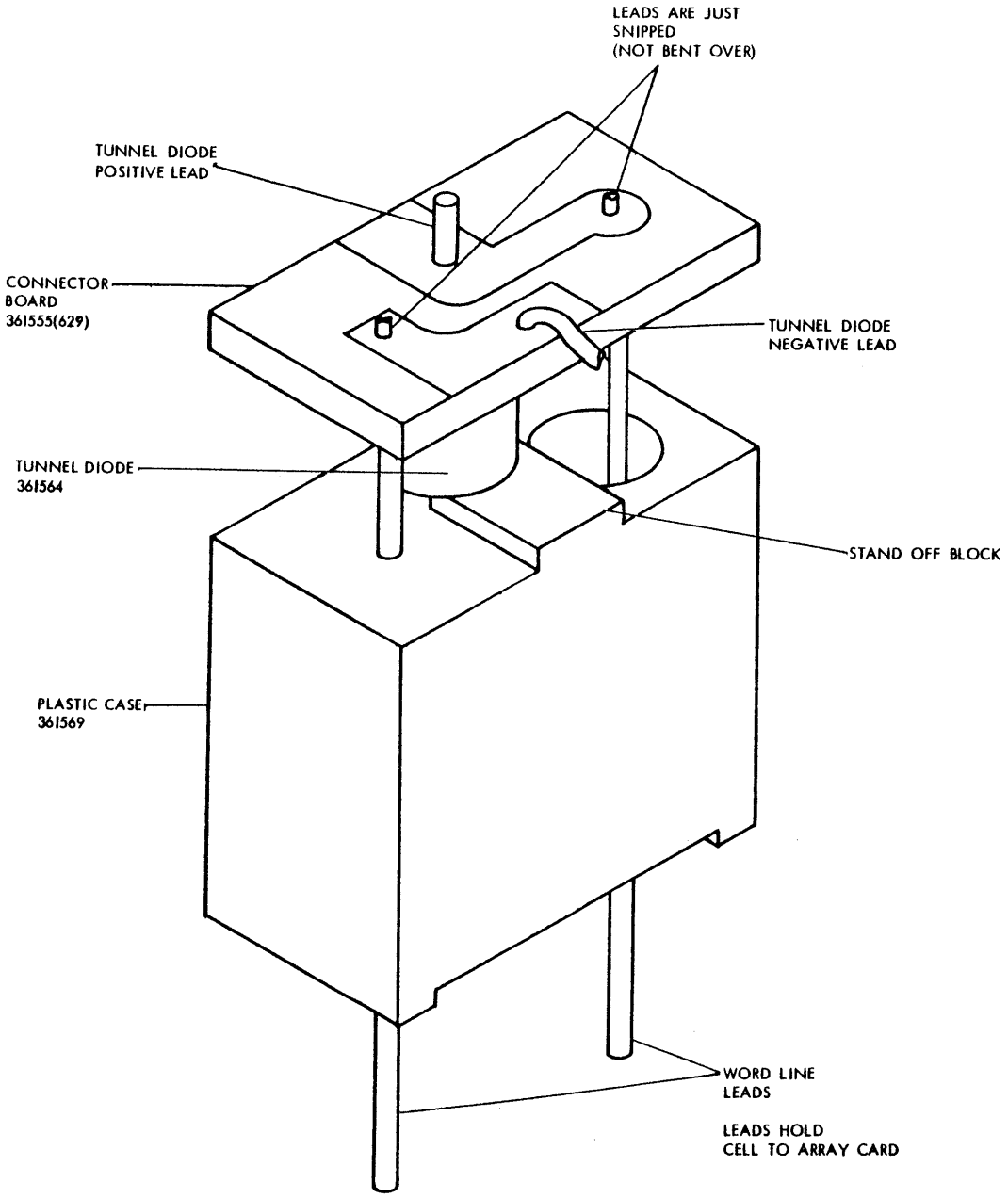


FIGURE 4.3.3. MEMORY CELL ASSEMBLY

6. Clean lands on the connector board with a rubber eraser. Scrape the tunnel diode lands tightly with tweezers or a pocket knife.

7. Using rosin-core solder, solder wires to connector board, using minimum heat.

CAUTION

Do not damage connector board.

8. Curve-trace all affected diodes before replacing array card in panel.

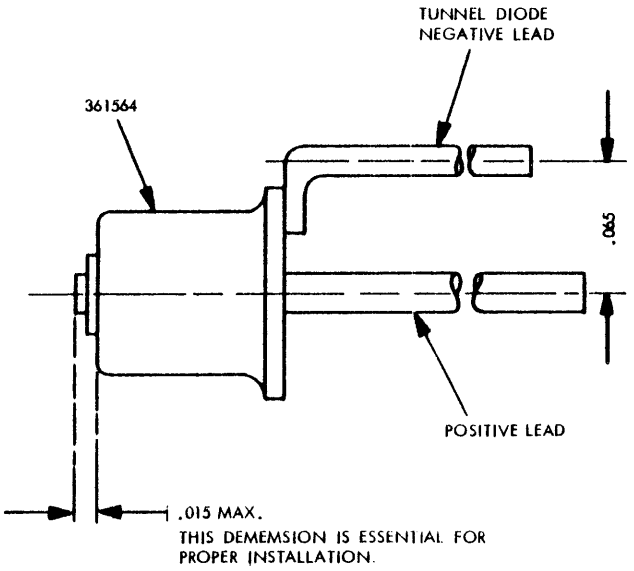


FIGURE 4.3.4. TUNNEL DIODE

DESCRIPTION

This procedure is used to replace the memory cell.

EQUIPMENT

Jig Assembly (P/N 5230007)

Soldering Iron (P/N 5230119)

Memory Cell (P/N 361575)

Segment Wire (P/N 361574)

Epoxy (P/N 5230042)

PROCEDURAL STEPS

1. Place array card in jig assembly.

2. To remove the connector board of the memory cell to be replaced, unsolder wires, i.e., tunnel diode negative leads that overlap adjacent connector boards.

3. To remove memory cell, apply soldering iron to word line leads of memory cells to be changed, lift wires from land, using round toothpick, and cut wires (fig. 4.4.1). Continue applying heat to word line leads extracting memory cell.

4. Check new memory cell to see if the segment wire is bonded in memory cell slot; if not, apply epoxy to slot, and let it cure undisturbed for 24 hours.

5. Place new memory cell (fig. 4.4.2) on array card with segment wire. Put each end of segment wire through holes in array card, bend wires to land, apply flux and solder; trim off excess wire.

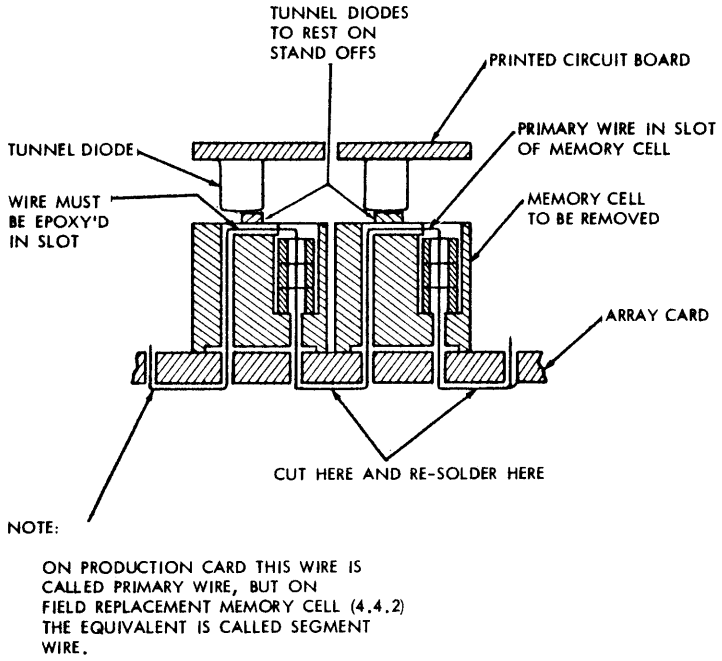


FIGURE 4.4.1, MEMORY CELL

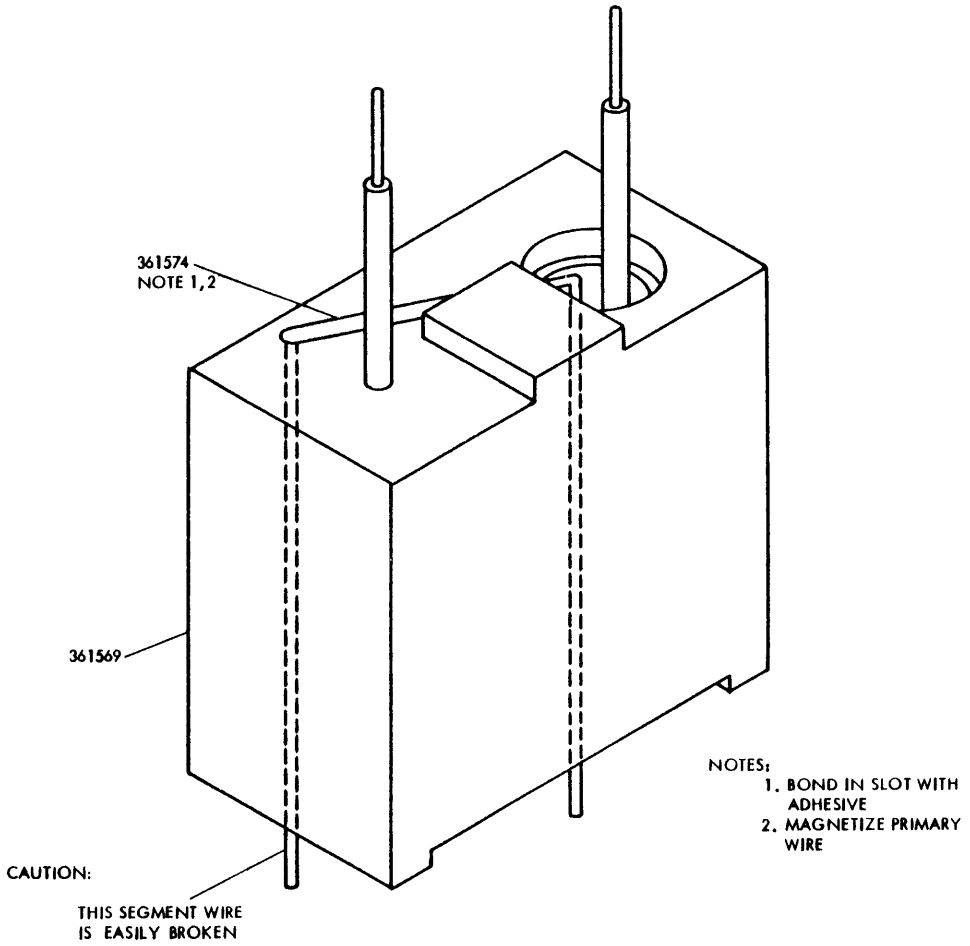


FIGURE 4.4.2. SOLDERING OF TUNNEL DIODE TO ARRAY CARD

DESCRIPTION

This procedure describes the tuning of a word-driver card that replaces the old card in the index tunnel diode register.

REQUIREMENTS

Vacuum Tube Voltmeter (P/N 5231703)

PROCEDURAL STEPS

Amplitude potentiometer will be set to 0 ohm at the factory and must remain at 0 ohm.

1. Set turn-on-time potentiometer (1K) to 500 ohms, using VTVM meter.
2. Turn off d-c power, and replace card in panel.
3. Turn on power.
4. Measure word-driver output, test point table 2.7.1 (Sect. 2).
5. To set turn-on-time potentiometer, see Check Procedure 7.

DESCRIPTION

This procedure is used to replace the fuse or resistor within the index tunnel diode register circuitry.

EQUIPMENT

Jig Assembly P/N 5230007

Soldering Iron P/N 5230119

Chain Nose Pliers P/N 450786

Fuse P/N 361570

Resistor P/N 550051

VTVM P/N 5231703

PROCEDURAL STEPS

1. Place array card in jig assembly.

2. Apply soldering iron to fuse lead on land side of card, and apply pressure with chain nose pliers on fuse side of array card so that bent portion of lead is pushed away from land. Straighten bent lead, and remove fuse.

CAUTION

Use minimum heat to avoid land damage (fig. 4.6.1.)

3. Place new fuse on array card; bend and trim leads.

4. Apply flux and solder, using minimum heat. If circuit land pulls away from card, the wires should be soldered together directly, and epoxy should be used to cement the wires and land to the card for mechanical strength.

5. Use same procedure when changing resistor.

CAUTION

Check fuse after this replacement. Using a VTVM, set scale for RX 1 and check for 10 to 25 ohms across fuse on top of card

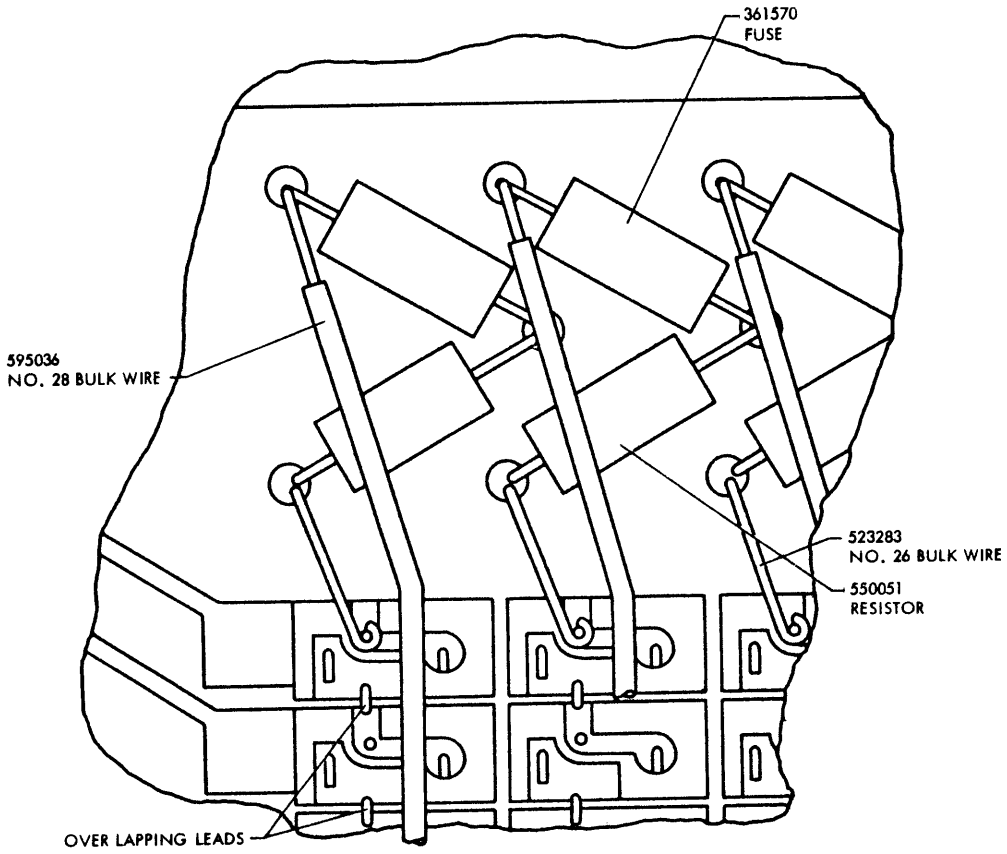


FIGURE 4.6.1. XTD FUSE REPLACEMENT

DESCRIPTION

This procedure is performed if the Index Tunnel Diode Storage Tuning program reveals the picking or dropping of bits by the tunnel diode storage register.

REQUIREMENTS

Index Tunnel Diode Tuning Tape (Two programs, XTDT1 and XTDT2)

Index Tunnel Diode Storage Unit, 7101 Instruction Unit IBM CEIM, Form R23-9916.

GENERAL INFORMATION

1. Tuning memory properly requires two persons: one at the maintenance console and one at frame 14. Since the two must work closely together, a telephone is used to facilitate communications.

2. The front panel on gate 14B must be covered completely throughout the tuning operation. Cardboard inserts may be used to good advantage here, for they are easy to move as tuning progresses from bit to bit.

3. The basic tuning philosophy is as follows:

   a. The bit to be tuned is called the bit in question (BIQ).

   b. The limits of operation for a BIQ are established by varying the discriminating potentiometers on each of the sense amplifier-bit driver (SA-BD) cards for the BIQ to each extreme (i.e., to the points of failure). There are two potentiometers per card, and each card contains circuits. The optimum tuning point for the BIQ is realized by setting the potentiometer to the mid-point of the range defined by the two failing points.

   c. The mid-point of operation is established by counting the number of full turns applied to the tuning slug of the SA-BD potentiometer while adjusting it from one failing point to the other. This range of operation is called the "turns latitude"; it will average approximately 15 turns latitude from one failing point to the other. Some BIQ's will have as little as 5 turns latitude, which is probably the lowest acceptable number of turns for good performance. Some BIQ's may have turns latitude of over 20, which means that these bits have an excellent range of operation. Some BIQ's will appear to have no failing point at one end of the turns latitude (mainly the "drops" end). In this condition the failing point is considered at the end of potentiometer (EOP).

4. The XTDT Tuning Tape program is used as follows:

   The coarse tuning procedure permits use of the XTDT Tuning Tape program to tune the memory to error-free operation. The XTDT tuning tape contains two programs: XTDT1 and XTDT2. The greatest difference between them is that XTDT2 makes use of the printer and XTDT1 does not. The printer's dependence on the diagnostic control program (DCP) requires that the index tunnel diode storage be error-free in operation to prevent losing program control and usually permits memory to be tuned to accept XTDT2. A significant feature of XTDT2 is the initial printout on the printer, which, together with these instructions, furnishes all rules of operation. The XTDT2 is also used as a diagnostic program for troubleshooting this memory. XTDT2's use of DCP allows a more thorough diagnostic check of memory and a printout of error conditions. This feature and the initial printout are the only advantages of XTDT2 over XTDT1. For all normal tuning the XTDT2 portion of XTDT Tuning Tape should be used.

PROCEDURAL STEPS

Using the XTDT2 program, proceed as follows:

1. Set octal designation for BIQ, maintenance keys 0 through 6. (See table 2.6.1 for octal bit designation for each BIQ.)

2. Set maintenance key 31. This switch is set to cause the program to run in the tuning mode. Read program into machine.

   Note

   Since maintenance key 31 is set before the initial program load (IPL), a printout on the printer will indicate all program options available to the customer engineer. Use of these options is determined by the operation from this printout.

3. Set maintenance key 32. Setting this bit causes the error printouts to come out on the typewriter (unless switch 48 is set).

4. Set maintenance key 45. This allows the program to loop on specified bit option available to tests 3 through 7.

5. Set maintenance key 46. This allows the program to loop on selected test option available to all tests.

6. Set maintenance key 48 to display errors.

7. Set maintenance key 59. This bit must be set to prevent a wipeout by DCP should it gain control.

8. Set maintenance key 61. This bit will bypass all attempts to print through DCP and should be set in connection with switches 48 and 32. (See printout on printer.)

9. For data bits, set key 38 to select test 6.
For parity bits, set key 36 to select test 4.

10. Reverse key 63. Program should be cycling in proper test and on proper bit.

11. Turn timing slug clockwise until $ULB 49 lights (fig. 4.3.2).

12. Set Maintenance key 13 and reverse key 63. Setting this key causes bit 49 of the $ULB register to be reset to a zero.

13. Turn timing slug counterclockwise until $ULB goes out.

14. Stop computer.

Note

Steps 15 through 18 are for data bits only.

15. Set maintenance key 40, and turn off key 38.

16. Start computer.

17. Set maintenance key 11, and look for test to change in indicators 32 through 41 of lower boundary register; then turn off key 11.

18. If bit 49 of $ULB goes on, reset 49 to zero, then turn tuning slug counterclockwise until bit 49 no longer comes on. Then adjust clockwise to failure. This is the drop fail point.

19. Stop computer. Turn off key 40, and set key 37. Start computer. Turn slug counterclockwise.

20. Count number of turns counterclockwise from drop failing point. Turn until 49 of $ULB lights; this is the pick fail point.

21. Set SA BD potentiometer halfway between failing points.

22. Proceed to tune next bit, following steps 9 through 21.

TABLE 2.6.1. OCTAL BIT DESIGNATION

Bit	Octal	Bit	Octal	Bit	Octal	Bit	Octal	Bit	Octal
0	000	16	020	32	040	48	060	P0-17	100
1	001	17	021	33	041	49	061	P18-23	101
2	002	18	022	34	042	50	062	P24-27	102
3	003	19	023	35	043	51	063	P28-31	103
4	004	20	024	36	044	52	064	P32-49	104
5	005	21	025	37	045	53	065	P50-55	105
6	006	22	026	38	046	54	066	P56-59	106
7	007	23	027	39	047	55	067	P60-63	107
8	010	24	030	40	050	56	070	P46-49	110
9	011	25	031	41	051	57	071		
10	012	26	032	42	052	58	072		
11	013	27	033	43	053	59	073		
12	014	28	034	44	054	60	074		
13	015	29	035	45	055	61	075		
14	016	30	036	46	056	62	076		
15	017	31	037	47	057	63	077		

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